1. Identify the write-read, write-write, and read-write dependencies in the instruction sequence below by entering each line pair with a dependency in the correct column of the table to the right. For example, if L1 and L4 had a write-write dependency (which they don't), you would enter L1-L4 in the column labeled "write-write".

```
L1:  R1 = 100

L2:  R1 = R2 + R4

L3:  R2 = R4 - 25

L4:  R4 = R1 + R3

L5:  R1 = R1 + 30
```

write-read	write-write	read-write

2. Rename the registers from problem 1 to prevent dependency problems. Identify references to initial register values using the subscript 'a' to the register reference.

Questions 3 and 4 are based on the "in-order issue/in-order completion" execution sequence shown in the figure below.

Decode		Execute			Write		Cycle
I1	I2						1
	I2			I1			2
	I2			I1			3
I3	I4		I2				4
I5	I6		I4	I3	I1	I2	5
I5	I6			I3			6
		I5	I6		I3	I4	7
		I5					8
					I5	I6	9

3. Identify the most likely reason why I2 could not enter the execute stage until the 4th cycle. Will "in-order issue/out-of-order completion" or "out-of-order issue/out-of-order completion" fix this? If so, which?

4. Identify the reason why I6 could not enter the write stage until the 9th cycle. Will "in-order issue/out-of-order completion" or "out-of-order issue/out-of-order completion" fix this? If so, which?