Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 – Computer Organization
TEST 2 for Spring Semester, 2001

Instructor: David Tarnoff

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes
- You may use a calculator
- **All** answers **must** be placed in blanks provided. Failure to do so will result in no credit for answer.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

"Fine print"

Academic Misconduct:

ETSU Policy No. 3.13, October 1, 1979:

"All students in attendance at East Tennessee State University are expected to be honorable."

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing or falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of "F" on the work in question, a grade of "F" for the course, reprimand, probation, suspension, and expulsion. For a second academic offense, the penalty is permanent expulsion."

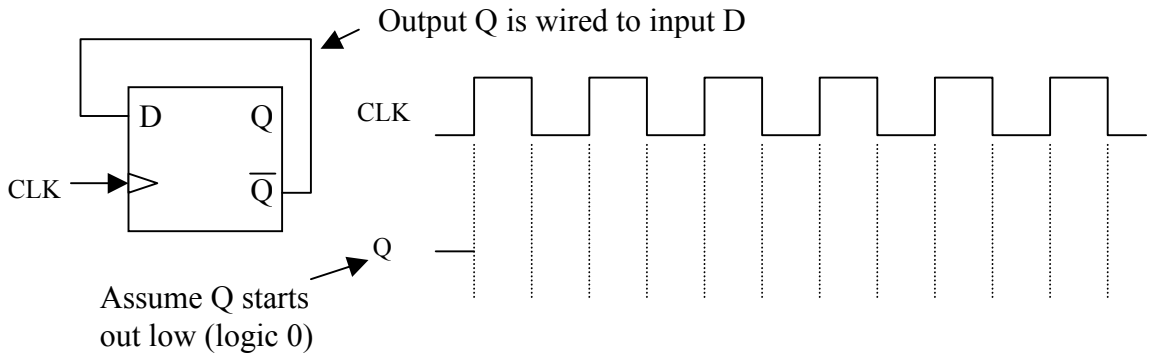
1.) Which of the following is an invalid state of an S-R flip-flop? (3 points)

a.) $\overline{S}$=0, $\overline{R}$=0 b.) $\overline{S}$=1, $\overline{R}$=0 c.) $\overline{S}$=0, $\overline{R}$=1 d.) $\overline{S}$=1, $\overline{R}$=1

2.) True or false: The D flip-flop has no invalid states. (3 points)

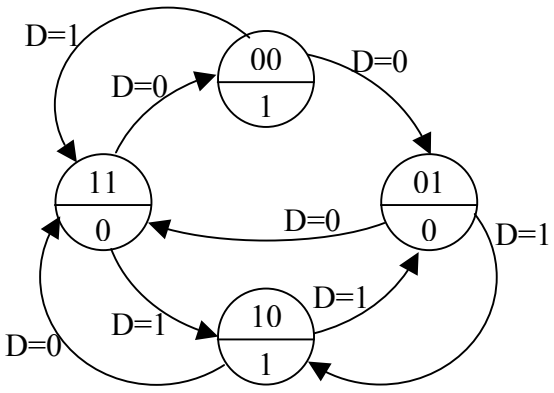
3.) If a D flip-flop has the inputs $\overline{S}$=1, $\overline{R}$=0, D=1, & CLK=0, what is the output Q? (3 points)

4.) The D flip-flop circuit below is one of the special applications we studied in class. Even if you don't remember the circuit, you should still be able to draw the output based on the system clock input. Assume flip-flop captures D on the clock's rising edge. (6 points)



5.) What is the minimum number of D flip-flops you will need to represent the states of a state diagram with 24 states? (5 points)

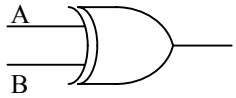
6.) Create the next state truth table and the output truth table from the state diagram below. Make sure you label the bits of your states using the state numbers from the diagram. (10 points)



7.) The three Boolean expressions below represent the next state bits (S_0' and S_1') and the output bit (X) based on the current state (S_0 and S_1). Draw the logic circuit for the state machine including the flip-flops and output circuitry. (12 points):

$$S_0' = \overline{S_0}\,\overline{S_1} + S_0 S_1 \qquad S_1' = \overline{S_0} \qquad X = S_0 + \overline{S_1}$$

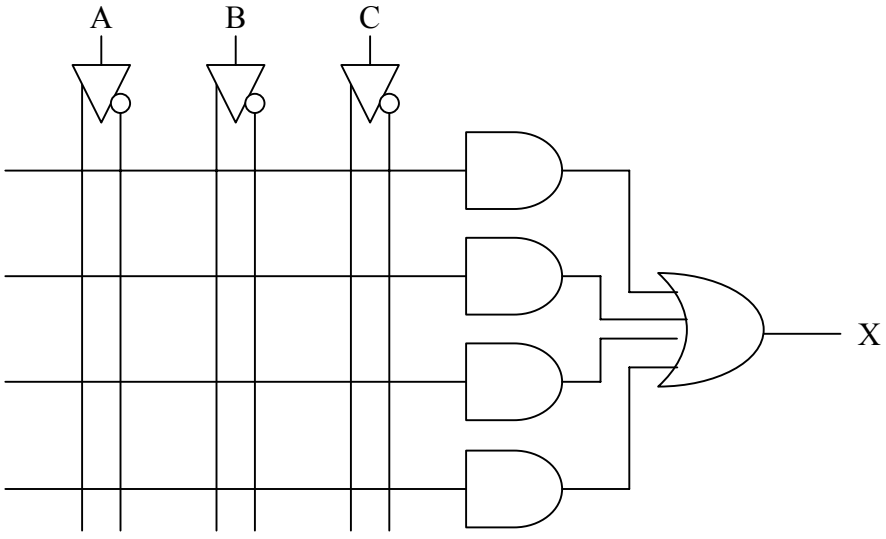
8.) Connect input A of the XOR gate shown to the right so as to invert input B at the XOR gate's output. (3 points)



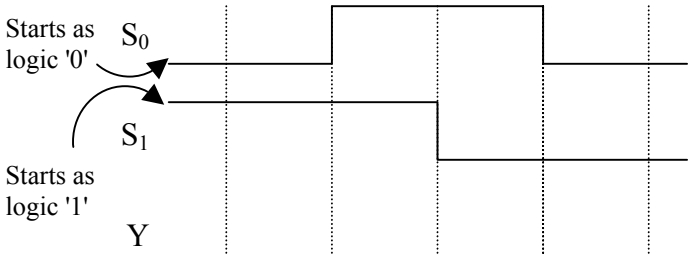
9.) A connection between a row and a column in a PAL array is made by: (3 points)

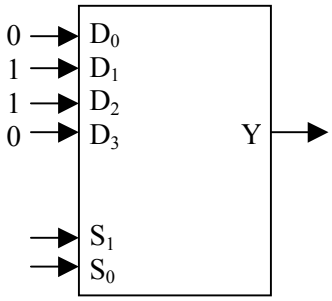
a.) Blowing a fusible link
b.) Leaving a fusible link
c.) Wiring an input variable to the input line
d.) Wiring an input variable to the product term line

10.) Using the shorthand notation, set the PAL diagram below to represent the boolean expression $X = \overline{A}\,B\,\overline{C} + \overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + C$. (5 points):



11.) For the multiplexer/selector shown to the right, sketch the output wave-form Y for the inputs S_0 and S_1 shown below? (5 points)





12.) The bit capacity (i.e., the total number of flip-flops) in a RAM with 12 address lines and 8 bits stored at each address is: (4 points)

a.) 32,768 b.) 65,536 c.) 4,096 d.) 256

13.) Of the bus control lines, the write line goes low when: (3 points)

a.) Data is passing from memory to processor
b.) The bus is idle
c.) Data is passing from processor to memory
d.) Cannot tell without read line value

14.) Circle ***all*** that apply. A storage cell in a DRAM: (4 points)

a.) is volatile
b.) is a capacitor
c.) needs to be refreshed regularly
d.) is smaller than a cell in an SRAM

15.) Circle ***all*** the memory types below that are non-volatile. (6 points)

a.) SRAM b.) Flash RAM c.) Custom-masked ROM
d.) EEPROM e.) OTPROM f.) DRAM

16.) Circle ***all*** the memory types below that can be written to multiple times. (6 points)

a.) Battery-backed SRAM b.) Flash RAM c.) Custom-masked ROM
d.) EEPROM e.) OTPROM f.) EPROM

17.) True or False: One memory block can have a low address of 3400_{16} and a high address of $3FFF_{16}$? (5 points)

18.) What is the high address **IN HEX** for a 1K ROM with a low address of 3800_{16}? (6 points)

19.) Design the chip select (w/logic gates) for a 16K RAM placed in a 1MEG memory space with a low address of 58000_{16}. ***Label all address lines used for chip select.*** (8 points)