Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 3 for Fall Semester, 2005

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving an answer as a numeric expression is acceptable.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, October 21, 2005:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

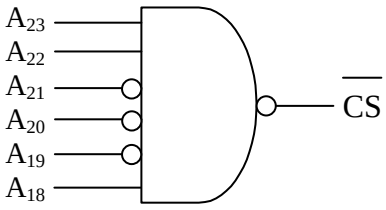
1. Match each of the settings of the bus control signals $\overline{R}$ and $\overline{W}$ on the left with the bus operation on the right. (3 points)

$\overline{R}$	$\overline{W}$			Operation of the bus
0	0	☐	☐	Processor reads from memory
0	1	☐	☐	Processor writes to memory
1	0	☐	☐	The bus is idle
1	1	☐	☐	Illegal setting

2. Circle ***all*** that apply. A storage cell in a DRAM: (4 points)

a.) is volatile
b.) is a capacitor
c.) is cheaper than cells in a SRAM
d.) is a latch
e.) must be refreshed regularly
f.) is smaller than cells in a SRAM
g.) is typically used for cache RAM
h.) is faster than an SRAM

3. What are the high and low addresses (in hexadecimal) of the memory range defined with the chip select shown to the right? (4 points)



Low address: _____ High address: _____

4. For the chip select in problem 3, how big is the memory chip that uses this chip select? (3 points)

5. For the chip select in problem 3, how big is the memory space of the processor whose address lines are used for the chip select? (3 points)

6. True or false: The address range $1AFFFF_{16}$ to $1AC000_{16}$ is a valid range for a single memory. (2 points)

7. The NAND gate is used for chip selects because of its operation (it has exactly one combination of inputs that result in a low output) and its speed. What other logic gate might also work for a chip select when speed is not a factor? (2 points)

8. Using logic gates, design an active low chip select for a RAM placed in a 16 Meg memory space with a low address of $5C0000_{16}$ and a high address of $5DFFFF_{16}$. ***Label all address lines used for chip select.*** (5 points)

9. For each of the four following groups of information, put a check mark next to the ones for which there is enough information to correctly make the chip select logic for a memory device. (4 points)

   ☐ The high and low addresses for the memory device's address range.
   ☐ The starting (low) address and the size of the memory device.
   ☐ The starting (low) address and the size of the processor's address space.
   ☐ The number of address lines going to the memory device, the number of address lines coming from the processor, and ***any*** valid address for that memory device.

10. What characteristic of storage devices ***improves*** as you move ***up*** through the memory hierarchy towards the processor? (2 points)

11. True or false: ***Multiple zone recording*** hard drives have more complex controllers than ***constant angular velocity*** hard drives. (2 points)

12. True or false: ***Multiple zone recording*** hard drives have better data density than ***constant angular velocity*** hard drives. (2 points)

13. By using different encoding methods, hard drive designers are able to increase _____ without changing the physical technology of the drive. (2 points)

    a.) reliability b.) data density c.) error detection d.) throughput (speed data is retrieved)
    e.) A and C b.) B and D c.) A, B, C, and D d.) none of the above

14. The number of sectors per track on a multiple zone recording hard drive _____ as you go closer to the outside edge of the disk. (2 points)

    a.) increases b.) decreases c.) stays the same

15. Describe how the LFU replacement algorithm for the fully associative mapping algorithm works. (3 points)

The table below represents a small section of a cache that uses fully associative mapping. Refer to it to answer questions 16 through 20.

Tags (binary)	Word within the block															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
110010110110	00_{16}	61_{16}	$C2_{16}$	13_{16}	84_{16}	$E5_{16}$	46_{16}	$A7_{16}$	12_{16}	34_{16}	56_{16}	78_{16}	$9A_{16}$	BC_{16}	DE_{16}	$F0_{16}$
010101011100	60_{16}	71_{16}	$D2_{16}$	33_{16}	94_{16}	$F5_{16}$	36_{16}	$B7_{16}$	23_{16}	45_{16}	67_{16}	89_{16}	AB_{16}	CD_{16}	EF_{16}	01_{16}
010111001011	20_{16}	81_{16}	$E2_{16}$	83_{16}	$A4_{16}$	05_{16}	66_{16}	$C7_{16}$	88_{16}	99_{16}	AA_{16}	BB_{16}	CC_{16}	DD_{16}	EE_{16}	FF_{16}
110010100110	30_{16}	91_{16}	$F2_{16}$	53_{16}	$B4_{16}$	15_{16}	$A6_{16}$	$D7_{16}$	FE_{16}	DC_{16}	BA_{16}	98_{16}	76_{16}	54_{16}	32_{16}	10_{16}
011011011001	40_{16}	**$A1_{16}$**	02_{16}	63_{16}	$C4_{16}$	25_{16}	86_{16}	$E7_{16}$	ED_{16}	CB_{16}	$A9_{16}$	87_{16}	65_{16}	43_{16}	21_{16}	$0F_{16}$
110010100101	50_{16}	$B1_{16}$	22_{16}	73_{16}	$D4_{16}$	35_{16}	96_{16}	$F7_{16}$	11_{16}	44_{16}	55_{16}	77_{16}	$0F_{16}$	$1F_{16}$	$2F_{16}$	$3F_{16}$

16. Assuming the tags shown above do ***not*** delete leading zeros, how many address lines does the processor that uses this cache have? (2 points)

17. What is the block size (in number of memory locations) for the cache shown above? (2 points)

18. From what address in main memory did the value $A1_{16}$ (the value in bold) come from? Leave your answer in binary. (3 points)

19. A copy of the data from memory address $CA5B_{16}$ is contained in the portion of the cache shown above. What is the value stored at that address? (2 points)

20. If the block containing memory address 4648_{16} were to be loaded into the cache described above, what would the tag be? (2 points)

21. True or false: The method used to make a chip select for a memory device is the same as that used to identify a subnet ID in a TCP/IP network or to identify a block ID in a memory space. (2 points)

22. Assume a processor takes 3 cycles to execute any instruction (fetch, decode, execute)

a. How many cycles would a ***non-pipelined*** processor take to execute 7 instructions? (2 points)

b. How many cycles would a ***pipelined*** processor take to execute 7 instructions? (2 points)

23. What are the settings of the zero flag, the sign flag, the carry flag, and the overflow flag after a processor performs the addition shown to the right? (4 points)

```
1 111 1
  01010101
+ 10110110
  00001011
```

ZF = _____ SF = _____ CF = _____ OF = _____

24. What mathematical operation does a processor use to compare two values to see if they are equal or to see if one is greater than the other? (2 points)

Answer: _____

25. What is the purpose of the ALU? (2 points)

26. Name the two benefits of the segment/pointer addressing system of the 80x86. (3 points)

27. Assume AX=1000_{16}, BX=2000_{16}, and CX=3000_{16}. After the following code is executed, what would AX, BX, and CX contain? (3 points)

```
PUSH AX
PUSH BX
PUSH CX
POP BX
POP CX
POP AX
```

Place your answers in space below:

AX =

BX =

CX =

28. What is the physical address pointed to by the 80x86 segment/pointer pair 3200:1234? Note that the values given are in hexadecimal. (2 points)

29. Which 80x86 segment/pointer register pair points to the next instruction to be executed by the processor? (2 points)

a.) es:sp b.) es:di c.) ss:bp d.) ds:si e.) cs:ip f.) ds:ip g.) cs:di h.) ss:sp

30. Which 80x86 segment/pointer register pair points to where the arguments for a function or procedure are stored on the stack? (2 points)

a.) es:sp b.) es:di c.) ss:bp d.) ds:si e.) cs:ip f.) ds:ip g.) cs:di h.) ss:sp

31. Using an original value of 10011001_2 and a mask of 00001111_2, calculate the results of a bitwise AND, a bitwise OR, and a bitwise XOR for these values. (2 points each)

Original value	Bitwise operation	Mask	Result
10011001_2	AND	00001111_2	
10011001_2	OR	00001111_2	
10011001_2	XOR	00001111_2	

32. If the datasum calculated from a sequence of values is a hexadecimal $5A_{16}$, what would the hexadecimal value of the 1's complement checksum be? (2 points)

33. Describe the primary drawback discussed in class of a datasum-based checksum. (2 points)

34. Describe one of the two reasons discussed in class for using an XOR "borrow-less" subtraction in the calculation of a CRC. (2 points)

35. True or false: When using a CRC for error checking, both the transmitting device and the receiving device must use the same polynomial (divisor) for calculation of the CRC. (2 points)

36. For each of the following statements, identify whether it describes an Ethernet frame (E), an IP packet (I), or a TCP packet (T) by placing the corresponding letter (E, I, or T) in the space provided. (6 points)

_____ This protocol is used to get a message from one host to another across multiple interconnected networks.

_____ This protocol uses a preamble of alternating 1’s and 0’s to synchronize all receivers.

_____ This protocol uses a CRC instead of a datasum-based checksum.

_____ This protocol includes a “time to live” field so that it can be removed from the network(s) in case it cannot find its destination.

_____ Uses a logical address defined by a network administrator for its addressing.

_____ Uses a physical address on the network interface hardware for its addressing.