Points missed: _____ Student's Name: _________________________________

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Fall Semester, 2003

Section 001

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. True or False: If done properly, there is exactly one possible arrangement for the rectangles of ones in a Karnaugh map. (2 points)

   The answer is FALSE. To show this, look at the following example (note the red rectangle):

2. In a 4-variable Karnaugh map, how many variables (e.g., A, B, C, etc.) does a product have if its rectangle of 1's contains 8 cells? (2 points)

   Remember that each time the size of a rectangle is doubled (e.g., 1 cell doubled to 2 cells, 2 cells doubled to 4 cells, etc.) a single input variable drops out. In addition, a rectangle of size 1 uses all of the input variables. Therefore, since a rectangle of 8 cells has doubled three times over the size of a single cell rectangle, there are 3 variables that have dropped out. ***Therefore, a product from a rectangle of eight cells in a 4-variable K-map has 1 variables.*** (You could also show this by creating an example.)

3. True or False: In order to keep a Karnaugh map in 2-dimensions, i.e., so that it can be written on a piece of paper, we are limited to 4 input variables. (2 points)

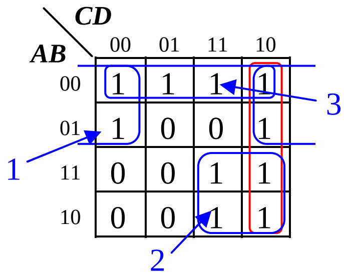
   The answer is TRUE. It is impossible to label 8 rows with three binary variables so that only one binary variable changes between adjacent rows.

4. Create a Karnaugh map from the truth table below. Do not worry about making the rectangles. (5 points)

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

AB \ C	0	1
00	0	1
01	1	1
11	0	0
10	1	0

5. Derive the minimum SOP expression from the Karnaugh map below. (6 points)



Rectangle 1

A	B	C	D
0	0	0	0
0	1	0	0
0	0	1	0
0	1	1	0

B and C drop out and A and D are inverted.

$\overline{A}\cdot\overline{D}$

Rectangle 2

A	B	C	D
1	1	1	1
1	0	1	1
1	1	1	0
1	0	1	0

B and D drop out and A and C are not inverted.

$A\cdot C$

Rectangle 3

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0

C and D drop out and A and B are inverted.

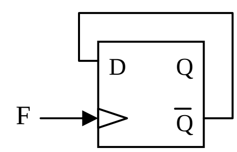
$\overline{A}\cdot\overline{B}$

Note that the red rectangle is a duplicate of the others and should be removed.

The final answer is:

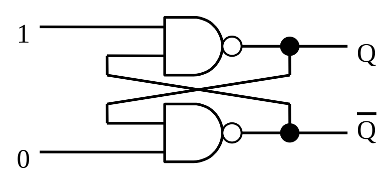
$\overline{A}\cdot\overline{D} + A\cdot C + \overline{A}\cdot\overline{B}$

6. The circuit shown to the right was discussed in class and had a special application for digital circuits. What was that application? Hint: F is a periodic clock signal. (2 points)



The circuit was called a divide by two circuit and the output of Q was a periodic clock signal that had a frequency half that of F.

7. For the circuit to the right, what value does Q have? (2 points)



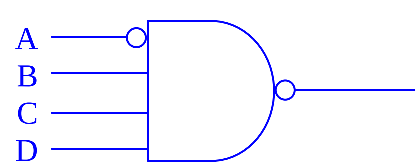
a.) 0 c.) Must know previous value for Q to answer.
b.) 1 d.) Illegal state. Should never have these inputs.

The answer is A. If you recall from our introduction to latches, this is the S-R latch with the top input being ^S and the lower input being ^R. When ^R is low and ^S is high, the latch is in its RESET state where the Q output is reset to zero.

8. True or False: For the circuit in the previous problem, if the inputs changed from 1-0 (the values shown) to 1-1, the value of Q would remain unchanged. (2 points)

The answer is TRUE. Once again, from our discussion on the S-R latch, when both ^S and ^R go to 1, the previous values of Q and ^Q remain unchanged.

9. In the space to the right, draw the ***decoding logic circuit*** with an ***active-low output*** for the inputs A = 0, B = 1, C = 1, and D = 1. (5 points)

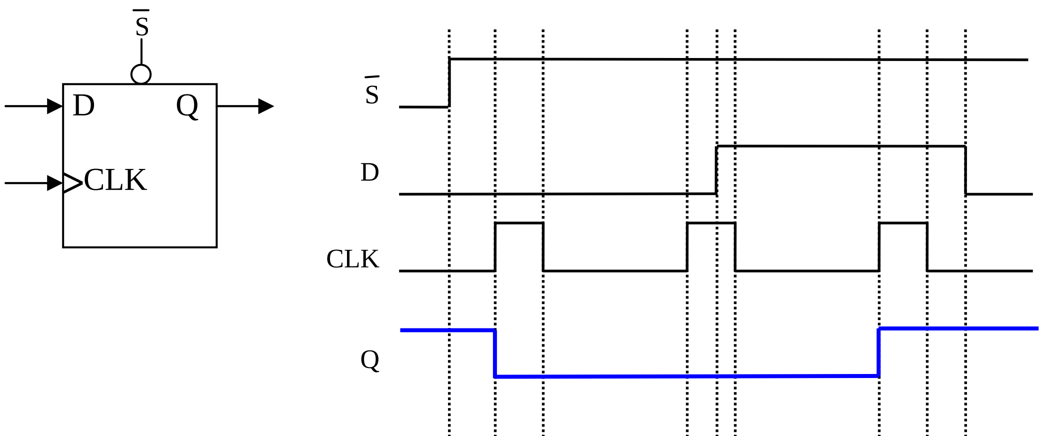


10. In a truth table, the symbol ↑ indicates that the input is: (2 points)

a.) a logic 0
b.) a logic 1
c.) changing from a 1 to a 0
d.) changing from a 0 to a 1
e.) this is an output symbol, not an input
f.) a "don't care"

The up arrow indicates a rising edge, i.e., a transition from a 0 to a 1. Therefore, the answer is D.

11. Show the D flip-flop output waveform Q based on the inputs D and CLK indicated in the figure below. Assume the flip-flop captures on the rising edge. (6 points)



Note that the ^S input starting off as a 0 forces the Q output to be a 1. Also note that once ^S goes to 1, the output Q can only change when there is a 0 to 1 transition on the clock, CLK.

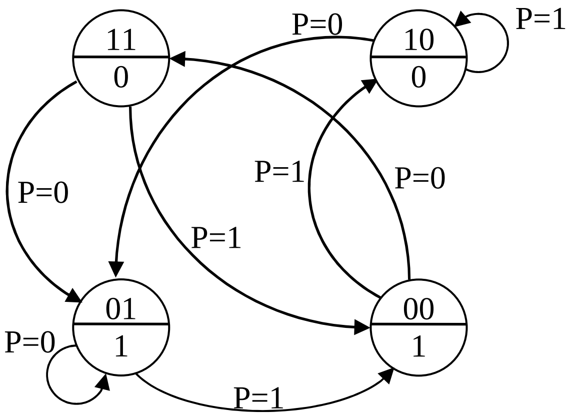
12. What does the term ***active low*** mean? (3 points)

The term describes a circuit where the active state occurs when a 0 is placed on the input or output described as active low. The circuit is idle when a 1 is placed on the input or output.

13. How many latches or flip-flops are needed to realize a state machine with 34 states? (3 points)

A state machine with 34 states requires numbers from 0 to 33_{10} to uniquely number each state. (Remember to begin numbering at 0!) Since 33_{10} is the largest number we need to represent, then it's going to require the most digits to be stored by the latches. Since $33_{10} = 100001_2$, then 6 digits are needed and therefore, 6 latches are needed. Another way of looking at the problem is that 33 is greater than 31, the largest number representable with 5 digits, but less than 63, the largest number representable with 6 digits. Therefore, 6 latches will be needed.

14. Create the next state truth table and the output truth table for the state diagram below. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. (8 points)



Next State T.T.

S_1	S_0	P	S_1'	S_0'
0	0	0	1	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	0

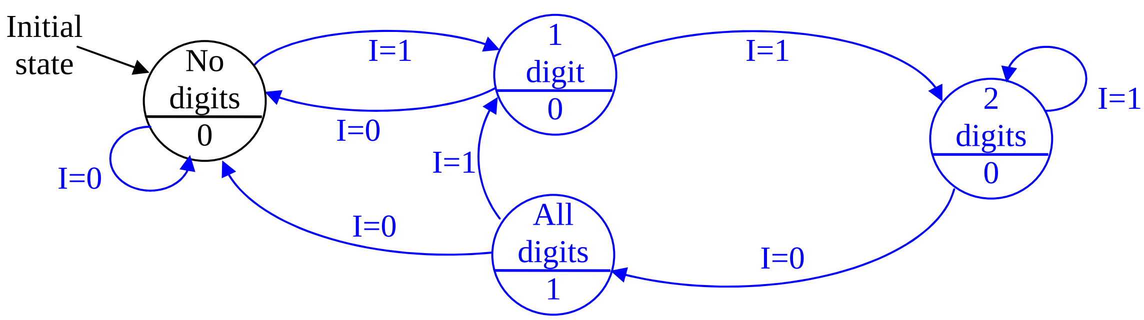
Output T.T.

S_1	S_0	X
0	0	1
0	1	1
1	0	0
1	1	0

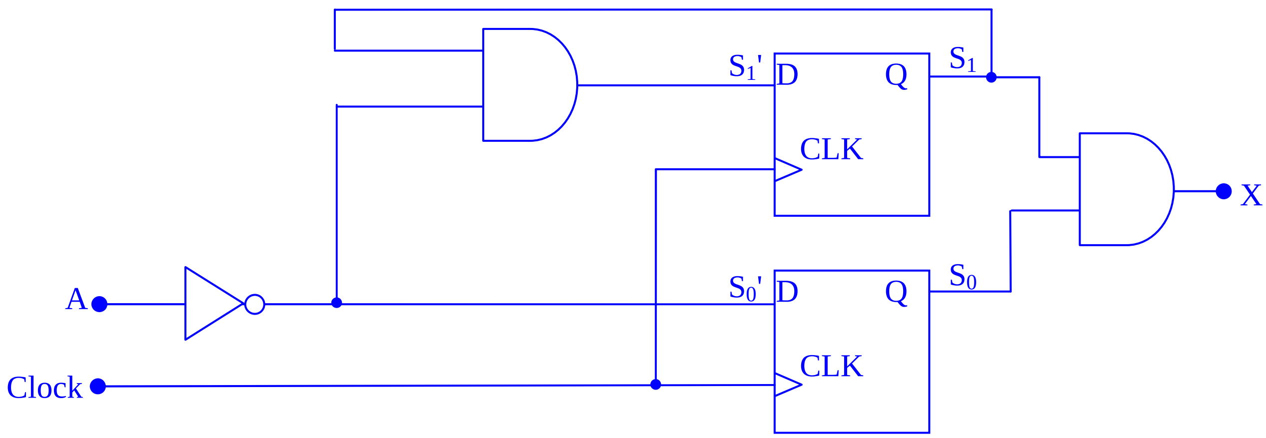
15. Make the state diagram that will output a '1' when the sequence '110' is detected in a serial stream of bits, D. For example, if the following binary stream is received:

0 0 1 0 1 1 1 1 0 0 1 1 0 0 0 0 1 1 1 1 1 1 0 1 0 0 1

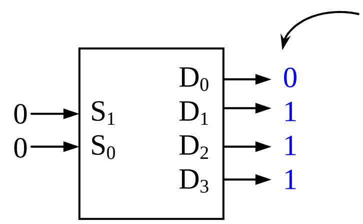
then 1's will be output here. Otherwise, the system will output zeros. (7 points)



16. The three Boolean expressions below represent the ***next state bits (S_0' and S_1')*** and the ***output bit X*** based on the ***current state (S_0 and S_1)*** and the ***input A***. Draw the logic circuit for the state machine including the flip-flops and output circuitry. Be sure to label flip-flop inputs and other signals.
(8 points) $S_0' = \overline{A}$ $S_1' = S_1\overline{A}$ $X = S_0S_1$



17. For the ***active-low*** output decoder shown to the right, fill in the values for all of the outputs D_0 through D_3. Assume S_1 is most significant bit. (3 points)



Fill in the ones and zeros for each of these outputs.

18. How many D latches or flip-flops are contained in a RAM memory that has 20 address lines and 8 data lines? (Don't do the calculation; only write the equation with the correct values.) (3 points)

First, there are 2^{20} memory locations, one for each unique combination of 1's and 0's for the address lines. Each memory location contains 8 latches, and therefore, the number of latches is equal to:

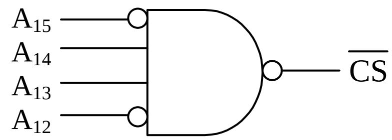
$$2^{20} * 8 = 8 \text{ Meg}$$

19. Select the invalid setting (if any) of the memory bus signals $\overline{R}$ and $\overline{W}$? (2 points)

a.) $\overline{R} = 0, \overline{W} = 0$ b.) $\overline{R} = 0, \overline{W} = 1$ c.) $\overline{R} = 1, \overline{W} = 0$ d.) $\overline{R} = 1, \overline{W} = 1$ e.) None

Since the active low signals ^R and ^W control whether the system is reading or writing to a memory location, the case where they are attempting to both read and write at the same time is invalid. ***Therefore, the answer is A.***

20. What are the high and low addresses (in hexadecimal) of the memory range defined with the chip select shown to the right? (6 points)



The chip select is active when $A_{15} = 0$, $A_{14} = 1$, $A_{13} = 1$, and $A_{12} = 0$. The low address occurs when A_0 through A_{11} are all equal to 0 and the high address occurs when A_0 through A_{11} are all equal to 1.

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Low address =	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
High address =	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1

Low address: **6000_{16}** High address: **$6FFF_{16}$**

21. For the chip select in problem 20, how big is the memory space for this processor? (3 points)

The processor has a total of 16 address lines (A_0 through A_{15}). Therefore, its memory space is capable of addressing $2^{16} = 2^6 * 2^{10} = 64K$.

22. For the chip select in problem 20, how big is the memory chip that uses this chip select? (3 points)

Twelve address lines (A_0 through A_{11}) go to the memory chip. Therefore, the memory chip has $2^{12} = 2^2 * 2^{10} = 4K$ memory locations.

23. What is the largest memory that can have a starting (lowest) address of 16000_{16}? (3 points)

Remember that the lowest address must have all zeros going to the address lines of the memory chip. Therefore, if we can determine the number of bits equal to zero starting with the least significant, A_0, and going left, then we know how many address lines can be used for the memory chip. Begin by converting 16000_{16} to binary.

$$16000_{16} = 0\,0\,0\,1 \quad 0\,1\,1\,0 \quad 0\,0\,0\,0 \quad 0\,0\,0\,0 \quad 0\,0\,0\,0$$

There are thirteen zeros before you get to the first 1 in the binary value of 16000_{16}. Therefore, thirteen address lines can go to the memory chip. The answer, therefore, is $2^{13} = 2^3 * 2^{10} = 8K$.

24. How many 16K memories can be placed (without overlapping) in the memory space of a processor that has 24 address lines? (3 points)

Since $16K = 2^4 * 2^{10} = 2^{14}$, then a 16K memory chip has 14 address lines. When connected to a processor with 24 address lines, 24-14 = 10 address lines are left for chip selects. Therefore, there are $2^{10} = 1024$ (1K) possible combinations of 1's and 0's for the chip selects which means that 1024 16K memories can be placed in the memory space of a processor with 24 address lines.

25. True or false: A 16K memory and a 4 Meg memory can be connected at the same time to the same address bus of a processor with a memory space of 16 Meg. (2 points)

TRUE: Different size memories can be connected to a single processor as long as a unique range of memory addresses can be found for each.

26. Using logic gates, design an active low chip select for a RAM placed in a 4 Meg memory space with a low address of 30000_{16} and a high address of $37FFF_{16}$. ***Label all address lines used for chip select.*** (7 points)

Begin by converting 30000_{16} and $37FFF_{16}$ to binary. ***Remember that a processor with a 4 Meg memory space requires 22 address lines (4 Meg = $2^2 * 2^{20} = 2^{24}$), so be sure to convert to binary values with 22 digits.***

30000_{16} = 00 0011 0000 0000 0000 0000_2
$37FFF_{16}$ = 00 0011 0111 1111 1111 1111_2

	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	…	A_5	A_4	A_3	A_2	A_1	A_0
Low address =	0	0	0	0	1	1	0	0	0	…	0	0	0	0	0	0
High address =	0	0	0	0	1	1	0	1	1	…	1	1	1	1	1	1

Note that the dividing line between the bits that remain constant and the bits that change from all ones to all zeros is between address lines A_{14} and A_{15}. Therefore, A_{15} through A_{21} will be the inputs to the chip select circuitry.

The chip select is always made from a NAND gate with the inputs that are meant to be zeros going through inverters. The result is shown in the answer below.