Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Fall Semester, 2004

# Section 001

**Read this before starting!**

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

| Binary | Hex |
|---|---|
| 0000 | 0 |
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 7 |

| Binary | Hex |
|---|---|
| 1000 | 8 |
| 1001 | 9 |
| 1010 | A |
| 1011 | B |
| 1100 | C |
| 1101 | D |
| 1110 | E |
| 1111 | F |

| Power of 2 | Equals |
|---|---|
| $2^3$ | 8 |
| $2^4$ | 16 |
| $2^5$ | 32 |
| $2^6$ | 64 |
| $2^7$ | 128 |
| $2^8$ | 256 |
| $2^9$ | 512 |
| $2^{10}$ | 1K |
| $2^{20}$ | 1M |
| $2^{30}$ | 1G |

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

***Short answers – 2 points each (unless otherwise noted)***

1. True or False: The expression (A+B+C)·(B+C)·(A+D) is in proper Product-of-Sums format.

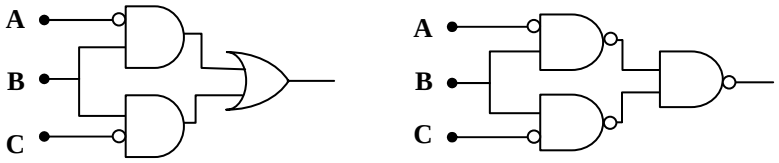
   TRUE: This expression can be realized with two layers of logic, a set of OR gates feeding into a single AND gate.

2. The expression $\overline{A}\cdot B\cdot C + A\cdot B\cdot C + \overline{A\cdot B}$ is not in proper Sum-of_Products format. What boolean algebra operation would you need to apply to correct this?

   a.) It's not a problem; illegal term drops out  b.) Distributive Law  c.) Use "F-O-I-L"
   d.) Take the inverse of the inverse  e.) DeMorgan's Theorem  f.) It can't be fixed

   e.) The inverse over the last product, A·B, needs to be distributed to the individual terms. This means using DeMorgan's Theorem.

3. True or False: The two circuits below are equal.




   TRUE: Since an OR gate is equivalent to a NAND gate with inverted inputs, then all of the gates of an SOP circuit can be replaced with NAND gates.

4. If a Sum-of-Products expression uses four input variables, and there is a product within the SOP expression that uses only three of the four variables, how many rows in the SOP expression's truth table have ones as a result of that particular product?

   a.) 1  b.) 2  c.) 3  d.) 4  e.) 6

   b.) A product that uses all of the variables of the expression turns exactly one row of the truth table to a one. For every variable removed from that product, the number of rows in the truth table with one's output as a result of that product is doubled. Therefore, with only 3 of the 4 variables in the product, exactly two rows will have ones in them. For example, in an expression using A, B, C, and D, the product A·C·D will have ones in the truth table for rows A=1, B=0, C=1, and D=1 and A=1, B=1, C=1, and D=1.

5. Complete the truth table to the right with the values for the following Sum-of-Products expression: (3 points)

$$X = (\overline{A}\cdot B\cdot\overline{C}) + (\overline{A}\cdot\overline{B}\cdot C) + (A\cdot B)$$

   $\overline{A}\cdot B\cdot\overline{C}$: A = 0, B = 1, C = 0
   $\overline{A}\cdot\overline{B}\cdot C$: A = 0, B = 0, C = 1
   $A\cdot B$: A = 1, B = 1, C = 0 or 1

| A | B | C | X |
|---|---|---|---|
| 0 | 0 | 0 | **0** |
| 0 | 0 | 1 | **1** |
| 0 | 1 | 0 | **1** |
| 0 | 1 | 1 | **0** |
| 1 | 0 | 0 | **0** |
| 1 | 0 | 1 | **0** |
| 1 | 1 | 0 | **1** |
| 1 | 1 | 1 | **1** |

6. Why do we limit ourselves to 4-input Karnaugh maps? (3 points)

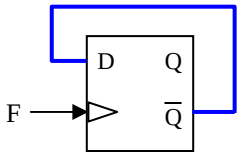
   Because a 5-input K-map would require a three dimensional grid of cells.

7. In a 4-variable Karnaugh map, how many input variables, A, B, C, or D, does a product have if its rectangle of 1's contains 2 cells? For example, the product A·D contains 2 input variables.

   a.) 0 b.) 1 c.) 2 d.) 3 e.) 4

   d.) As stated in problem 4, every time a variable is removed from the product, the number of rows in the truth table resulting in ones is doubled. This works backwards too. In the Karnaugh map, every time the number of cells in a rectangle doubles, one variable drops out. Therefore, for a rectangle of size 2, we have doubled only once so only one variable has dropped out. This leaves 3 variables.

8. Make the connections to the latch in the figure to the right that makes a divide-by-two circuit.




9. How many cells total does a 3 variable Karnaugh map have?

   A 3-variable Karnaugh map has one cell for every possible pattern of ones and zeros for the 3 variables. Therefore, the answer is $2^3 = 8$.

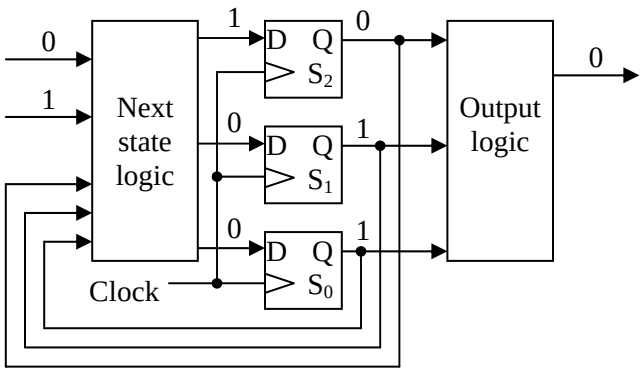
10. True or False: If done properly, there is exactly one possible arrangement for the rectangles of ones in a Karnaugh map.

    The answer is FALSE. To show this, look at the following example (note the red rectangle):

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 0 | 1 | 0 |
| 11 | 0 | 0 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 |

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 0 | 1 | 0 |
| 11 | 0 | 0 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 |

Problems 11, 12, and 13 use the state machine diagram to the right. Assume the state bits use $S_2$ as MSB and $S_0$ as LSB.




11. What is the maximum number of states this system could have?

    The three latches represent the states, and since three latches can have $2^3 = 8$ possible values, then this system can have 8 possible states.

12. What is the current state of this system? Keep your answer in binary.

    The current state is represented with the output of the latches which is 0 – 1 – 1.

13. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

The next state is represented with the input to the latches which is 1 – 0 – 0.

14. In a truth table, the symbol ↑ indicates that the input is:

a.) a logic 0 c.) changing from a 1 to a 0 e.) this is an output symbol, not an input
b.) a logic 1 d.) changing from a 0 to a 1 f.) a "don't care"

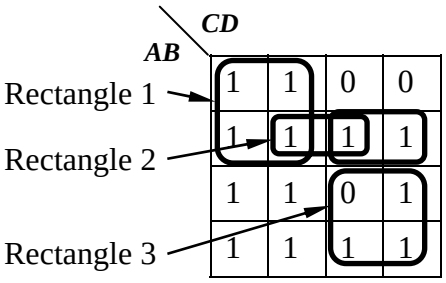
The up arrow represents a transition from a 0 to a 1. Therefore, the answer is d.

15. How many latches will a state machine with 28 states require?

a.) 1 b.) 2 c.) 3 d.) 4 e.) 5 f.) 6 g.) 7

Twenty-eight states will be numbered 0, 1, 2, 3, 4, 5, … , 25, 26, and 27. Since $27_{10} = 11011_2$, we will need at least 5 bits to represent the state. Therefore, the answer is e.

16. For the Karnaugh map to the right, identify the problems with each of the three rectangles shown. (2 points each)




Rectangle 1: The rectangle is too small. It can double in size by including the four cells beneath it.

Rectangle 2: Completely overlapped by other rectangles. It is unnecessary.

Rectangle 3: Contains a zero.

17. If a group of four rows or columns in a Karnaugh map is identified with two variables, it is numbered 00, 01, 11, 10 instead of 00, 01, 10, 11. Why? (3 points)

Because any horizontal or vertical movement between adjacent cells can only have 1 input variable change. Numbering 00, 01, 10, 11 has two variables changing when going from 01 to 10 and when wrapping around the table from 00 to 11.

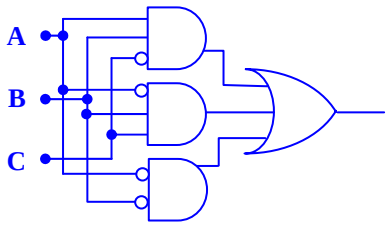
18. List one of the reasons discussed in class why the NAND-NAND implementation of an SOP expression is preferred over an AND-OR implementation. (3 points)

NAND gate logic is typically the fastest.
One type of gate used in a logic circuit is more efficient design and manufacturing wise.

***Medium answers – points vary***

19. Draw the digital circuit corresponding to the following SOP expression. (4 points)

$$X = (A \cdot B \cdot \overline{C}) + (\overline{A} \cdot B \cdot C) + (\overline{A} \cdot \overline{B})$$




20. Create a Karnaugh map from the truth table below. ***Do not worry about making the rectangles.*** (5 points)

| A | B | C | X |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

| AB \ C | 0 | 1 |
|---|---|---|
| 00 | 1 | 0 |
| 01 | 1 | 1 |
| 11 | 1 | 1 |
| 10 | 0 | 1 |

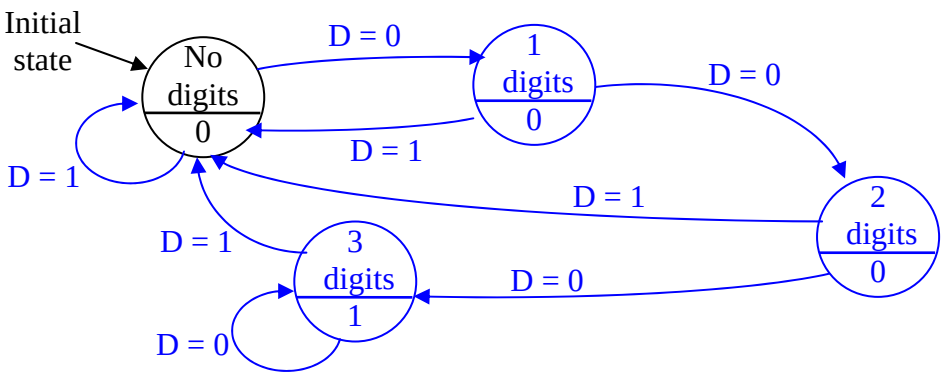
21. In the Karnaugh map to the right, draw the best pattern of rectangles you can. ***Do not derive the SOP expression.*** (4 points)

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | X | 1 |
| 01 | 0 | 0 | X | 1 |
| 11 | 0 | 0 | X | 0 |
| 10 | 0 | 0 | X | X |

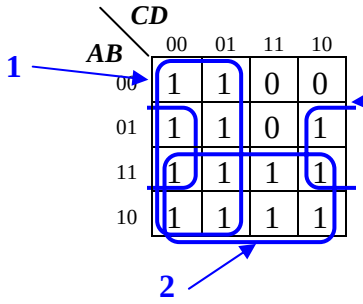
22. Make the state diagram that will output a '1' when the sequence '000' is detected in a serial stream of bits, D. For example, if the following binary stream is received:

0 0 1 0 1 0 0 0 0 1 0 0 0 1 0 0 1 1 1 1 0 0 0 1 0 0 1

then 1's will be output here. Otherwise, the system will output zeros. (7 points)



23. Derive the minimum SOP expression from the Karnaugh map below. (6 points)




Rectangle 1

| A | B | C | D |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |

A, B and D drop out and C, since it is equal to 0, is inverted.

$\overline{C}$

Rectangle 2

| A | B | C | D |
|---|---|---|---|
| 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 |

B, C, and D drop out and A, since it is equal to 1, is not inverted.

A

Rectangle 3

| A | B | C | D |
|---|---|---|---|
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

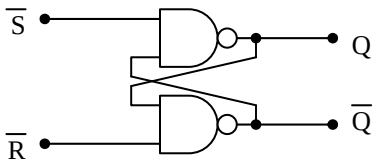
A and C drop out . B is not inverted and D is inverted.

$B \cdot \overline{D}$

The final answer is:

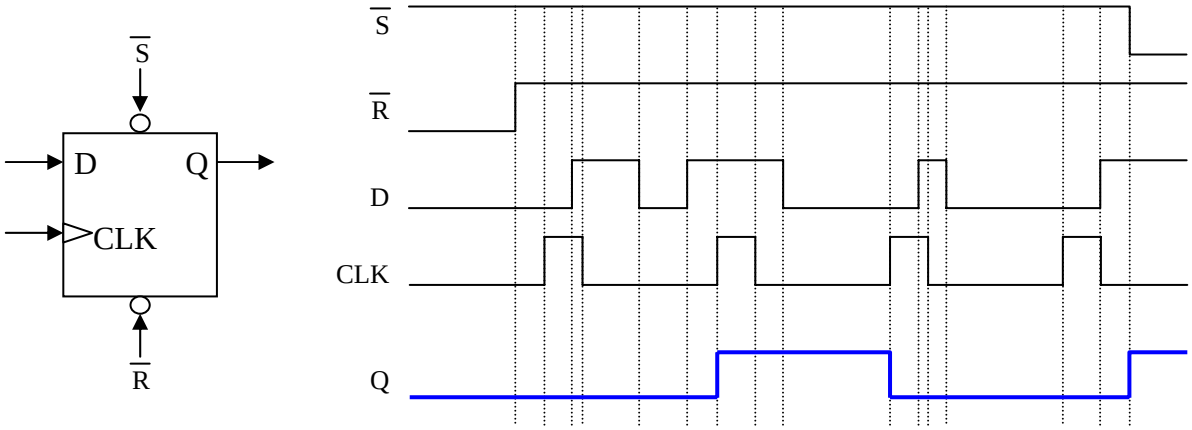
$\overline{C} + A + B \cdot \overline{D}$

24. Fill out the truth table to the right for all possible combinations of inputs for the circuit below. (5 points)



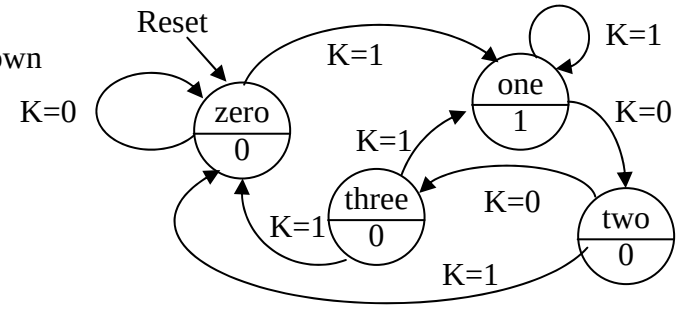

| $\overline{S}$ | $\overline{R}$ | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | U | U |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | $Q_0$ | $\overline{Q_0}$ |

25. Show the D latch output waveform Q based on the inputs D, ^S, ^R, and CLK indicated in the figure below. Assume the latch captures on the rising edge. (6 points)

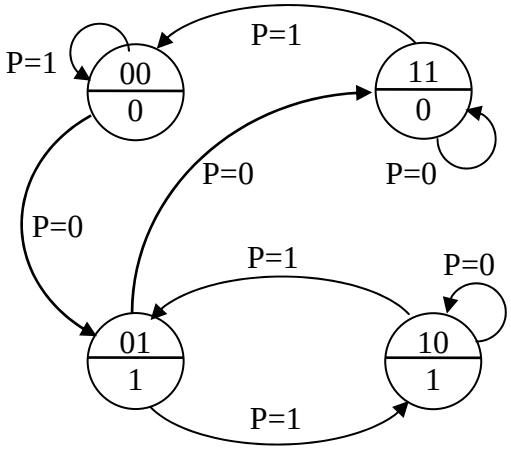


26. Identify the error in the state diagram shown to the right. (3 points)

State 3 has 2 K=1 transitions and no K=0 transitions.




27. Create the next state truth table and the output truth table for the state diagram below. Use the variable names $S_1$ and $S_0$ to represent the most significant and least significant bits respectively of the binary number identifying the state. (8 points)




Next State T.T.

| $S_1$ | $S_0$ | P | $S_1'$ | $S_0'$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |

Output T.T.

| $S_1$ | $S_0$ | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

28. The three Boolean expressions below represent the ***next state bits ($S_0'$ and $S_1'$)*** and the ***output bit X*** based on the ***current state ($S_0$ and $S_1$)*** and the ***input A***. Draw the logic circuit for the state machine including the latches and output circuitry. Be sure to label the latch inputs and other signals.
(8 points) $S_0' = \overline{A} \cdot S_0 \cdot S_1$ $S_1' = \overline{A}$ $X = S_0$