

Points missed: \_\_\_\_\_ Student's Name: \_\_\_\_\_

Total score: \_\_\_\_\_/100 points

East Tennessee State University  
Department of Computer and Information Sciences  
CSCI 2150 (Tarnoff) – Computer Organization  
TEST 2 for Fall Semester, 2006

**Read this before starting!**

- The total possible score for this test is 100 points.
- This test is *closed book and closed notes*.
- *Please turn off all cell phones & pagers during the test.*
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- **Calculators are not allowed.** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
$2^3$	8
$2^4$	16
$2^5$	32
$2^6$	64
$2^7$	128
$2^8$	256
$2^9$	512
$2^{10}$	1K
$2^{20}$	1M
$2^{30}$	1G

“Fine print”

Academic Misconduct:

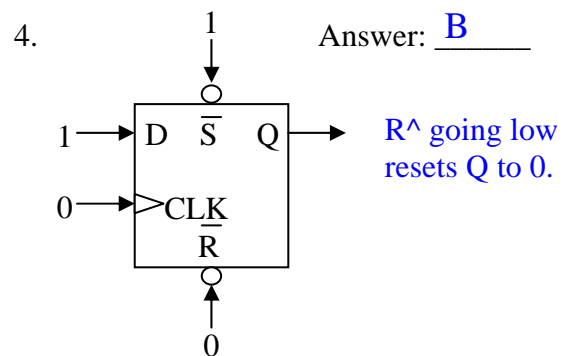
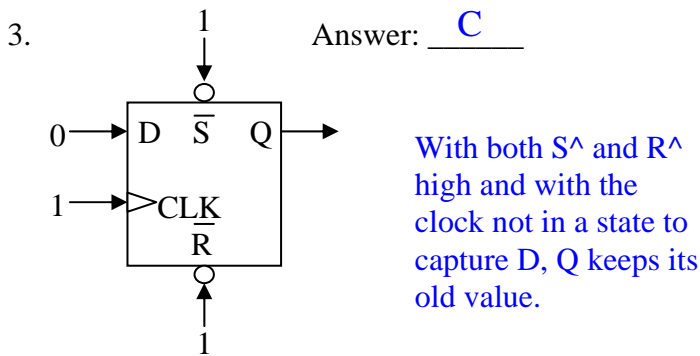
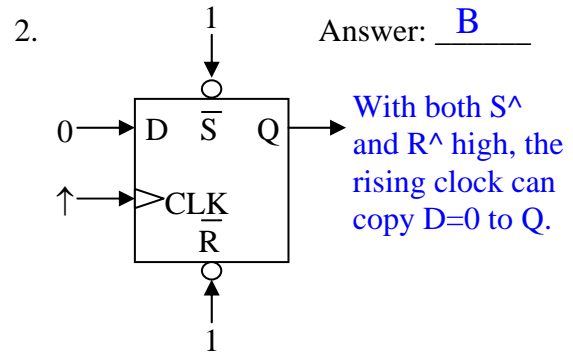
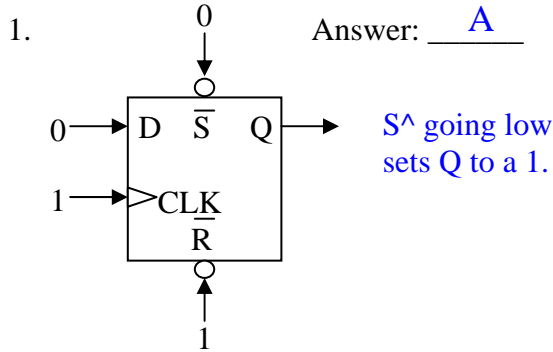
Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarizing, the changing or falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

**Short answers – 2 points each unless otherwise noted**

For the following **four** circuits, identify the value of the output Q from the following choices. Consider the D-latch a **rising edge triggered latch**.

- a.) 1      b.) 0      c.)  $Q_0$  (stored value of Q)      d.) undefined/illegal      e.) can't tell



5. The expression  $\overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C}$  is not in proper Sum-of-Products format. What boolean algebraic operation would you need to apply first to begin to correct this?

- a.) Commutative Law      b.) Associative Law      c.) Use "F-O-I-L"  
 d.) Take the inverse of the inverse      **e.) DeMorgan's Theorem**      f.) It can't be fixed

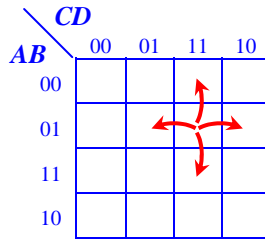
6. How many cells would a three-input Karnaugh Map have?

A three-input Karnaugh map, e.g., one with inputs A, B, and C, would have  $2^3 = 8$  possible combinations of 1's and 0's for A, B, and C giving us 8 cells.

- a.) 2      b.) 4      c.) 6      **d.) 8**      e.) 12      f.) 16      g.) 32

7. What is the largest number of input variables a Karnaugh map can handle and still remain two-dimensional?

Remember that the purpose of a Karnaugh map is to rearrange the truth table so that adjacent cells can be combined allowing for a term to drop out. In other words, the key to the effectiveness of Karnaugh maps is that each cell represents the output for a specific pattern of ones and zeros at the input, and that to move to an adjacent cell, exactly one of those inputs can change, the rest must remain the same. Take for instance the 16 cell (4-input) Karnaugh map. The cell in the third column of the second row represents the condition where  $A=0, B=1, C=1,$  and  $D=1$ . Moving to the cell immediately to the left will change only C; moving right will change D; moving up changes B; and moving down changes A. Therefore, there is an adjacent cell that represents a change in any of the four input variables.

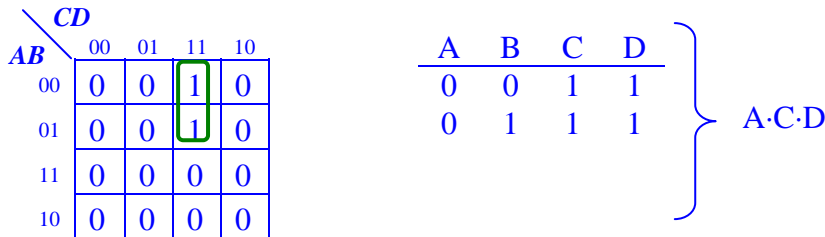


Since a square only has 4 sides, it can only represent 4 single-bit changes in the inputs. Therefore, 4 is the maximum.

- a.) 2      b.) 3      **c.) 4**      d.) 5      e.) 6      f.) 7      g.) 8

8. In a 4-variable Karnaugh map, how many input variables (A, B, C, or D) does a product have if its corresponding rectangle of 1's contains 2 cells?

The simplest way to answer this question is to create a 4-variable/input Karnaugh map that has a rectangle with two 1's, then figure out what the product is. The number of inputs in the product will give us our answer.



The resulting product has three inputs. You'll find that regardless of how the 2 cell rectangle is arranged, the resulting product will always have 3 inputs.

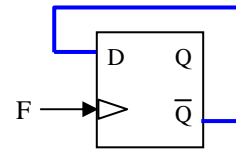
- a.) 1      b.) 2      **c.) 3**      d.) 4      e.) Cannot be determined

9. An active-high transparent latch copies data from the D input to the Q output:
- a.) as long as the clock equals a logic 0      b.) the instant the clock changes from a 1 to a 0
- c.) as long as the clock equals a logic 1**      d.) the instant the clock changes from a 0 to a 1

10. **True** or False: The  $\bar{S}$  and  $\bar{R}$  inputs of a D-latch override any input from the D and clock inputs.

The set and reset inputs always override the data and clock inputs to a latch.

11. Make the connections to the latch in the figure to the right that makes a divide-by-two circuit, i.e., divides the frequency F in half at the output Q.



12. Which of the following expressions produces the truth table to the right?

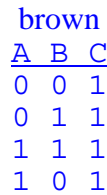
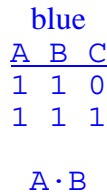
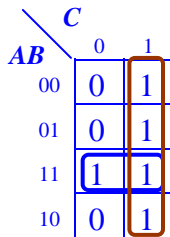
- a.)  $A \cdot \bar{B} + C$   
 d.)  $B + C$

- b.)  $A + C$   
 e.)  $A + \bar{B} \cdot C$

- c.)  $A \cdot B + C$   
 f.) None of the above

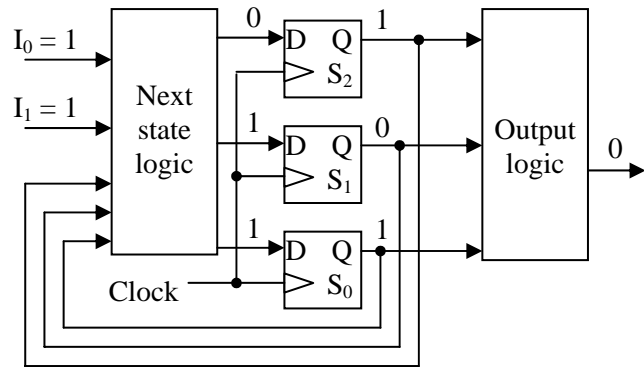
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The Spring 2006 test shows two alternate ways to do this problem, so here I will show you a third. Simply use a Karnaugh map and solve for a S.O.P. function.



Or-ing the products from these two rectangles gives us  $A \cdot B + C$ .

The next five problems use the state machine circuit to the right. Assume that the states are numbered so that bit  $S_2$  is the MSB and bit  $S_0$  is the LSB.



13. What is the maximum number of states that this system can handle?

Since there are three latches, then the internal memory of this state machine can remember  $2^3 = 8$  states: 000, 001, 010, 011, 100, 101, 110, and 111. Therefore, the answer is 8.

14. What is the current state of this system? Keep your answer in binary.

The current state is the value stored in the latches and found at the Q outputs. In the case of the diagram above, that is 1-0-1 with  $S_2$  being the most significant bit.

15. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

The next state is the value present at the D inputs, i.e., the value that would be stored if we had a clock pulse occur. In the case of the diagram above, that is 0-1-1 with  $S_2$  being the most significant bit.

$S_2$	$S_1$	$S_0$	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

16. The truth table to the right represents the output logic truth table for the above state machine. Circle the row that identifies the current output condition of the system, i.e., which row is represented by the state of the logic in the diagram above?

The output is determined by the current state, i.e., 1-0-1. Therefore, the sixth row identifies the output, which fortunately equals 0 just like the figure.

17. If the clock were to pulse right now, what would the output be? Use the truth table from the previous problem to answer the question.

- a.) 0                      **b.) 1**                      c.) Not enough information given

The next state is 0-1-1. Looking at the truth table, we see that the output for the state 0-1-1 is 1.

18. True or **False** Renumbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.

The numbering of the states directly affects the next state truth table, and therefore changes the logic that is derived from it. Therefore, the answer is **False**.

19. How many latches will a state machine with 23 states require?

- a.) 3            b.) 4            **c.) 5**            d.) 6            e.) 7            f.) 8            g.) 9

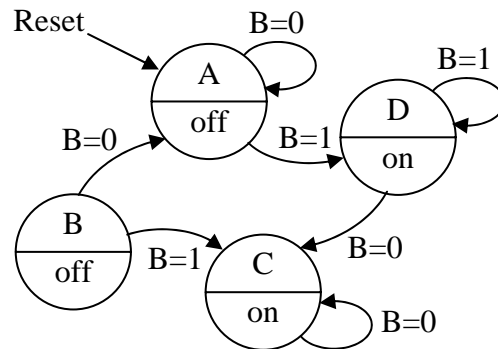
Twenty-three states will be numbered 0, 1, 2, 3, ..., and 22. Since  $22_{10} = 10110_2$ , we will need 5 bits to represent the state. **Therefore, the answer is c.** Another way of looking at it is to see how many states it is possible to represent with n bits, and to figure out what value of  $2^n$  is greater than or equal to 23.  $2^4 = 16$  which is not enough, but  $2^5 = 32$  which should be plenty. Therefore, 5 bits will do the trick.

20. If a group of four rows or columns in a Karnaugh map is identified with two variables, it is numbered 00, 01, 11, 10 instead of 00, 01, 10, 11. Why?

Because any horizontal or vertical movement between adjacent cells can only have 1 input variable change. Numbering 00, 01, 10, 11 has two variables changing when going from 01 to 10 and when wrapping around the table from 00 to 11. 00, 01, 11, 10 does not have this problem.

21. Identify the two errors in the state diagram to the right. The circuit is to have a single binary input B. Do not bother to correct the errors. (2 points each)

- 1.) There is no way to get to state B, and therefore it should be removed.
- 2.) State C has no transition for B=1.

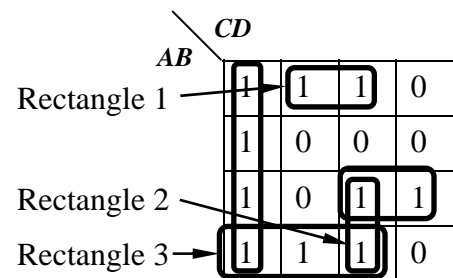


22. For the Karnaugh map to the right, identify the problems with each of the three rectangles shown. (2 points each)

Rectangle 1: Rectangle 1 could be made larger by doubling it "up" across the top border to the bottom row of the map.

Rectangle 2: Rectangle 2 has no cell that is unique to it. Therefore, it should be removed.

Rectangle 3: Rectangle 3 has three cells which is an illegal number of cells. The number of cells in a rectangle must equal a power of 2.



**Medium answers – 4 points each**

23. Complete the truth table to the right with the values for the following sum-of-products expression:

$$\overline{A} \cdot \overline{B} \cdot \overline{C} + A \cdot B + \overline{B} \cdot C$$

Remember that each product generates a 1 when all of its inputs are one, e.g.,  $1 \cdot 1 \cdot 1 = 1$ . This means that if we can figure out where each product equals one, we know where the ones are in the truth table. The remaining positions are filled with zeros.

$$(\overline{A} \cdot \overline{B} \cdot \overline{C}) = 1 \text{ when } A=0, B=0, \text{ and } C=0$$

$$(A \cdot B) = 1 \text{ when } A=1, B=1, \text{ and } C=0 \text{ or } 1$$

$$(\overline{B} \cdot C) = 1 \text{ when } A=0 \text{ or } 1, B=0, \text{ and } C=1$$

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

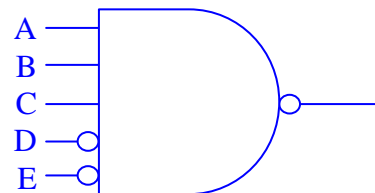
24. In the Karnaugh map to the right, draw the best pattern of rectangles you can. **Do not derive the SOP expression.**

Remember to only include X's in rectangles if they make the rectangle bigger. Do not include an X if it adds an additional rectangle.

		CD			
		00	01	11	10
AB	00	1	1	0	0
	01	1	0	0	1
	11	X	X	0	1
	10	1	0	0	0

25. In the space to the right, draw the decoding logic circuit with an active-low output that identifies when  $A = 1, B = 1, C = 1, D = 0,$  and  $E = 0$ .

An active-low decoder is meant to have a zero output for exactly one pattern of 1's and 0's at its inputs. This is done with a NAND gate where the inputs that are supposed to be 1 go straight into the inputs while the inputs that are supposed to be 0 pass through an inverter first.

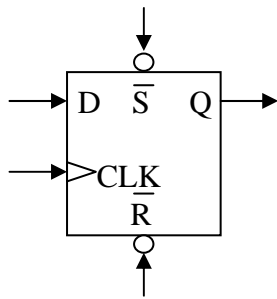


26. Create a Karnaugh map from the truth table below. **Do not worry about making the rectangles.**

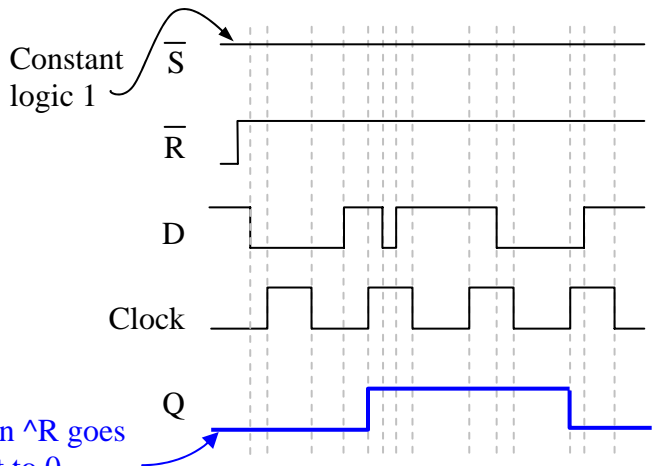
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

		C	
		0	1
AB	00	0	1
	01	1	0
	11	0	0
	10	1	1

27. Show the  $D$  latch output waveform  $Q$  based on the inputs  $D$ ,  $\bar{S}$ ,  $\bar{R}$ , and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)



Note that when  $\bar{R}$  goes low,  $Q$  is reset to 0.

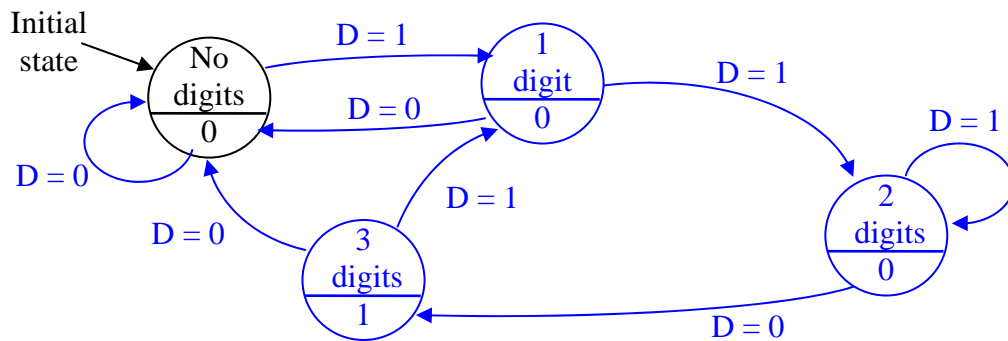


**Longer answers – Points vary per problem**

28. Make the state diagram that will output a '1' when the sequence '110' is detected in a serial stream of bits. For example, if the following binary stream is received:

0 0 1 **1 1 0** 1 0 1 0 1 1 **1 1 0** 0 0 0 0 **1 1 0** 1 **1 1 0** 0 1 0

then 1's will be output at these points. At all other times, the system will output zeros. Label the input  $D$ . (8 points)



29. Derive the minimum SOP expression from the Karnaugh map below. (6 points)

	$CD$			
$AB$	00	01	11	10
00	0	0	0	1
01	1	1	0	1
11	1	1	0	1
10	1	1	1	1

Red rectangle

A	B	C	D
0	1	0	0
0	1	0	1
1	1	0	0
1	1	0	1

A and D drop out. Since C equals 0 for all cells, it is inverted.

$$B \cdot \bar{C}$$

Blue rectangle

A	B	C	D
0	0	1	0
0	1	1	0
1	1	1	0
1	0	1	0

A and B drop out. Since D equals 0 for all cells, it is inverted.

$$C \cdot \bar{D}$$

Green rectangle

A	B	C	D
1	0	0	0
1	0	0	1
1	0	1	1
1	0	1	0

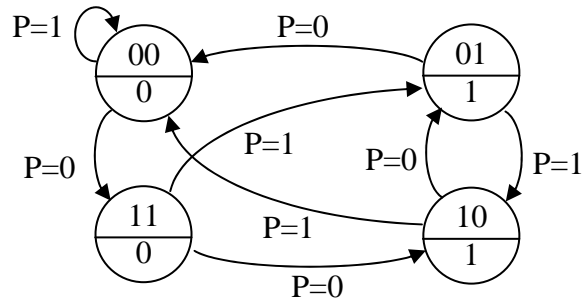
C and D drop out. Since B equals 0 for all cells, it is inverted.

$$A \cdot \bar{B}$$

The final answer is:

$$A \cdot \bar{B} + B \cdot \bar{C} + C \cdot \bar{D}$$

30. Create the next state truth table and the output truth table for the state diagram to the right. Use the variable names  $S_1$  and  $S_0$  to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (8 points)



Next State T.T.

$S_1$	$S_0$	P	$S_1'$	$S_0'$
0	0	0	1	1
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	1

Output T.T.

$S_1$	$S_0$	X
0	0	0
0	1	1
1	0	1
1	1	0

31. The three Boolean expressions below represent the *next state bits* ( $S_0'$  and  $S_1'$ ) and the *output bit X* based on the *current state* ( $S_0$  and  $S_1$ ) and the *input A*. Draw the logic circuit for the state machine including the latches and output circuitry. *Be sure to label the latch inputs and other signals.* (8 points)

$$S_0' = S_1 + A$$

$$S_1' = \overline{S_0} \cdot A$$

$$X = S_1$$

