

Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Spring Semester, 2006

Section 001

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- **Calculators are not allowed.** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

“Fine print”

Academic Misconduct:

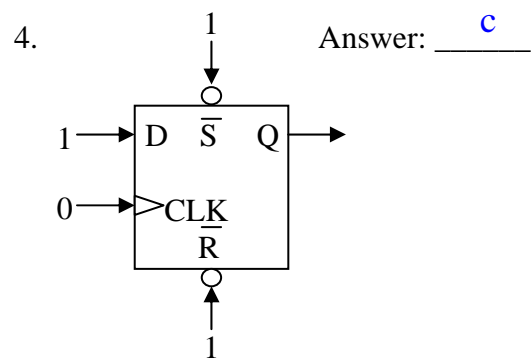
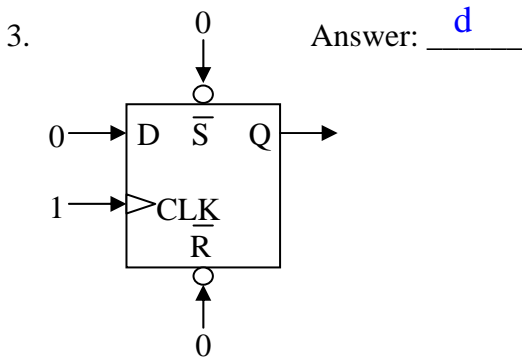
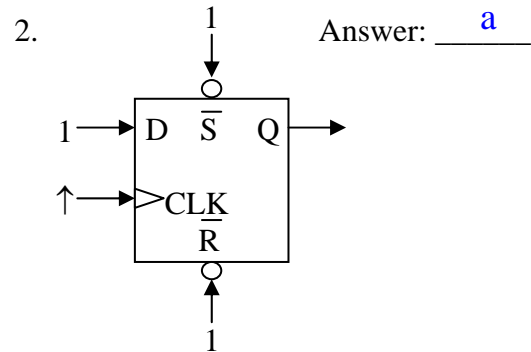
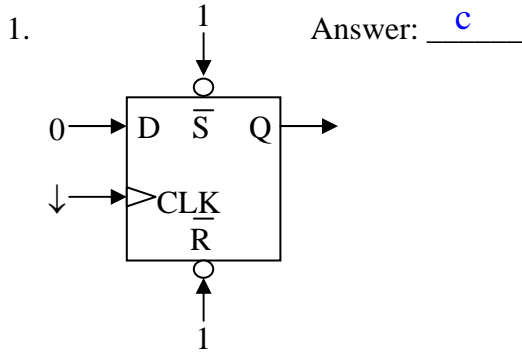
Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarizing, the changing or falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Short answers – 2 points each

For the following **four** circuits, identify the value of the output Q from the following choices. Consider the D-latch a **rising edge triggered latch**.

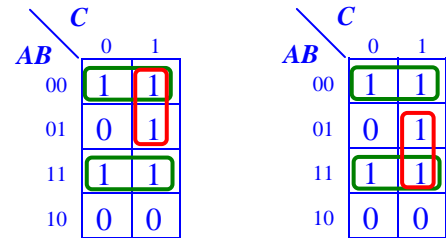
- a.) 1 b.) 0 c.) Q_0 (stored value of Q) d.) undefined/illegal e.) can't tell



5. True or False: The expression $(\bar{A} + B + C) \cdot (B + C) \cdot (\bar{A} + \bar{B})$ is in proper Product-of-Sums format.

6. In the space to the right, give an example of a 3-input Karnaugh map where more than one pattern of rectangles exists for the same arrangement of 1's and 0's.

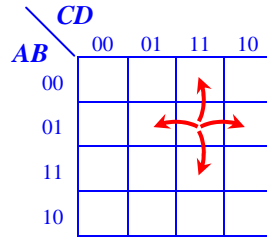
There are a number of cases where multiple rectangles can be used to satisfy a Karnaugh map. The one I've shown to the right can have the vertical rectangle in one of two places.



7. True or False: In a Karnaugh map, there must be an adjacent cell for every possible single-variable change. For example, if a Karnaugh map has three input variables, then there must be three cells adjacent to every cell in the map where only one variable value changes in a move to that cell.

This is true. Remember that the purpose of a Karnaugh map is to rearrange the truth table so that adjacent cells can be combined allowing for a term to drop out. In other words, the key to the effectiveness of Karnaugh maps is that each cell represents the output for a specific pattern of ones and zeros at the input, and that to move to an adjacent cell, exactly one of those inputs can change, the rest must remain the same. Take for instance the 16 cell (4-input) Karnaugh map. The cell in the third column of the second row represents the condition where $A=0, B=1, C=1,$ and $D=1$. Moving to the cell immediately to the left will change only C; moving right will change D; moving

up changes B; and moving down changes A. Therefore, there is an adjacent cell that represents a change in any of the four input variables.



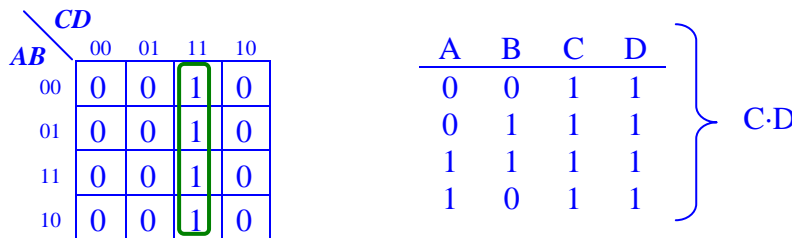
8. How many cells does a 2 input Karnaugh map have?

There are $2^2 = 4$ possible values for two inputs, i.e., 00, 01, 10, and 11. Since there must be a cell in the Karnaugh map for every possible pattern of ones and zeros at the input, there must be four cells.

- a.) 2 **b.) 4** c.) 6 d.) 8 e.) 16 f.) 24 g.) 32

9. In a 4-variable Karnaugh map, how many input variables (A, B, C, or D) does a product have if its corresponding rectangle of 1's contains 4 cells?

A simple way to answer this question is to create a Karnaugh map that has a rectangle with four 1's, then figure out what the product is. The number of inputs in the product will give us our answer.



The resulting product has two inputs. You'll find that regardless of how the 4 cell rectangle is arranged, the resulting product will always have 2 inputs.

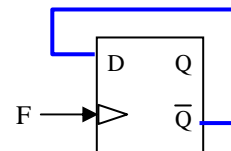
- a.) 1 **b.) 2** c.) 3 d.) 4 e.) Cannot be determined

10. An active-low transparent latch copies data from the D input to the Q output:

- a.)** as long as the clock equals a logic 0 b.) the instant the clock changes from a 1 to a 0
 c.) as long as the clock equals a logic 1 d.) the instant the clock changes from a 0 to a 1

11. **True** or False: The D-latch is built around the S-R latch, and therefore, every D-latch contains within it an S-R latch.

12. Make the connections to the latch in the figure to the right that makes a divide-by-two circuit, i.e., divides the frequency F in half at the output Q.



13. Which of the following expressions produces the truth table to the right?

- a.) $A + C$
d.) $\bar{B} \cdot C$

- b.) $A + \bar{B}$
e.) $A + \bar{B} \cdot C$

- c.) $A + \bar{B} + C$
f.) None of the above

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

The easiest way to figure out this problem is to figure out what the truth tables for each of the options is.

- Selection 'a' will have a 1 in every row where $A=1$ or $C=1$. This doesn't work because the fourth row (where $C=1$) has a zero output. This eliminates selection 'a'.
- Selection 'b' will have a 1 in every row where $A=1$ or $B=0$. This doesn't work because the first row (where $B=0$) has a zero output. This eliminates selection 'b'.
- Selection 'c' will have a 1 in every row where $A=1$, $B=0$, or $C=1$. This doesn't work because the first row (where $B=0$) and the fourth row (where $C=1$) have a zero output. This eliminates selection 'c'.
- Selection 'd' will have a 1 in every row where both $B=0$ and $C=1$, but zeros everywhere else. This doesn't work because the fifth, seventh, and eighth rows need one's, but this selection will place zeros. This eliminates selection 'd'.
- Selection 'e' will have a 1 in every row where $A=1$ or both $B=0$ and $C=1$, but zeros everywhere else. This works! Therefore, the answer must be 'e'.

This problem could also be done using the SOP process to come up with an equation which can then be simplified. The table to the right shows the different products that are needed to create an SOP function.

$$\bar{A} \cdot \bar{B} \cdot C + A \cdot \bar{B} \cdot \bar{C} + A \cdot \bar{B} \cdot C + A \cdot B \cdot \bar{C} + A \cdot B \cdot C$$

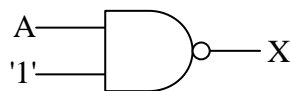
$$\bar{A} \cdot \bar{B} \cdot C + A \cdot (\bar{B} \cdot \bar{C} + \bar{B} \cdot C + B \cdot \bar{C} + B \cdot C)$$

$$\bar{A} \cdot \bar{B} \cdot C + A$$

$$\bar{B} \cdot C + A$$

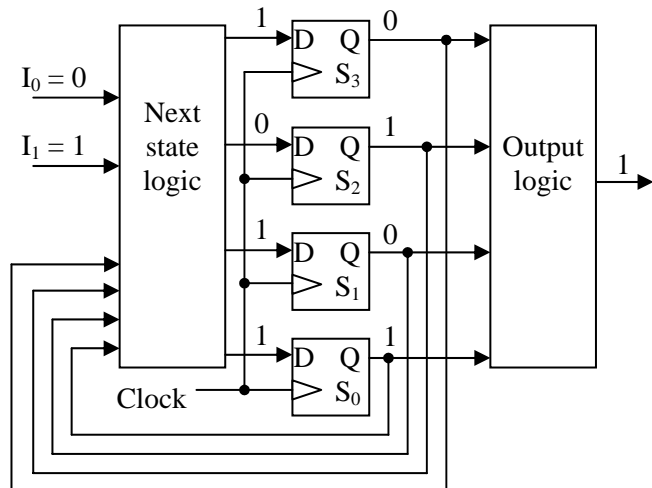
A	B	C	X	
0	0	0	0	
0	0	1	1	$\bar{A} \cdot \bar{B} \cdot C$
0	1	0	0	
0	1	1	0	
1	0	0	1	$A \cdot \bar{B} \cdot \bar{C}$
1	0	1	1	$A \cdot \bar{B} \cdot C$
1	1	0	1	$A \cdot B \cdot \bar{C}$
1	1	1	1	$A \cdot B \cdot C$

14. Fill in the truth table for the NAND circuit shown below.



A	X
0	1
1	0

The next five problems use the state machine diagram to the right. Assume that the states are numbered so that bit S_3 is the MSB and bit S_0 is the LSB.



15. What is the maximum number of states that this system can handle?

Since there are four latches, then the internal memory of this state machine can remember $2^4 = 16$ states: 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, and 1111.

Therefore, the answer is 16.

16. What is the current state of this system?
Keep your answer in binary.

The current state is the value stored in the latches and found at the Q outputs. In the case of the diagram above, that is 0-1-0-1 with S_3 being the most significant bit.

17. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

The next state is the value present at the D inputs, i.e., the value that would be stored if we had a clock pulse occur. In the case of the diagram above, that is 1-0-1-1 with S_3 being the most significant bit.

18. If the input I_1 changed from 1 to 0, but everything else remained unchanged, the output of the system would remain unchanged.

The output of the type of state machine we've described in class relies ONLY on the current state. Since only the input is changing (i.e., we don't get a clock pulse to move to the next state) then the current state stays the same and so does the output.

- a.) True b.) False c.) Not enough information given

19. If the input I_1 changed from 1 to 0, but everything else remained unchanged, the next state that the system would go to after a clock pulse would remain unchanged.

The next state of the machine depends on both the system input and the current state. Therefore, if the input changed, the next state *might* change too depending on the next-state logic. I therefore accepted both "False" and "Not enough information given" as appropriate answers.

- a.) True b.) False c.) Not enough information given

20. True of **False** Renumbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.

The numbering of the states directly affects the next state truth table, and therefore changes the logic that is derived from it. Therefore, the answer is **False**.

21. How many latches will a state machine with 65 states require?

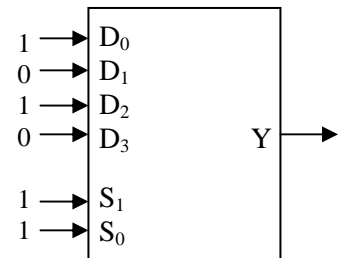
Sixty-five states will be numbered 0, 1, 2, 3, ..., 63, and 64. Since $64_{10} = 1000000_2$, we will need 7 bits to represent the state. **Therefore, the answer is e.** Another way of looking at it is to see how many states it is possible to represent with n bits, and to figure out what value of 2^n is greater than or equal to 65. $2^6 = 64$ which is not enough, but $2^7 = 127$ which should be plenty. Therefore, 7 bits will do the trick.

- a.) 3 b.) 4 c.) 5 d.) 6 **e.) 7** f.) 8 g.) 9

22. If a group of four rows or columns in a Karnaugh map is identified with two variables, it is numbered 00, 01, 11, 10 instead of 00, 01, 10, 11. Why?

Because any horizontal or vertical movement between adjacent cells can only have 1 input variable change. Numbering 00, 01, 10, 11 has two variables changing when going from 01 to 10 and when wrapping around the table from 00 to 11. 00, 01, 11, 10 does not have this problem.

23. For the multiplexer/selector shown to the right, what is the output Y?



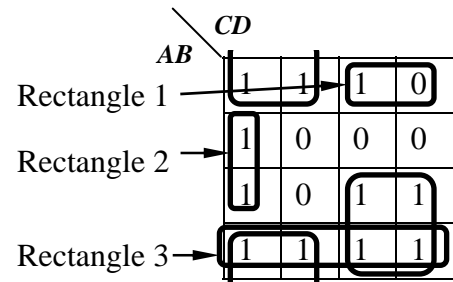
Remember that a multiplexer is like a digitally controlled channel changer using the inputs S_1 and S_0 , to select either D_0 , D_1 , D_2 , or D_3 to be output to Y. The way it works is that the decimal equivalent of the bits at the inputs S_1 and S_0 identify the subscript of the D input being routed to Y. Since S_1 and S_0 both equal 1, and since $11_2 = 3_{10}$, then D_3 is routed to Y. Since D_3 equals 0, then the output at Y equals 0.

24. For the Karnaugh map to the right, identify the problems with each of the three rectangles shown. (2 points each)

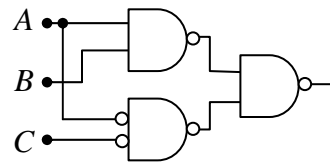
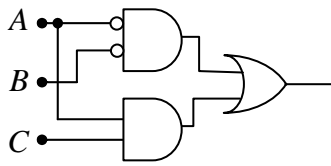
Rectangle 1: This rectangle contains a zero.

Rectangle 2: This rectangle could be made larger by including the whole first column.

Rectangle 3: This rectangle does not contain any unique cells, i.e., it is completely overlapped by other rectangles.



25. True or false The two circuits below are equivalent.



DeMorgan's theorem shows us that an OR gate can be replaced with a NAND gate with inverted inputs. The circuit above replaces the OR gate with a NAND gate with inverted inputs, but it also inverts all of the inputs to the AND gates. This is where the situation becomes false.

This problem could also have been done by developing the truth tables for each circuit and seeing that they were not equal. The truth tables shown below do just that.

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Medium answers – 4 points each

26. Complete the truth table to the right with the values for the following Product-of-Sums expression:

$$(A + B + \bar{C}) \cdot (A + C) \cdot (\bar{A} + B)$$

Remember that each sum generates a 0 when all of its inputs are zero, i.e., $0+0+0=0$. This means that if we can figure out where each sum equals zero, we know where the zeros are in the truth table. The remaining positions are filled with ones.

$(A + B + \bar{C}) = 0$ when $A=0$, $B=0$, and $C=1$

$(A + C) = 0$ when $A=0$, $C=0$, and $B=0$ or 1

$(\bar{A} + B) = 0$ when $A=1$, $B=0$, and $C=0$ or 1

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	
1	0	0	0
1	0	1	0
1	1	0	
1	1	1	

27. In the Karnaugh map to the right, draw the best pattern of rectangles you can. **Do not derive the SOP expression.**

In the pattern of rectangles shown to the right, note that the X's are only included in a rectangle when they are needed to make a larger rectangle. Do not include them if they force you to add another rectangle.

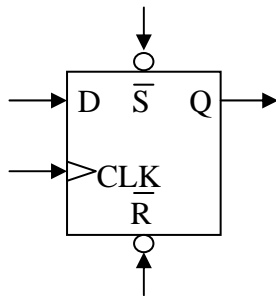
	CD			
AB	00	01	11	10
00	1	1	1	1
01	X	X	0	0
11	0	1	0	0
10	1	1	1	1

28. Create a Karnaugh map from the truth table below. *Do not worry about making the rectangles.*

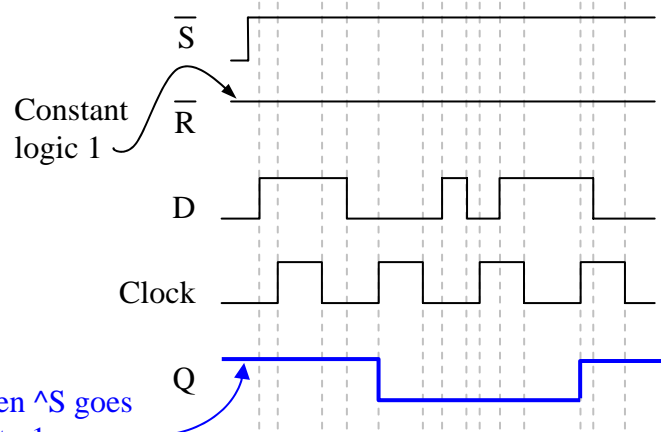
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

		C	
		0	1
AB	00	1	0
	01	0	1
	11	0	1
	10	1	0

29. Show the D latch output waveform Q based on the inputs D , \bar{S} , \bar{R} , and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)



Note that when \bar{S} goes low, Q is set to 1.

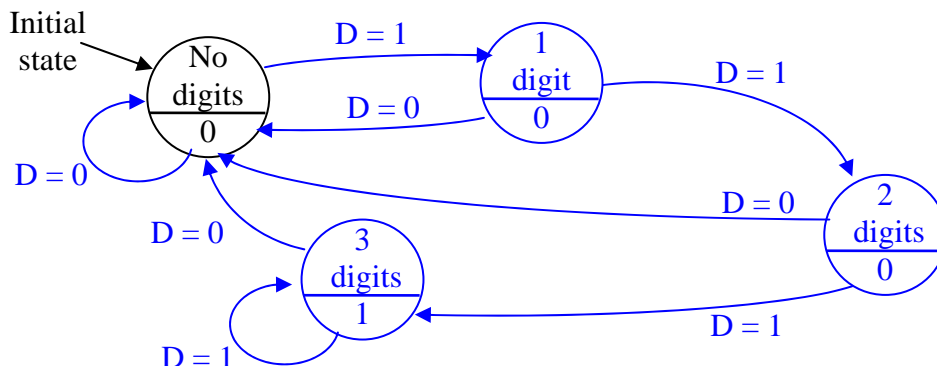


Longer answers – Points vary per problem

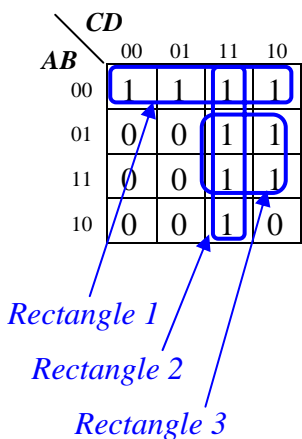
30. Make the state diagram that will output a '1' when the sequence '111' is detected in a serial stream of bits. For example, if the following binary stream is received:

0 0 **1 1 1** 0 1 0 1 0 **1 1 1 1** 0 0 0 0 1 1 0 **1 1 1** 0 0 1 1

then 1's will be output at these points. (Notice that the last two ones of the second pattern are shared with the first two ones of the third pattern.) At all other times, the system will output zeros. Label the input D. (8 points)



31. Derive the minimum SOP expression from the Karnaugh map below. (6 points)



Rectangle 1			
A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0

C, and D drop out. Since A and B are both equal to 0 for all cells, they are inverted.

$$\overline{A} \cdot \overline{B}$$

Rectangle 2			
A	B	C	D
0	0	1	1
0	1	1	1
1	1	1	1
1	0	1	1

A and B drop out. Neither C nor D equal 0, so neither term is inverted.

$$C \cdot D$$

Rectangle 3			
A	B	C	D
0	1	1	1
0	1	1	0
1	1	1	1
1	1	1	0

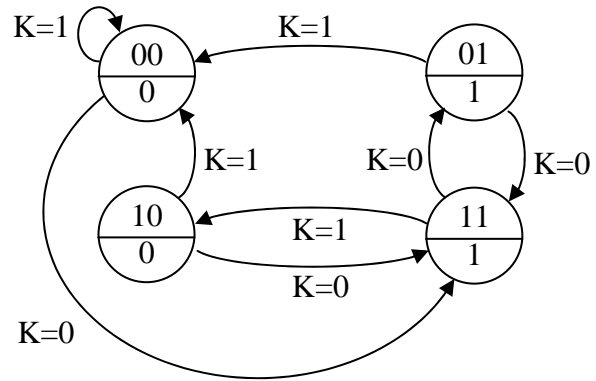
A and D drop out. Neither B nor C equal 0, so neither is inverted.

$$B \cdot C$$

The final answer is:

$$\overline{A} \cdot \overline{B} + C \cdot D + B \cdot C$$

32. Create the next state truth table and the output truth table for the state diagram to the right. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (8 points)



Next State T.T.

S_1	S_0	K	S_1'	S_0'
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Output T.T.

S_1	S_0	X
0	0	0
0	1	1
1	0	0
1	1	1

33. The three Boolean expressions below represent the *next state bits* (S_0' and S_1') and the *output bit* X based on the *current state* (S_0 and S_1) and the *input* A . Draw the logic circuit for the state machine including the latches and output circuitry. *Be sure to label the latch inputs and other signals.* (8 points)

$$S_0' = \bar{S}_1 \bar{S}_0$$

$$S_1' = A$$

$$X = S_1 + S_0$$

