Points missed: _____   Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 1 for Fall Semester, 2002
Section 201

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader (who might not be me!) Failure to do so might result in no credit for answer. Example:**

$$\boxed{32F1_{16}}$$

- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

Binary	Hex		Binary	Hex		Power of 2	Equals
0000	0		1000	8		2^4	16
0001	1		1001	9		2^5	32
0010	2		1010	A		2^6	64
0011	3		1011	B		2^7	128
0100	4		1100	C		2^8	256
0101	5		1101	D		2^9	512
0110	6		1110	E		2^{10}	1K
0111	7		1111	F		2^{20}	1M
						2^{30}	1G

"Fine print"

Short-ish Answer (2 points each)

1. The following component descriptions should suggest whether a device should be implemented in hardware (HW), software (SW), or firmware (FW). In the space next to the description, indicate which implementation would be best. (2 points each)

    ____ The component of a cache that searches the tags for a match must be extremely fast.

    ____ The component that controls engine operation will need to be occasionally changed, but not often, and must have good throughput.

    ____ The component used to control the lights of a traffic signal must be extremely reliable.

    ____ Modifications to the component that interfaces with a camera must be quick and simple with changes in technology.

2. For the following items, indicate whether the characteristic more closely describes a top-down (TD) or a bottom-up (BU) design method. (2 points each)

    ____ Cheaper for small production quantities.

    ____ Efficient use of components

    ____ Past design experience can be drawn upon

    ____ Easier to meet performance goals

3. True or False: Gordon Moore's law (1965) stating that the number of transistors in a single chip would double every year was based trends he had previously observed in the industry.

4. Match the performance solution on the left with the suitable example on the right. (2 points each)

    Removing bottlenecks ❑   ◯ Pipelining

    Prediction ❑   ◯ Distributed processing to peripherals

    Ensuring no component is idle ❑   ◯ Prefetching code for possible branching

    I/O Schemes ❑   ◯ Memory Cache

5. True or False: A block from main memory could possibly be stored in ***any*** line of a cache using fully associative mapping.

6. What is the major drawback of a cache using direct mapping?

    a.) Searching to see if the block is contained in one of the cache's lines is slow.
    b.) Although simple in operation, the hardware to realize its operation is complex.
    c.) It is possible that the cache will thrash between two block making misses very high.
    d.) It is the most expensive of the three configurations.

7. True or False: With a 2-way set associative cache it is easier to implement the Least Frequently Used replacement algorithm than the Least Recently Used algorithm?

8. True or False: The "write back" cache write policy means that when an update is made to main memory, every cache that is connected to memory is automatically updated by a controller.

9. True or False: Simulation studies have shown that the random replacement algorithm for caches provides only slightly inferior performance to an algorithm based on usage.

10. True or False: The Least Recently Used replacement algorithm for caches always replaces the block/line in a cache that was loaded longest ago.

The next 3 questions are based on the small portion shown below of a cache using direct mapping.

Tag (binary)	Line number (binary)	Word within block				
		00	01	10	11	
0101 0011 01	01 0100 1001 10	0x23	0x56	0xaf	0x3d	Row a
0100 1101 10	01 0100 1001 11	0x12	0xc4	0xa1	0x00	Row b
1010 1101 11	01 0100 1010 00	0x34	0x3a	0x09	0x03	Row c
0110 1011 11	01 0100 1010 01	0x58	0xa5	0x56	0x76	Row d
1011 0101 01	01 0100 1010 10	0x67	0xa2	**0xff**	0xf4	Row e
1111 0001 00	01 0100 1010 11	0x9a	0xa3	0xf2	0xf3	Row f
		Col 0	Col 1	Col 2	Col 3	

11. A block containing the address 0x3514a5 is not contained in the cache. When loaded, which row (a through f) and column (0 through 3) will its value be stored in?

12. What is the main memory address of the data 0xff in the section of cache? Leave your answer in binary if you wish.

13. The main memory address $0x53549b = 01010011110101001001011_2$ is contained in this cache.

    a.) True   b.) False   c.) Cannot be determined -- could possibly be elsewhere in the cache

14. For a memory organization with 32-bit addresses, blocks containing 8 words, and a cache containing $2^{12} = 2K$ lines, how many bits does the tag have with direct mapping?

15. For the previous question, how many bits would the tag have if the mapping function were changed to 4-way set associative mapping?

16. The term "split caches" best refers to:
    a) Multiple levels of cache memory in the hierarchy between the processor and main memory.
    b) A method of splitting the lines of a cache based on a mapping algorithm.
    c) A cache that is embedded within a pipe-lined architecture
    d) Two separate caches: one for instructions and one for data
    e) Caches used within a predictive architecture
    f) Caches used with multiple CPU systems

17. The graphic to the right depicts the digits of a 4-bit Hamming code where a single bit error has occurred. Circle the bit that has flipped.
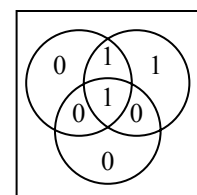
18. True or False: The graphic to the right depicts the digits of a 4-bit Hamming code with parity where a double bit error has occurred.
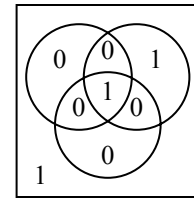
19. If it takes a minimum of 8 bits to correct a single error in a 128-bit data word, then how many bits will it take to do single-error correction with double-error detection?

    a.) 8   b.) 9   c.) 10   d.) Cannot be determined   e.) None of the above

20. For single error correction, what is the minimum number of check bits required for 32 data bits?

    a.) 4   b.) 5   c.) 6   d.) 7   e.) 8   f.) 9   g.) 10   h.) 11   i.) 12

21. If the check code stored for a piece of data is 01101 and the check code calculated on the data retrieved from memory is 01110, what is the syndrome word?

22. What is the capacity in terms of the number of *addressable* locations of a DRAM with 15 rows?

23. True or false: The data rate (i.e., rate at which bits are retrieved from the disk) goes up for tracks on a hard drive that are farther from the center on a disk with constant angular velocity.

24. True or false: Low-level formatting is used to set up the sectors and tracks and add identification and error checking to them.

25. True or false: Rotational Position Sensing increases a magnetic disk system's speed by increasing the density of data on tracks that are further from the center of the disk.

26. True or false: RAID 1 with its mirrored disks potentially reduces read times over RAID 0.

27. True or false: RAID 4 with its large strips and bit-by-bit parity stored on a parity disk has high parallel I/O request rates, but has very poor data transfer rates.

28. Assume that disk 3 of 5 total disks in a RAID 2 system fails and must be replaced. What value would you replace bit $X_3(i)$ with if $X_0(i)=0$, $X_1(i)=1$, $X_2(i)=1$, and $X_4(i)=1$.

    a.) 1   b.) 0   c.) Cannot be determined. Need to know which disk was parity disk.

29. Assume a user needs the capacity of 6 hard drives. If they were to use RAID 6 with its XOR parity and its data check algorithm, how many hard drives would be required to implement it?

Longer Answers (Points vary per problem)

30. Three policies were discussed in class on how to deal with multiple CPUs writing to their individual caches, but not updating main memory. List one of the methods. (Be more descriptive than just writing the name alone.) (4 points)

31. The table below describes the position number of the data and code bits of a single error correction code. Determine the equations to derive C4, C2, and C1 from D4, D3, D2, and D1. (6 points)

M+K Bit position	7	6	5	4	3	2	1
Position number	111	110	101	100	011	010	001
Data bits	D4	D3	D2		D1		
Code bits				C4		C2	C1

C4 =

C2 =

C1 =

32. For the error correcting system of the previous question, assume that the data *retrieved* from memory was 1111, the check code *retrieved* from memory was 001, and the newly calculated check code on the data retrieved from memory was 111. Assuming a single bit error has occurred, what is the original data value? (2 points)

a.) 1111   c.) 1011   e.) 1110   g.) Cannot be determined
b.) 0111   d.) 1101   f.) 1001   h.) None of the above

33. There are two causes for a DRAM cell to require refreshing. List *both* of them. (4 points)

34. There are two reasons why DRAM is preferred over SRAM for main memory. List both of them. (4 points)

35. What is the reason SRAM is preferred over DRAM for cache memory? (3 points)

36. There is one advantage and one disadvantage to reducing the gap between tracks on a hard drive disk. What are they? (4 points)

37. RAID 4 and RAID 5 are similar in that they both calculate parity strips for corresponding strips on other disks. How does RAID 5 offer an improvement over RAID 4? (3 points)