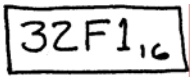
Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 1 for Fall Semester, 2006
Section 001

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes***
- ***Please turn off all cell phones & pagers during the test.***
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader. Failure to do so might result in no credit for answer. Example:**



- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. For each of the following traits of system component design, indicate which implementation method is the best, hardware (HW), software (SW), or firmware (FW), and which is the worst.

Best	Worst	Characteristic	
_____	_____	Least expensive during development	(2 points)
_____	_____	Least expensive during manufacturing	(2 points)
_____	_____	Ease of upgrade	(2 points)
_____	_____	Reliability	(2 points)

2. For the following items, indicate whether the characteristic more closely describes a top-down (TD) or a bottom-up (BU) design method. (1 point each)

   ____ Best for small production quantities, i.e., we're not going to sell a lot of these

   ____ Doesn't have any excess components, e.g., one goal is to reduce chip count for size

   ____ New design is closely related to long-standing, existing product line

   ____ Cost is not a concern

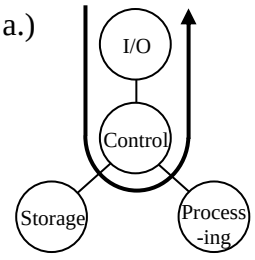
   ____ There are critical performance goals that need to be met

3. Name an important performance measurement for a video conferencing system? Justify your answer. (3 points)

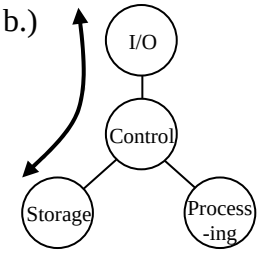
4. Name an important performance measurement for a PDA? Justify your answer. (3 points)

For problems 5 through 8, identify which of the following system functional diagrams, a, b, c, or d, best describes the operation of the example system or application. (2 points each)

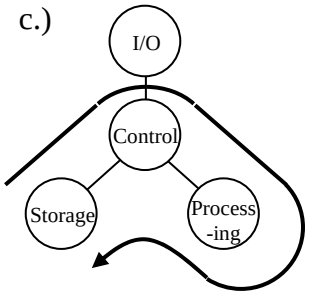
a.)



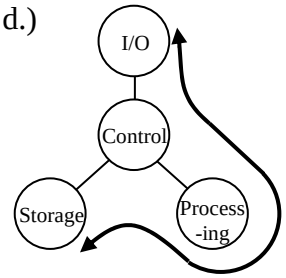
b.)



c.)



d.)



5. An inventory control system checking inventory in and out of a database: _____

6. A hard drive controller buffering data between hard drives and the processor: _____

7. A lighting controller reading switch inputs to control the lighting in a room: _____

8. Hand writing recognition (processor must identify character written before storing it): _____

9. Name three of the five effects discussed in class that Moore's law has had on the contemporary application of computers. (4 points)

10. Name two of the four solutions discussed in class for improving DRAM transfer rates. (3 points)

11. Circle ***all*** of the following traits that are identified as key concepts of the von Neumann architecture. (3 points)

    a.) Control unit interprets instructions and causes them to be executed
    b.) Memory divided into blocks as a way to group related data or instructions
    c.) Sequential execution of code except in the case of "jumps"
    d.) The use of transistors instead of vacuum tubes for the implementation of circuits
    e.) Addressable memory contents without consideration to type of content

12. In the space below, sketch the basic von Neumann architecture. Be sure to label each component and include each of the interconnections. (4 points)

13. Which cache mapping function does not require a replacement algorithm? (2 points)

    a.) Direct mapping b.) Set associative mapping c.) Fully associative mapping

14. Which cache mapping function does not relate a block address to a specific line or set of lines in the cache? (2 points)

    a.) Direct mapping b.) Set associative mapping c.) Fully associative mapping

15. Which cache mapping function is the most expensive to implement? (2 points)

    a.) Direct mapping b.) Set associative mapping c.) Fully associative mapping

16. Which cache mapping function is most likely to thrash, i.e., two blocks contending with each other to be stored in the same line of the cache? (2 points)

    a.) Direct mapping b.) Set associative mapping c.) Fully associative mapping

17. Which replacement algorithm is ***easier*** to implement with a 2-way set associative cache, Least Frequently Used or Least Recently Used? (2 points)

18. Describe how the Least Frequently Used cache replacement algorithm works. (3 points)

19. Assume the processor needs to check the cache for data from the 20-bit memory address $3C45D_{16}$ = 00111100010001011101_2. The cache is a fully associative cache with 2^{10} = 1024 lines and a block size of 2^3 = 8. Derive the tag from the address that will be used to compare to the tags in the cache. (3 points)

20. Repeat the previous problem for a direct cache instead of fully associative. (3 points)

The table below represents a small section of a cache that uses direct mapping. Refer to it to answer questions 21 and 22. Assume the processor's memory bus uses 24 bits for an address.

Tag (binary)	Line number (binary)	Word within block				
		00	01	10	11	
100111011010	0101001011	08_{16}	19_{16}	$2A_{16}$	$3B_{16}$	Row a
110110011000	0101001100	$4C_{16}$	$5D_{16}$	$6E_{16}$	$7F_{16}$	Row b
101101010101	0101001101	50_{16}	61_{16}	72_{16}	83_{16}	Row c
010010111101	0101001110	94_{16}	$A5_{16}$	$B6_{16}$	$C7_{16}$	Row d
111001110011	0101001111	$D7_{16}$	$E9_{16}$	FA_{16}	$0B_{16}$	Row e
011001111001	0101010000	$1C_{16}$	$2D_{16}$	$3E_{16}$	$4F_{16}$	Row f
		Col 0	Col 1	Col 2	Col 3	

21. What is the size of the cache in words (bytes)? (2 points)

22. A block containing the address $8B453F_{16}$ = $100010110100010100111111_2$ is not contained in the cache. When loaded, which row (a-f) and column (0-3) will its values be stored in? (3 points)

23. Assume a ***2-way set-associative cache*** with 2^{11} = 2048 lines is being used in a system with a 24-bit address using a 16-word block size. If a block containing the address $7BE453_{16}$ = $011110111110010001010011_2$ is stored in the cache, what would the tag be? (2 points)

24. Assume a memory access to main memory on a cache "miss" takes 40 ns and a memory access to the cache on a cache "hit" takes 10 ns. If 75% of the processor's memory requests result in a cache "hit", what is the average memory access time? (2 points)

    a.) 17.5 nS b.) 32.5 nS c.) 10 nS d.) 40.0 nS e.) 7.5 nS f.) 2.5 nS

25. For each of the following statements, identify which represent write-back (WB) and which represent write-through (WT) cache writing policies? (2 points each)

    ____ When using this write policy with multiple cache-equipped processors sharing a single RAM, it is possible for RAM to contain an incorrect value for a significant period.

    ____ This write policy generates higher write traffic to DRAM.

26. Why does a DRAM use column and row addressing? ***Circle all that apply.*** (2 points)

    a.) It reduces the number of pins needed to interface with the DRAM
    b.) It's necessary in order to store data to capacitors.
    c.) It can be used to speed up transfers of sequential data within the same row by using page mode.
    d.) It allows for simultaneous writing data to and reading data from the DRAM.
    e.) The cache uses the columns and rows to organize its own data.

27. True or false: The processor may still read from the DRAM while the DRAM is being refreshed. (2 points)

28. True or false: A time critical interrupt should allow nested interrupts. (2 points)

29. Name and describe one of the four types of interrupts, i.e., what types of interrupt triggers are there, that we discussed in class. (2 points)

30. Match the DRAM type with its primary characteristic. (5 points)

Fast Page Mode	❑	❍ overlaps data read with column address write for next read
Extended Data Out	❑	❍ uses fixed row address for multiple column reads
SDRAM	❑	❍ requires adherence to exact bus specification
DDR-SDRAM	❑	❍ incorporates a cache on the memory stick
RAMBUS	❑	❍ returns data to processor synchronized to a full clock pulse
CDRAM	❑	❍ returns data to processor synchronized with both the rising and falling edges of a clock pulse

31. For single error correction, what is the minimum number of check bits required for 12 data bits? (2 points)

a.) 4 b.) 5 c.) 6 d.) 7 e.) 8 f.) 9 g.) 10 h.) 11 i.) 12

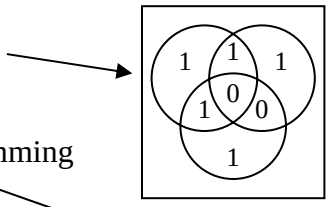
32. If it takes a minimum of 9 bits to correct a single error in a 256-bit data word, then how many bits will it take to do single-error correction with double-error detection? (2 points)

a.) 8 b.) 9 c.) 10 d.) Cannot be determined e.) None of the above

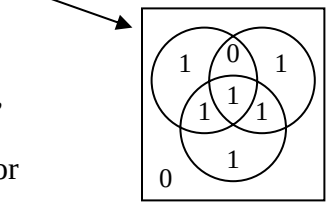
33. What is the total number of ***possible*** syndrome word values for 4 data bits and 3 check bits if we only allow for the cases of no errors or single bit errors? (2 points)

a.) 6 b.) 7 c.) 8 d.) 16 e.) 32 f.) 64 g.) 128 h.) 256 i.) 512

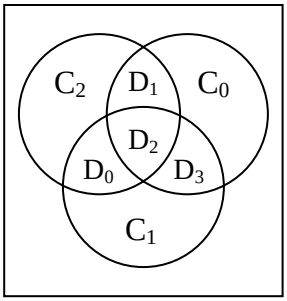
34. The graphic to the right depicts the digits of a 4-bit Hamming code where a single bit error has occurred. Circle the bit that has flipped. (2 points)



35. True or false: The graphic to the right depicts the digits of a 4-bit Hamming code with parity where a double bit error has occurred. (2 points)



36. Assume the figure below shows the grouping of four data bits, D_0, D_1, D_2, and D_3, with three check code bits, C_0, C_1, and C_2. In the space provided, write the expressions used to generate the check code bits for this system. (4 points)



C_2 =

C_1 =

C_0 =