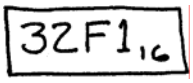
Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 2 for Fall Semester, 2003
Section 201

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader (who might not be me!) Failure to do so might result in no credit for answer. Example:**



- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

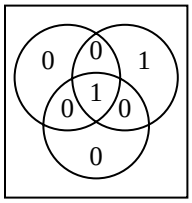
Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

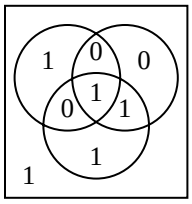
"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Error Checking and Correction

1. True or false: Regarding types of memory errors, a hard error refers to a permanent defect in memory whereas a soft error is a random event causing no permanent damage. (2 points)
2. An error checking code is generated both when data is stored and when it is retrieved. These two codes are compared by doing a bitwise _____ to see if an error has occurred. (2 points)
3. The graphic to the right depicts the digits of a 4-bit Hamming code where a single bit error has occurred. Circle the bit that has flipped. (2 points)



4. True or false: The graphic to the right depicts the digits of a 4-bit Hamming code with parity where a double bit error has occurred. (2 points)



5. If the check code stored with a piece of data is 10011 and the check code calculated on the data retrieved from memory is 10010, what is the syndrome word? (2 points)
6. True or false: Assuming that a single bit error occurred for the syndrome word from problem 5, the syndrome word indicates that there was an error in the check codes, not the stored data. (2 points)
7. If it takes a minimum of 7 bits to correct a single error in a 64-bit data word, then how many bits will it take to do single-error correction with double-error detection? (2 points)

   a.) 7 b.) 8 c.) 9 d.) Cannot be determined e.) None of the above
8. What is the maximum number of data bits that can be monitored for single error correction using a 5 bit check code? (2 points)

   a.) 15 b.) 16 c.) 20 d.) 26 e.) 27 f.) 31 g.) 32 h.) 33 i.) 64
9. The table below describes the position number of the data and code bits of a single error correction code. Determine the equations to derive C_8, C_4, C_2, and C_1 from D_8 through D_1. (6 points)

M+K bit position	12	11	10	9	8	7	6	5	4	3	2	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bit	D_8	D_7	D_6	D_5		D_4	D_3	D_2		D_1		
Check code bit					C_8				C_4		C_2	C_1

   C_8 =

   C_4 =

   C_2 =

   C_1 =
10. For the error correcting system of the previous question, assume that the check code ***retrieved*** from memory was 1001, and the newly ***calculated*** check code on the data retrieved from memory was 1111. Assuming a single bit error has occurred, which bit was the one that flipped, D_8, D_7, D_6, D_5, D_4, D_3, D_2, D_1, C_8, C_4, C_2, or C_1? (2 points)

RAID

11. Assume a user needs the capacity of 4 hard drives. How many drives would the user need for each of the following implementations of RAID?

    RAID 0 _____ drives (1 point)

    RAID 1 _____ drives (1 point)

    RAID 2 _____ drives (1 point)

    RAID 5 _____ drives (1 point)

    RAID 6 _____ drives (1 point)

12. True or false: RAID 1 with its mirrored disks potentially reduces read times over RAID 0. (2 points)

13. What is the bottleneck of the RAID 4 configuration? (3 points)

14. Assume that disk 3 of 5 total disks in a RAID 3 system fails and must be replaced. What value would you replace bit $X_3(i)$ with if $X_0(i)=1$, $X_1(i)=1$, $X_2(i)=0$, and $X_4(i)=0$. (2 points)

    a.) 1 b.) 0 c.) Cannot be determined. Need to know which disk was parity disk.

15. True or False: RAID level 0 does not provide data backup but does improve performance. (2 points)

16. Which level(s) of RAID (0 through 6) can recover from 2 drives failing at the same time regardless of which drives fail? (2 points)

17. Which level(s) of RAID (0 through 6) detects errors using an error detection scheme such as a Hamming Code? (2 points)

18. Which level(s) of RAID (0 through 6) does not provide for any data recovery? (2 points)

Input/Output

19. What is the primary advantage of interrupt driven I/O over programmed or polling I/O. (3 points)

20. What is the primary advantage of DMA over interrupt driven I/O. (3 points)

21. How is priority determined for interrupts connected to the processor where each interrupt has its own interrupt line into the processor? (3 points)

22. How is priority determined for interrupts sharing a single interrupt connected to the processor where the processor must use a software poll? (3 points)

23. What does the processor do while a DMA module takes and retains control of a bus? (2 points)

24. If the DMA module and the I/O device it communicates with are both attached to the system bus, then the DMA must perform both a read and a write for a single transaction. This is no different than the processor having to do both a read and a write. There is still a benefit though. What is it? (2 points)

25. How many times must the DMA use the bus for a single transaction if the DMA module acts as a bridge between the I/O device and the system bus? (2 points)

26. Setting up a DMA transfer required the DMA module be told four details of the transfer. What are they? (4 points)

Bus Architectures

27. List two of the three problems discussed in class that occur when the number of devices on a single bus increases. (3 points)

28. Give an example of a device connected to the Northbridge of the Pentium architecture. (2 points)

29. Give an example of a device connected to the Southbridge of the Pentium architecture. (2 points)

30. True or false: The backside bus is used to connect the processor to high-speed devices such as the L2 cache and the Northbridge. (2 points)

31. True or false: The Northbridge and Southbridge are connected using a PCI bus. (2 points)
32. What signal does a bus with synchronous timing require that asynchronous does not? (2 points)

PCI Bus Architecture

33. The optional PCI bus lines (referring to the original PCI stardard) allow for data widths of how many bits? (2 points)

    a.) 16 b.) 32 c.) 64 d.) 128 e.) None of the above

34. Does the PCI bus arbitration use a single arbiter or distributed arbitration? (2 points)

35. One of the purposes of the PCI bus lines C/BE is to indicate which of the four byte-lanes carry meaningful data. What is their other purpose? (3 points)

36. What is the purpose of the JTAG/boundary scan pins? (2 points)

Of the following characteristics, identify whether the characteristic describes PCI, PCI-E, both, or neither.

37. Has a parallel bus structure. (2 points)

    ☐ PCI ☐ PCI-E ☐ Both ☐ Neither

38. Supports interrupts. (2 points)

    ☐ PCI ☐ PCI-E ☐ Both ☐ Neither

39. Uses differential signalling to allow for long distances. (2 points)

    ☐ PCI ☐ PCI-E ☐ Both ☐ Neither

40. Uses serial "lanes" to communicate. (2 points)

    ☐ PCI ☐ PCI-E ☐ Both ☐ Neither

41. Uses a command structure of approximately 12 to 16 commands. (2 points)

    ☐ PCI ☐ PCI-E ☐ Both ☐ Neither

42. Allows x1, x2, x4, x8, x12, and x16 cards to be plugged into an x16 socket. (2 points)

    ☐ PCI ☐ PCI-E ☐ Both ☐ Neither