Points missed: _____ Student's Name: ___________________________________

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 2 for Fall Semester, 2003
Section 201

**Read this before starting!**

- The total possible score for this test is 100 points.
- This test is closed book and closed notes
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader (who might not be me!) Failure to do so might result in no credit for answer. Example:**

$$\boxed{32F1_{16}}$$

- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

| Binary | Hex |
|---|---|
| 0000 | 0 |
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 7 |

| Binary | Hex |
|---|---|
| 1000 | 8 |
| 1001 | 9 |
| 1010 | A |
| 1011 | B |
| 1100 | C |
| 1101 | D |
| 1110 | E |
| 1111 | F |

| Power of 2 | Equals |
|---|---|
| $2^4$ | 16 |
| $2^5$ | 32 |
| $2^6$ | 64 |
| $2^7$ | 128 |
| $2^8$ | 256 |
| $2^9$ | 512 |
| $2^{10}$ | 1K |
| $2^{20}$ | 1M |
| $2^{30}$ | 1G |

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

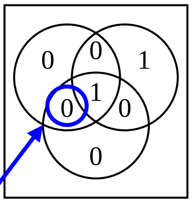
## *Error Checking and Correction*

1. [✓ True] or false: Regarding types of memory errors, a hard error refers to a permanent defect in memory whereas a soft error is a random event causing no permanent damage. (2 points)

   See slide 2 of the Error Detection & Correction lecture.

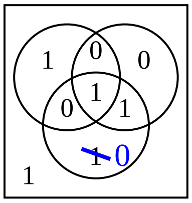
2. An error checking code is generated both when data is stored and when it is retrieved. These two codes are compared by doing a bitwise __XOR____ to see if an error has occurred. (2 points)

3. The graphic to the right depicts the digits of a 4-bit Hamming code where a single bit error has occurred. Circle the bit that has flipped. (2 points)



   The goal here is to find the intersection of the circles with incorrect (non-even) parity. The parity of the top left circle is odd (incorrect). The parity of the top right circle is even (correct). The parity of the bottom circle is odd (incorrect). Therefore, the error is in the intersection of the top left and bottom circles, but NOT the top right circle. This gives us the one section here.

4. True or [✓ false:] The graphic to the right depicts the digits of a 4-bit Hamming code with parity where a double bit error has occurred. (2 points)



   Begin by using the same process from problem 3 to find and correct the bit that is in error. The only circle that has incorrect parity is the bottom circle, and it is corrected by changing the bottom 1 to a 0. Once the suspected bit is corrected, parity is then computed for the entire diagram including the parity bit in the lower left corner. This results in 1 + 0 + 0 + 0 + 1 + 1 + 1 = 4 which is even. Therefore, since correcting the single bit error also corrected the whole diagram's parity, no double error has occurred.

5. If the check code stored with a piece of data is 10011 and the check code calculated on the data retrieved from memory is 10010, what is the syndrome word? (2 points)

$$\begin{array}{r} 10011 \\ \underline{\oplus 10010} \\ 00001 \end{array}$$

6. [✓ True] or false: Assuming that a single bit error occurred for the syndrome word from problem 5, the syndrome word indicates that there was an error in the check bits, not the stored data. (2 pts)

   A syndrome word with exactly one bit set to a 1 occurs only when one bit differs between the two sets of check codes, the one calculated upon storing and the one calculated from the retrieved data. This indicates a bit in the check code was flipped since any error in the data would have resulted in a syndrome word with multiple bits set to one.

7. If it takes a minimum of 7 bits to correct a single error in a 64-bit data word, then how many bits will it take to do single-error correction with double-error detection? (2 points)

   a.) 7 [✓ b.)] 8 c.) 9 d.) Cannot be determined e.) None of the above

8. What is the maximum number of data bits that can be monitored for single error correction using a 5 bit check code? (2 points)

   a.) 15 b.) 16 c.) 20 [✓ d.)] 26 e.) 27 f.) 31 g.) 32 h.) 33 i.) 64

9. The table below describes the position number of the data and code bits of a single error correction code. Determine the equations to derive $C_8$, $C_4$, $C_2$, and $C_1$ from $D_8$ through $D_1$. (6 points)

| M+K bit position | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Position number | 1100 | 1011 | 1010 | 1001 | 1000 | 0111 | 0110 | 0101 | 0100 | 0011 | 0010 | 0001 |
| Data bit | $D_8$ | $D_7$ | $D_6$ | $D_5$ |  | $D_4$ | $D_3$ | $D_2$ |  | $D_1$ |  |  |
| Check code bit |  |  |  |  | $C_8$ |  |  |  | $C_4$ |  | $C_2$ | $C_1$ |

$C_8 = D_8 \oplus D_7 \oplus D_6 \oplus D_5$

$C_4 = D_8 \oplus D_4 \oplus D_3 \oplus D_2$

$C_2 = D_7 \oplus D_6 \oplus D_4 \oplus D_3 \oplus D_1$

$C_1 = D_7 \oplus D_5 \oplus D_4 \oplus D_2 \oplus D_1$

10. For the error correcting system of the previous question, assume that the check code ***retrieved*** from memory was 1001, and the newly ***calculated*** check code on the data retrieved from memory was 1111. Assuming a single bit error has occurred, which bit was the one that flipped, $D_8$, $D_7$, $D_6$, $D_5$, $D_4$, $D_3$, $D_2$, $D_1$, $C_8$, $C_4$, $C_2$, or $C_1$? (2 points)

Begin by calculating the syndrome word. This is done as in problem 5 by a bitwise XOR.

$$\begin{array}{r} 1001 \\ \underline{\oplus 1111} \\ 0110 \end{array}$$

This implies that $C_2$ and $C_4$ are the parity calculations that are in error. The only bit that is a member of these two parity calculations and NOT the parity calculations for $C_8$ and $C_1$ is:

$D_3$

### *RAID*

11. Assume a user needs the capacity of 4 hard drives. How many drives would the user need for each of the following implementations of RAID?

Note: There is a figure in the book that does this exact calculation for each of the configurations.

RAID 0 ___ 4 ___ drives (1 point) No data duplication, just striping → no extra drives

RAID 1 ___ 8 ___ drives (1 point) Full mirroring → duplicate number of drives

RAID 2 ___ 7 ___ drives (1 point) Hamming code → 4 bits + 3 check bits = 7 drives

RAID 5 ___ 5 ___ drives (1 point) One additional disk for parity

RAID 6 ___ 6 ___ drives (1 point) One disk for parity, 2nd for data check algorithm

12. [✓ True] or false: RAID 1 with its mirrored disks potentially reduces read times over RAID 0. (2 points)

Due to different positions of the read heads, the seek time of one of the mirrored disks will be slightly quicker than the other. This improves performance slightly.

13. What is the bottleneck of the RAID 4 configuration? (3 points)

Every read or write to the array must access the ***parity disk*** regardless of which of the other disks the desired data is on.

14. Assume that disk 3 of 5 total disks in a RAID 3 system fails and must be replaced. What value would you replace bit $X_3(i)$ with if $X_0(i)=1$, $X_1(i)=1$, $X_2(i)=0$, and $X_4(i)=0$. (2 points)

a.) 1 [✓ b.)] 0 c.) Cannot be determined. Need to know which disk was parity disk.

XOR is an odd mathematical operation in that any of the terms of a sequence of XOR'ed values can be moved to the other side of the equal sign with no effect. For example, the expression below is true:

$$0 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 1$$

If we move the last XOR'ed value to the other side of the equal sign, we still have a valid expression, i.e., both sides of the expression now equal 1:

$$0 \oplus 1 = 1 \oplus 0 \oplus 1 \oplus 1$$

Therefore, it doesn't matter which disk is missing, an XOR of the remaining values should result in the data that was present on the original disk.

$$X_3(i) = X_0(i) \oplus X_1(i) \oplus X_2(i) \oplus X_4(i)$$

$$X_3(i) = 1 \oplus 1 \oplus 0 \oplus 0$$

$$X_3(i) = 0$$

15. [✓ True] or False: RAID level 0 does not provide data backup but does improve performance. (2 points)

16. Which level(s) of RAID (0 through 6) can recover from 2 drives failing at the same time regardless of which drives fail? (2 points)

RAID 1, with its fully mirrored drives, could conceivably recover from multiple drives failing as long as the drives weren't the ones that were mirrors of each other. Therefore, ***RAID 6 is the only one that can recover regardless of which drives fail.***

17. Which level(s) of RAID (0 through 6) detects errors using an error detection scheme such as a Hamming Code? (2 points)

RAID 2

18. Which level(s) of RAID (0 through 6) does not provide for any data recovery? (2 points)

RAID 0

## *Input/Output*

19. What is the primary advantage of interrupt driven I/O over programmed or polling I/O. (3 points)

    If interrupts are not used, the processor must continually check to see if the I/O devices are available or if they are in need of attention. This responsibility is removed when interrupts are used because each device is given the mechanism to demand the processor's attention even if the processor is doing something else. This frees the processor to work on other tasks.

20. What is the primary advantage of DMA over interrupt driven I/O. (3 points)

    A two-step process is required when a processor is used to transfer data from an I/O device to memory. First, the processor reads a data element from the I/O device, then it has to store it to memory. With DMA, the DMA processor handles the data transfer freeing the processor to do other things at the cost of losing some access to the bus.

21. How is priority determined for interrupts connected to the processor where each interrupt has its own interrupt line into the processor? (3 points)

    The internal (hardware) structure of the processor makes it so that certain interrupt lines are checked before others are. It is this internal structure that determines the priority. Therefore, the order in which the devices are connected to the interrupt pins is how the designer makes the interrupts of one device have priority over another.

22. How is priority determined for interrupts sharing a single interrupt connected to the processor where the processor must use a software poll? (3 points)

    In a software poll, the interrupt routine goes through and checks each device to see which one needed service. It is the order that this checking is done in software that determines the priority.

23. What does the processor do while a DMA module takes and retains control of a bus? (2 points)

    When the DMA module takes control of the bus, it suspends the processor's bus accesses. Therefore, the processor is free to do anything ***except*** access the bus.

24. If the DMA module and the I/O device it communicates with are both attached to the system bus, then the DMA must perform both a read and a write for a single transaction. This is no different than the processor having to do both a read and a write. There is still a benefit though. What is it? (2 points)

    The processor can still perform operations that do not require the bus. In addition, it does not need to pass the data from the I/O device through its internal registers thereby disrupting a more critical process.

25. How many times must the DMA use the bus for a single transaction if the DMA module acts as a bridge between the I/O device and the system bus? (2 points)

    **Once**

26. Setting up a DMA transfer required the DMA module be told four details of the transfer. What are they? (4 points)

    From slide 41 of the I/O lecture, we have:

    1. whether it will be a read or write operation
    2. the address of device to transfer data from
    3. the starting address of memory block for the data transfer
    4. the amount of data to be transferred

### *Bus Architectures*

27. List two of the three problems discussed in class that occur when the number of devices on a single bus increases. (3 points)

    - An increased number of devices usually requires a physically longer bus. A long bus causes attenuation of the bus signals and problems with signal reflections.
    - Slower devices will dictate the maximum speed of the bus.
    - More devices trying to communicate on the bus will cause congestion and force devices to wait longer for access to the bus.

28. Give an example of a device connected to the Northbridge of the Pentium architecture. (2 points)

    From slide 18 of the bus lecture, we can see that aside from its connection to the backside bus, the types of devices connected to the Northbridge are SDRAM, AGP graphics, and the PCI bus.

29. Give an example of a device connected to the Southbridge of the Pentium architecture. (2 points)

    From slide 18 of the bus lecture, we can see that aside from its connection to the Northbridge through the PCI bus, the Southbridge interfaces to slower buses such as ISA, EIDE, and USB.

30. [✓ True] or false: The backside bus is used to connect the processor to high-speed devices such as the L2 cache and the Northbridge. (2 points)

31. [✓ True] or false: The Northbridge and Southbridge are connected using a PCI bus. (2 points)

32. What signal does a bus with synchronous timing require that asynchronous does not? (2 points)

    A clock signal

### *PCI Bus Architecture*

33. The optional PCI bus lines (referring to the original PCI stardard) allow for data widths of how many bits? (2 points)

    a.) 16 b.) 32 [✓ c.)] 64 d.) 128 e.) None of the above

34. Does the PCI bus arbitration use a single arbiter or distributed arbitration? (2 points)

    Single

35. One of the purposes of the PCI bus lines C/BE is to indicate which of the four byte-lanes carry meaningful data. What is their other purpose? (3 points)

The 'C' in C/BE stands for "command" while the "BE" part stands for byte enable. Therefore, the other purpose of these lines is to provide the bus command, i.e., signal the transaction type.

36. What is the purpose of the JTAG/boundary scan pins? (2 points)

They are used to verify or test the hardware.

***Of the following characteristics, identify whether the characteristic describes PCI, PCI-E, both, or neither.***

37. Has a parallel bus structure. (2 points)

☑ PCI ☐ PCI-E ☐ Both ☐ Neither

38. Supports interrupts. (2 points)

☐ PCI ☐ PCI-E ☑ Both ☐ Neither

39. Uses differential signalling to allow for long distances. (2 points)

☐ PCI ☑ PCI-E ☐ Both ☐ Neither

40. Uses serial "lanes" to communicate. (2 points)

☐ PCI ☑ PCI-E ☐ Both ☐ Neither

41. Uses a command structure of approximately 12 to 16 commands. (2 points)

☐ PCI ☐ PCI-E ☑ Both ☐ Neither

42. Allows x1, x2, x4, x8, x12, and x16 cards to be plugged into an x16 socket. (2 points)

☐ PCI ☑ PCI-E ☐ Both ☐ Neither