# New Single-Clock CMOS Latches and Flipflops with Improved Speed and Power Savings

Jiren Yuan and Christer Svensson

*Abstract*—**New dynamic, semistatic, and fully static single-clock CMOS latches and flipflops are proposed. By removing the speed and power bottlenecks of the original true-single-phase clocking (TSPC) and the existing differential latches and flipflops, both delays and power consumptions are considerably reduced. For the nondifferential dynamic, the differential dynamic, the semistatic, and the fully static flipflops, the best reduction factors are 1.3, 2.1, 2.2, and 2.4 for delays and 1.9, 3.5, 3.4, and 6.5 for power-delay products with an average activity ratio (0.25), respectively. The total and the clocked transistor numbers are decreased. In the new differential flipflops, clock loads are minimized and logic-related transistors are purely $n$-type in both $n$- and $p$-latches, giving additional speed advantage to this kind of CMOS circuits.**

*Index Terms*— **Circuit design, circuit optimization, circuit topology, CMOS digital integrated circuits, flip-flops, high speed circuits/devices, integrated circuit design.**

## I. Introduction

LATCHES and flipflops are the basic building blocks of synchronous digital circuits and, to a large extent, determine circuit speed and power consumption. Their structures and performances are affected by clocking strategies of the circuits. The original true-single-phase clocking [1], [2] (TSPC) technique significantly advanced CMOS circuit speed and its nonprecharged version was considered superior in power savings [3]. However, facing today's demands on high speed and low power, its limitations emerge. For example, the lack of complementary signals and the large number of clocked transistors in heavily pipelined circuits are important drawbacks. The original TSPC was developed from dynamic and nondifferential style CMOS circuits, partly from NORA technique [4]. In recent years, precharged differential TSPC flipflops using cascade voltage switch logic (CVSL) logic [5] and set–reset NAND-pair are proposed [6], [7] with penalty of more transistors and precharged nodes. Being power effective, nonprecharged differential TSPC latches and flipflops using CVSL logic and SRAM structure appeared [8]. Among them, there are fully static versions. Static feature, besides its robustness and tolerance for low toggle frequency, is considered important in power savings due to the possibility to idle a circuit partly or completely. Although the existing nonprecharged differential latches and flipflops have advantages such as available complementary outputs, low power, and simple static construction, they suffer from ratio problems and, particularly, the $p$-latches of this kind are really speed bottlenecks.

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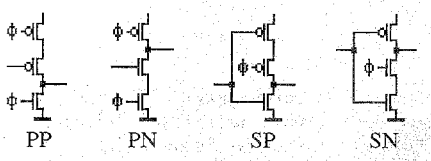


Fig. 1. Four basic stages in TSPC.

The intention of this paper is to propose new circuit solutions, in both nondifferential and differential styles, to meet these demands. TSPC and its speed and power bottlenecks are briefly discussed in Section II. A new nondifferential single-stage TSPC full-latch and its applications are presented in Section III. Bottlenecks of the existing differential latches and flipflops are discussed in Section IV. In Section V, ratio-insensitive differential latches and flipflops are suggested. Single-transistor-clocked differential latches and high-speed differential flipflops are proposed in Sections VI and VII, respectively. Their performances are predicted and compared in Section VIII by simulations and calculations. All simulations in this paper are done by using HSPICE and typical parameters of a 0.8-$\mu$m CMOS process [9]. Conclusions are given in Section IX.

## II. Bottlenecks of the Original TSPC

There are four basic stages in TSPC: precharged p- and n-stages and nonprecharged (static) p- and n-stages, named PP, PN, SP, and SN stages, shown in Fig. 1. A positive edge-triggered flipflop can be formed, in its precharge version, by a combination of PP + SP + PN + SN or, in its nonprecharge version, by a combination of SP + SP + SN + SN. We can call the first two stages a p-block (or p-latch) and the second two stages an n-block (or n-latch). A negative edge-triggered flipflop can be formed by exchanging the p- and n-blocks. Logic operating parts can be included in the flipflops as long as they obey the following rules: in stages PP or PN, logic parts are placed between two clocked transistors with single-type transistors (p or n) and in stages SP or SN, logic parts are placed in their both ends with complementary-type transistors [2]. A pipeline can be formed by alternately placing the p- and n-blocks with logic included or not included. From the viewpoint of high throughput, we prefer to arrange all logic operating parts only in n-blocks and leave p-blocks as half clock cycle delay elements. When complementary inputs to n-blocks are needed, we have to generate them through p-blocks. Fig. 2 shows complementary outputs from (a) a precharged p-block and (b) a nonprecharged p-block. The p-block in (a) or (b), therefore, gives a total delay of three stages which becomes a speed bottleneck.

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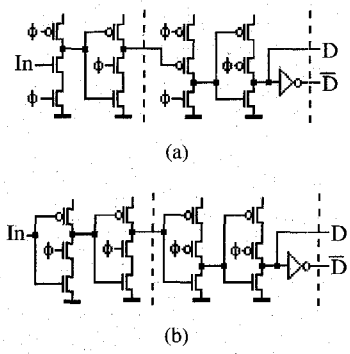


Fig. 2. Complementary outputs generated from original dynamic TSPC flipflops. (a) (PN + SN) + (PP + SP + INV). (b) (SN + SN) + (SP + SP + INV).

The low-power bottlenecks are, first, the clocked transistors with an activity ratio of 1 and, second, the precharged nodes with an activity ratio of 0.5, which is particularly severe in a heavily pipelined circuit [3]. Therefore, in order to raise speed, the p-blocks have to be improved. In order to save power, precharged nodes must be removed and clock loads must be minimized.

## III. A Single-Stage TSPC Full-Latch

For a nondifferential solution, we propose a single-stage TSPC full-latch (FL), which can latch both low and high inputs (an SP stage can only latch a low input), utilizing the available precharged-node signal, shown in Fig. 3(a). The TSPC full-latch, marked by the dash-line box, is similar to a $C^2$MOS stage [10] but does not need a real two-phase clock. Instead, one of the two clock inputs uses the precharged node signal of the preceding n-block. This signal has a feature of inverted clock but is data-dependent during its evaluation phase. Both p- and n-branches in the full latch now become nonconductive during the high clock phase and data-dependently conductive during the low clock phase. It works perfectly with the input data of both one and zero. There are a number of advantages; we can mention three of them. First, the data is fully latched at the output node of the single stage, so the succeeding stage does not have to be precharged [2]. Second, no matter whether the succeeding stage is precharged or not, an inverter can be placed between them to generate complementary outputs. Third, the output node is a three-state node like that of a $C^2$MOS stage, which is useful in, for example, driving a bus. Note that the critical delay path of the full-latch is the p-branch and the size of the middle n-transistor can be small, giving an insignificant load increase to the precharged node of the preceding n-block. In the case of generating complementary outputs, the overall speed is certainly improved. The preceding stage can also be a TSPC-2 type precharged n-latch (PN/SN), see Fig. 3(b).

The nonprecharged TSPC latches, see Fig. 2, are more robust than the precharged latches due to larger noise margins. In order to replace the p-latch (SP + SP) which is the speed bottleneck with the single-stage TSPC full-latch, we can make the n-latch "precharged" by adding a precharging p-transistor at the output node of the first SN stage, named a PSN stage, shown in Fig. 3(c), where the size of the p-transistor marked by * in the first stage is minimized as it is only used for preventing charge sharing. The sign * always represents a minimized size in all figures. After the modification, the advantage of wide noise margin remains, and the output of the n-latch becomes a three-state node.

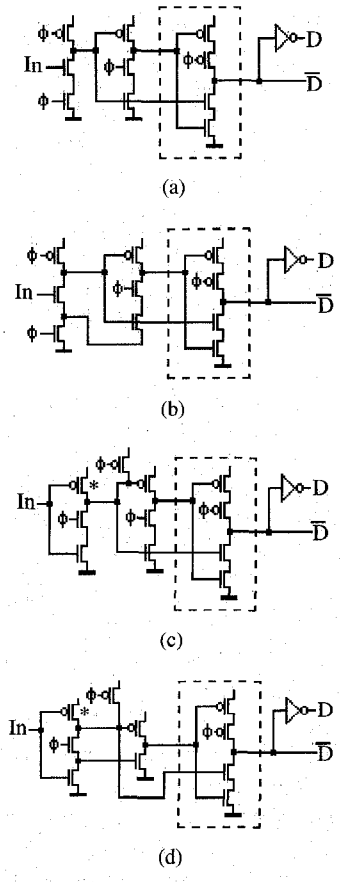


Fig. 3. Complementary outputs generated from new single-clock dynamic flipflops. (a) (PN + SN) + FL(P) + INV. (b) PN/SN + FL(P) + INV. (c) (PSN + SN) + FL(P) + INV. (d) PSLT(N) + FL(P) + INV.

The same modification can be applied to the split-output n-latch [2] which has less clock load and, according to simulation, comparable performance to the (SN + SN) $n$-latch. The modified split-output n-latch is named PSLT(N) and, in the flipflop shown in Fig. 3(d), only three clocked transistors are used in total. The size of the input p-transistor can be minimized. The added precharging p-transistor also increases the robustness of the n-latch as it prevents charge-sharing during a slow latching, so the allowable maximum clock slope is increased to 10 ns, more than twice the original value.

Note that while the flipflops in Fig. 3(a) and (b) do not require stable inputs in both high and low clock phases (except around clock edges), the flipflops in Fig. 3(c) and (d) do require stable inputs during high clock phase. If the input of the flipflop in Fig. 3(c) or (d) changes from high to low when clock is high, both $n$-transistors in the FL(P) stage will be simultaneously conductive for a short while, which may destroy the output. However, in a flipflop chain with or without logic blocks in between, the input to each flipflop is virtually stable between two triggered transitions. This is, therefore, not a problem but to note this is important in special cases.

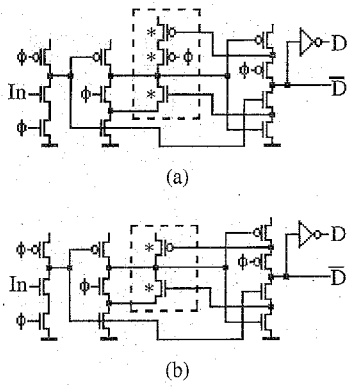


Fig. 4. Nondifferential semistatic flipflops, PN + SN + SFL(P) + INV. (a) Conflict-free version and (b) simplified version.

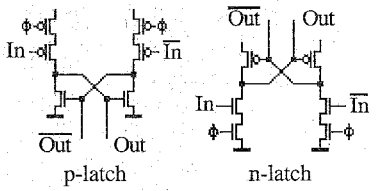


Fig. 5. CVSL-type latches.

The new TSPC full-latch can be made static, named SFL, by adding a few transistors using the similar arrangement of the semistatic divider in [11]. In many cases, it is enough for a flipflop to stay idle at just the low clock phase so a semistatic TSPC flipflop would be adequate in which the n-latch is kept dynamic for the purpose of quick logic operation in a pipeline. Two such semistatic flipflops are shown in Fig. 4(a) and (b). While Fig. 4(a) eliminates completely the conflict between p- and n-branches, Fig. 4(b) uses fewer transistors (less clock load) with very little conflict which will not pose any danger to the function as long as the size of p-transistor in the dashline box is kept minimum. In practice, sizes of both p- and n-transistors in the dashline boxes should be kept minimum to minimize the load. The gate connections (to the half-swing nodes) in Fig. 4(a) and (b) make them very weak when they are conducting and give less load to the full-swing output.

## IV. The Existing Differential Latches

Complementary outputs are inherently available in differential style circuits. The nonprecharged CVSL-type latches appearing in [8], see Fig. 5, do have such an advantage. Their static versions, called RAM-type latches [8], are shown in Fig. 6, where the sizes of two added transistors are minimized. The dynamic differential latches, CVSL(P) and CVSL(N), and the static differential latches, RAM(P) and RAM(N), can be cascaded or mixed to form dynamic, semistatic, and fully static flipflops.

However, they are sensitive to the ratio $W_p/W_n$. While this is not so severe for the $n$-latches as the n-branches can easily be made stronger than the pull-up p-transistors, it really poses a problem for the p-latches. We can use the CVSL latches as examples. If widths of the two p-transistors in the CVSL n-latch and the two n-transistors in the CVSL p-latch are minimized to 2 $\mu$m, corresponding to effective widths of

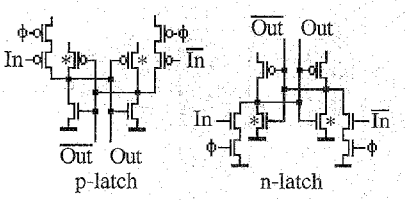


Fig. 6. RAM-type latches.

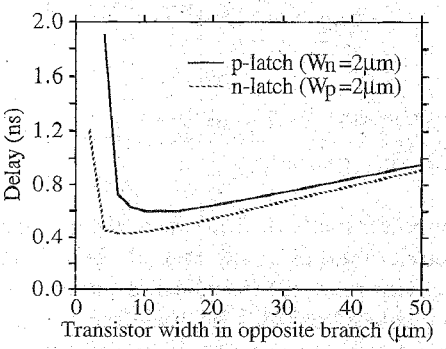


Fig. 7. Delays versus transistor widths for CVSL-type latches.

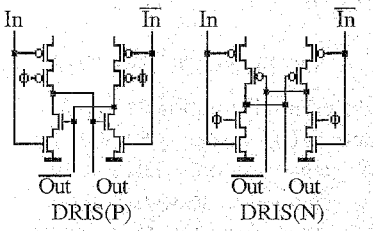


Fig. 8. Dynamic ratio-insensitive differential latches.

1.34 $\mu$m and 0.84 $\mu$m, respectively, in this process [9], delays of the two latches versus widths of the transistors in their opposite branches are shown in Fig. 7. Note that, if considering the effective widths, the real ratios are more than what can be seen in Fig. 7.

If the ratio is not properly designed or changes in different processes and/or with different temperatures, the latches may stop working or present an unexpected large delay, see the left part of Fig. 7. For example, if the n-widths are increased to 4 $\mu$m in the p-latch, the proper p-widths have to be more than 20 $\mu$m, which makes it unnecessarily large. Even so, the p-latch is still the speed bottleneck. Great care must be taken in designing the p-latches particularly when logic is included. In contrast, when $W_p = 4$ $\mu$m and $W_n = 6$ $\mu$m, the $n$-latches work well.

## V. Ratio-Insensitive Differential Latches

To avoid design difficulties and to be robust, completely ratio-insensitive (RIS) differential latches are useful. The proposed dynamic versions of this kind, DRIS(P) and DRIS(N), are shown in Fig. 8. They are formed by cross-connecting two identical $C^2MOS$-like stages with a single clock. From the first glance, they seem to present larger delays and input loads than that of CVSL-type latches but, in fact, it is not so. To be fair, their delays are compared under the same input and output loads. The best (least-delay) width ratios ($W_p/W_n$) are given to the CVSL-type p- and n-latches and, under the same input

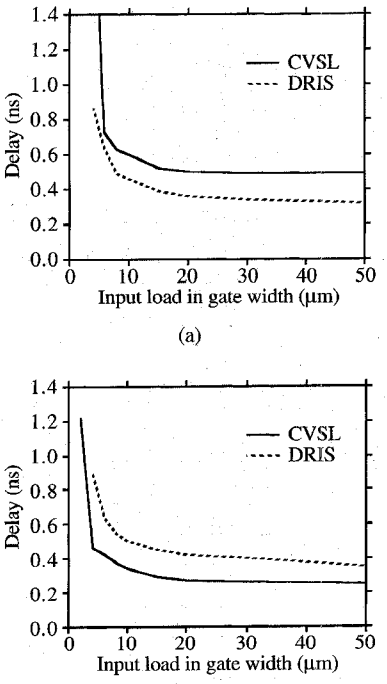


Fig. 9. Delay comparison between CVSL and DRIS latches. (a) P-latches and (b) N-latches.

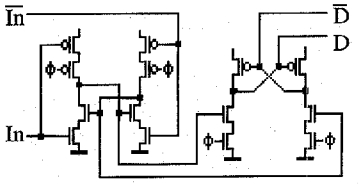


Fig. 10. Combination of DRIS(P) and CVSL(N).

load condition, the width ratios $(W_p/W_n)$ of DRIS n- and p-latches are fixed to two and one, respectively. A minimum inverter ($W_p = W_n = 2$ $\mu$m) is used for the output load. Results are shown in Fig. 9. Not only being ratio-insensitive, the DRIS p-latch is apparently faster than the CVSL-type p-latch, see Fig. 9(a). However, the DRIS n-latch presents larger delay than that of the CVSL-type n-latch, see Fig. 9(b), so the better combination for a flipflop is a DRIS p-latch plus a CVSL-type n-latch, shown in Fig. 10.

The proposed static RIS latches, SRIS(P) and SRIS(N), are shown in Fig. 11. Again, not only ratio-insensitive, the SRIS differential p-latch is significantly faster than the RAM-type p-latch. The principle for the SRIS p-latch is that the two extra minimum-size p-transistors lock the high-output and the extra minimum-size n-transistor locks the low-output (through one of the two bottom n-transistors) during high clock phase. The SRIS n-latch with similar principle is not as fast as the RAM-type n-latch but has the advantage of being ratio-insensitive.

## VI. Single-Transistor-Clocked Latches

It was found that the two clocked transistors in each of the CVSL-type and RAM-type latches can be merged to save power, becoming the proposed first-type single-transistor-clocked (STC) TSPC dynamic and static differential latches,

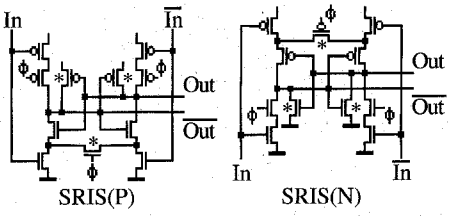


Fig. 11. Static ratio-insensitive differential latches.

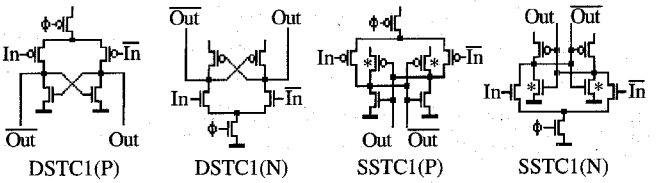


Fig. 12. Single-transistor-clocked TSPC dynamic and static differential latches.

DSTC1(P), DSTC1(N), SSTC1(P), and SSTC1(N), as shown in Fig. 12.

There will be a negative consequence in merging the two clocked transistors, which happens in the latched state. That is the charge-sharing between two output nodes due to the simultaneously conducting of two input transistors (it may happen during the input transition time), which cannot be recovered in the DSTC1 latches but can be recovered in the SSTC1 latches. It means that the correct input transition order and a glitch-free signal to DSTC1 latches are important. For example, the high-to-low input transition must precede the low-to-high transition for the DSTC1 n-latch. Unfortunately, the output transition order of the DSTC1 p-latch is just opposite. Therefore, it is risky to directly cascade DSTC1 p- and n-latches (vice versa). However, there will be virtually no risk to directly cascade SSTC1 latches to form either positive or negative edge-triggered flipflops. Note that the p-latches are still the speed bottlenecks and sensitive to the ratio of p- and n-transistor sizes.

All latches introduced above, except the DSTC1 latches, can be directly cascaded or mixed to form various dynamic, semistatic, and fully static flipflops. As an example, a SRIS p-latch plus a SSTC1 n-latch becomes a fully static flipflop, shown in Fig. 13(a). For DSTC1 latches, inputs must be glitch-free when they are latched and inverters have to be used in between when they are cascaded after other differential latches or in the cases where the input transition order is not correct. The clock load of SRIS p-latch (as well as SRIS n-latch) can be reduced from three-clocked-transistor ($-3$ CT) to two-clocked-transistor ($-2$ CT) by the merging method described above and the fully static flipflop using the SRIS-2 CT p-latch is shown in Fig. 13(b).

## VII. High-Speed Differential Flipflops

The clock loads of differential latches have been minimized above but the speed bottleneck is yet to be removed. We have so far followed the concept of the classic flipflop to develop all these latches. A classic edge-triggered flipflop contains two latches, a master and a slave. While the slave is unlatched, the master must be latched for both high and low output states and

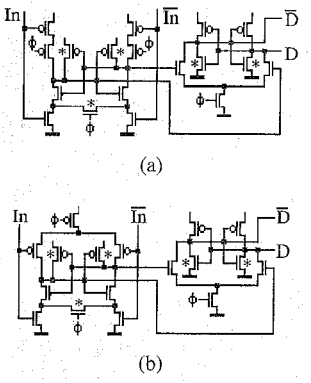


Fig. 13. Fully static flipflops constructed by SRIS p- and SSTC1 n-latches. (a) SRIS − 3CT(P) + SSTC1(N). (b) SRIS − 2CT(P) + SSTC1(N).

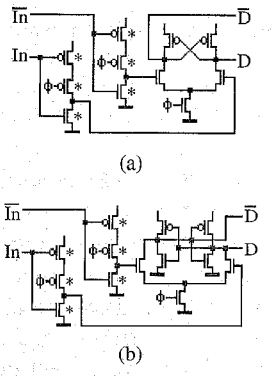


Fig. 14. Positive edge-triggered (a) dynamic ((SP + SP) + DSTC1(N)) and (b) semistatic flipflops ((SP + SP) + SSTC1(N)).

vice versa. However, if there is a nontransparent input state for the unlatched slave, the "latched" master output can be allowed to go to this state without risk. In other words, the master does not have to be a full-latch and it is enough to have only one isolated output state as long as it is identical to the nontransparent input state of the slave. This gives us an opportunity to remove the speed bottleneck. We have used this concept for constructing the nine-transistor high-speed precharged flipflop [2] and found that it can also be used for constructing completely nonprecharged high-speed differential flipflops.

In the proposed flipflops, DSTC1 and SSTC1 n-latch are used as slaves. Note that when they are unlatched, the low-input state is their nontransparent input state. For a dynamic flipflop, we can simply use two separate nonprecharged TSPC SP stages as the master. Although their outputs are not fully latched, they do isolate their outputs at the low state. Two such positive edge-triggered flipflops, a dynamic and a semistatic, are shown in Fig. 14(a) and (b). Note that the two SP stages always give a high-to-low transition first which is required by the DSTC1 n-latch. What worries us now is not the slowness but the fastness of the p-block. Therefore, the n-transistors in the SP stages must be minimized to give enough setup time for the n-latch, and the p-transistors can also be minimized to reduce load and power consumption. The flipflop in Fig. 15(a) or (b) is arranged with a single (nondifferential) input by cascading the two SP stages. To further reduce area and power consumption in a pipeline, the top p-transistors of the two SP stages can be merged with the p-transistors in the preceding DSTC1 or SSTC1 n-latch, shown in Fig. 16.

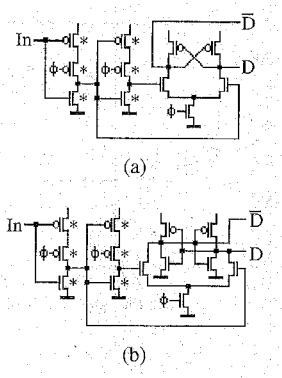


Fig. 15. Nondifferential input and differential output flipflops. (a) SP/SP + DSTC1(N). (b) SP/SP + SSTC1(N).

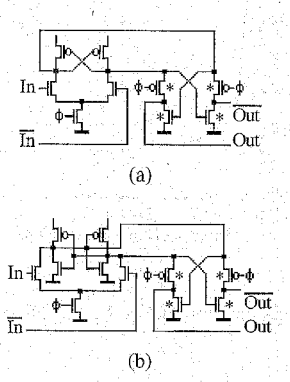


Fig. 16. Merged n- and p-blocks in pipelines. (a) DSTC1(N)/(SP + SP). (b) SSTC1(N)/(SP + SP).

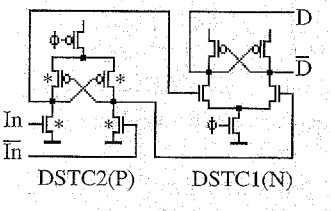


Fig. 17. A high-speed dynamic differential flipflop.

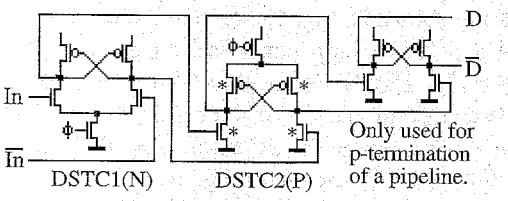


Fig. 18. A termination stage used in a pipeline.

The two separate SP stages of Fig. 14 can be merged, becoming the proposed second-type single-transistor-clocked TSPC dynamic differential p-latch, DSCT2(P), shown in Fig. 17 together with a DSTC1 n-latch forming a high-speed dynamic positive-edge-triggered flipflop. We found similar circuits requiring precharge in [12] but in our case no precharge is involved. A pipeline of this kind may be terminated with a DSTC2 p-latch, the outputs of which are not fully latched. In this case, a termination stage can be used in the end of the pipeline as shown in Fig. 18.

The DSTC2 p-latch looks similar to the DSTC1 n-latch. For example, both cross-coupled pairs are formed by p-transistors. However, they are quite different. The basic function of the

DSTC2 p-latch is similar to that of the two separate SP stages. The input transition order to the DSTC2 p-latch is not important although a DSTC1 n-latch always gives the high-to-low transition first, which is perfect for giving more setup time to a following flipflop of the same kind. When clock falls, the common node of the DSTC2 p-latch will be charged up to a voltage depending on the ratio between the conductances of the clocked transistor and the on-branch. Since the on-branch is formed by a p-transistor and an n-transistor in series with minimized size, the working ratio is easily satisfied. The output where the n-transistor is on will be kept low and the output where the n-transistor is off will be pulled to high, which will turn off the p-transistor where the output is low. Finally, both outputs are firmly defined by the pull-up and pull-down branches. Note that the reason for having high speed is because it has much less ratio problem and the output delay in its unlatched phase is caused by only a single transition (low-to-high) not by two transitions like that of the DSTC1 p-latch as the high-to-low transition has been done in its latched phase. When clock rises, if the inputs remain the same, the output states will be kept though the high-output will lose pull-up capability. If the inputs change to opposite states, both outputs become low after a certain delay. The original low-output will not share the charge on the common node, since the gate and the source of the p-transistor which is originally off will be pulled down simultaneously with a difference almost equal to the p-threshold voltage, confirmed by simulation. Compared with the two separate SP stage arrangement, the DSTC2 p-latch uses only a single clocked transistor and only n-transistors in logic operating positions. The delay of high-to-low transition during latching phase becomes longer due to the discharge of the common node, simulated to be approximately twice the delay of high-to-low transition of the DSTC1 n-latch, enough to guarantee its flip. The size of the clocked p-transistor in the DSTC2 p-latch can be used to control the delay ratio between low-to-high and high-to-low transitions. The input load of the DSTC2 p-latch can be minimized even if logic is included, giving less load to the preceding n-latch and making the flipflop very fast. The flipflop in Fig. 17, therefore, is superior in both high speed and low power.

In order to have all advantages, such as high speed, low power, small input load, logic with only n-transistors, and fully static operations in a single flipflop, we finally propose a static version of the second-type single-transistor-clocked TSPC differential p-latch, SSTC2(P). This is done by adding a minimum inverter and two minimum n-transistors into the DSTC2 p-latch as shown in Fig. 19, where the SSTC2 p-latch is used in a fully static flipflop together with the SSTC1 n-latch. The input inverter is optional depending on what kind of input, nondifferential or differential, is available, which is applicable to all previously introduced differential flipflops.

To make the DSTC2 p-latch static, we only need to prevent a low-output from floating to high and not necessarily to prevent a high-output from floating to low. If the inputs to the DSTC2 p-latch do not change, the above condition will be satisfied inherently since the high-input will pull-down the low-output always. However, when the inputs are flipped during high-clock phase, the low-output loses the pull-down capability

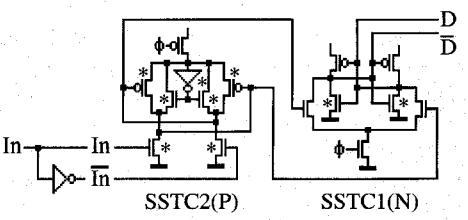


Fig. 19. A high-speed fully static differential flipflop.

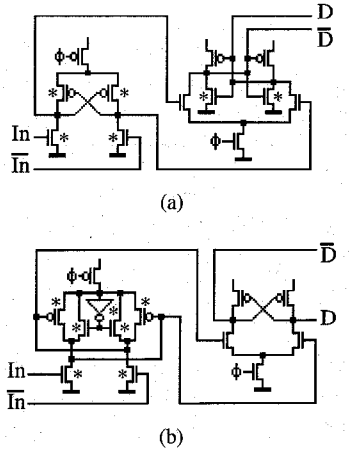


Fig. 20. High-speed semistatic flipflops. (a) DSTC2(P) + SSTC1(N). (b) SSTC2(P) + DSTC1(N).

and might float to high. The SSTC2 p-latch in Fig. 19 can prevent this from occurring. Since the original high-output is pulled down by the new coming high-input, the common node will be forced down and the inverter will give a high output to the two extra n-transistors to pull all other internal nodes down firmly. Only when the clock goes low, the common node is charged to high (the inverter gives a low output to turn off the two extra n-transistors) and the latch returns to normal. Although the ratio issue is affected by the two extra n-transistors now, a twice-the-minimum-size clocked p-transistor will make the SSTC2 $p$-latch work nicely, provided that all other transistors are minimized. To finish this section, we give two semistatic positive edge-triggered differential flipflops in Fig. 20(a) (clock can stay at low) and (b) (clock can stay at high), respectively.

## VIII. Performance Comparisons

To fairly compare different flipflops, complementary outputs are always assumed (remarks will be given to the case of single-ended output in the next section), and to avoid complication in sizing, transistor widths are fixed to $W_p = 6$ $\mu$m and $W_n = 3$ $\mu$m except the CVSL, RAM, and STC n-latches in which $W_p = 4$ $\mu$m and $W_n = 6$ $\mu$m. Widths of all minimum transistors are fixed to 2 $\mu$m. Typical SPICE parameters of a 0.8-$\mu$m CMOS single-poly double-metal process are used [9]. Three identical flipflops are cascaded to simulate realistic input waveforms and output loads. The delay of the middle one is used. Only dynamic power consumptions are taken into account, which are calculated from node to node according to three weight factors. The first is the activity ratio $A$ of a node. $A = 1.0$ for the gate of a clocked transistor, $A = 0.5$ for a

TABLE I
PERFORMANCE COMPARISON OF NONDIFFERENTIAL DYNAMIC FLIPFLOPS

| No. | Flipflop | WD (ns) | NP: A≤0.5 | A=0.1 | A=0.5 | CT | T | Fig. |
|---|---|---|---|---|---|---|---|---|
| 1 | PN+SN+PP+SP+INV | 0.70 (P) | 35.1+33.5A | 38.5 | 51.9 | 6 | 14 | 2(a) |
| 2 | SN+SN+SP+SP+INV | 0.72 (P) | 11.8+73.9A | 19.2 | 48.8 | 4 | 14 | 2(b) |
| 3† | PN+SN+FL(P)+INV | 0.54 (P) | 21.2+39.1A | 25.1 | 40.8 | 4 | 12 | 3(a) |
| 4† | PN/SN+FL(P)+INV | 0.54 (P) | 21.6+39.1A | 25.5 | 41.2 | 4 | 12 | 3(b) |
| 5† | PSN+SN+FL(P)+INV | 0.57 (P) | 22.0+41.0A | 26.1 | 42.5 | 4 | 13 | 3(c) |
| 6† | PSLT(N)+FL(P)+INV | 0.55 (P) | 18.9+41.1A | 23.0 | 39.5 | 3 | 12 | 3(d) |

TABLE II
PERFORMANCE COMPARISON OF DIFFERENTIAL DYNAMIC FLIPFLOPS

| No. | Flipflop | WD (ns) | NP: A≤0.5 | A=0.1 | A=0.5 | CT | T | Fig. |
|---|---|---|---|---|---|---|---|---|
| 7 | CVSL(P)+CVSL(N) | 0.74 (P) | 20.8+48.9A | 25.7 | 45.3 | 4 | 12 | 5 |
| 8† | DRIS(P)+CVSL(N) | 0.48 (N) | 18.0+65.5A | 24.6 | 50.8 | 4 | 14 | 10 |
| 9† | (SP+SP)+DSTC1(N) | 0.41 (N) | 8.1+40.5A | 12.2 | 28.4 | 3 | 11 | 14(a) |
| 10† | DSTC1(N)/(SP+SP) | 0.41 (N) | 8.1+37.5A | 11.9 | 26.9 | 3 | 9 | 16(a) |
| 11† | DSTC2(P)+DSTC1(N) | 0.35 (P) | 9.0+42.7A | 13.3 | 30.4 | 2 | 10 | 17 |

TABLE III
PERFORMANCE COMPARISON OF SEMISTATIC FLIPFLOPS

| No. | Flipflop | WD (ns) | NP: A≤0.5 | A=0.1 | A=0.5 | CT | T | Fig. |
|---|---|---|---|---|---|---|---|---|
| 12 | CVSL(P)+RAM(N) | 0.78 (P) | 20.8+52.8A | 26.1 | 47.2 | 4 | 14 | 5, 6 |
| 13† | PN+SN+SFL(P)+INV | 0.55 (P) | 21.5+43.3A | 25.8 | 43.2 | 4 | 14 | 4(b) |
| 14† | DRIS(P)+RAM(N) | 0.49 (N) | 18.0+69.4A | 24.9 | 52.7 | 4 | 16 | 8, 6 |
| 15† | (SP+SP)+SSTC1(N) | 0.48 (N) | 8.5+44.4A | 12.9 | 30.7 | 3 | 13 | * |
| 16† | SSTC1(N)/(SP+SP) | 0.47 (N) | 8.5+41.4A | 12.6 | 29.2 | 3 | 11 | * |
| 17† | DSTC2(P)+SSTC1(N) | 0.36 (N) | 9.8+46.6A | 14.5 | 33.1 | 2 | 12 | 20(a) |
| 18† | SSTC2(P)+DSTC1(N) | 0.36 (N) | 9.8+52.8A | 15.1 | 36.2 | 2 | 14 | 20(b) |

* Similar to circuit No. 9 and No. 10 with DSTC1(N) replaced by SSTC1(N).

TABLE IV
PERFORMANCE COMPARISON OF FULLY STATIC FLIPFLOPS

| No. | Flipflop | WD (ns) | NP: A≤0.5 | A=0.1 | A=0.5 | CT | T | Fig. |
|---|---|---|---|---|---|---|---|---|
| 19 | Classic Master-Slave | 0.85 | 38.3+108A | 50.1 | 93.3 | 10 | 18 | |
| 20 | RAM(P)+RAM(N) | 0.89 (P) | 20.8+56.8A | 26.5 | 49.2 | 4 | 16 | 6 |
| 21† | SRIS(P)+SSTC1(N) | 0.65 (P) | 13.7+75.4A | 21.2 | 51.4 | 2 | 18 | 13(a) |
| 22† | SSTC2(P)+SSTC1(N) | 0.36 (N) | 9.8+56.8A | 15.5 | 38.2 | 2 | 16 | 19 |

precharged node, and $A \leq 0.5$ for a normal node. The second is the swing $S$ of a node, $S = 1.0$ for an output node, $S = 0.7$ for a node between same-type transistors (body-effect), and $S = 0$ for a power or ground node. The third is the capacitance $C$. In the 0.8-$\mu$m CMOS process, the capacitance values of n (or p)-gate-to-substrate and n-drain (or source)-to-substrate are quite similar, 3.3 fF for a minimum width (2 $\mu$m) transistor defined as a unit-capacitance ($C_{\text{unit}}$), while the capacitance values of p-drain (or source)-to-substrate and n (or p)-gate-to-drain (or source) for a minimum width (2 $\mu$m) transistor are 1.2 $C_{\text{unit}}$ and 0.2 $C_{\text{unit}}$, respectively. The contribution of a gate-to-source capacitance is directly added to the gate node. The contribution of a gate-to-drain capacitance is calculated in two ways. First, if the gate transition directly leads to a drain transition, its contribution is multiplied by a factor of four before added to the gate node since it is not only discharged but also recharged oppositely (a factor of two), and such a discharge-recharge happens every transition, not every two transitions (another factor of two). Second, if the gate transition does not lead to a drain transition, its contribution is directly added to the gate node. The total dynamic power dissipation $P_d$ normalized by $V_{dd}^2 f_c / C_{\text{unit}}$, where $V_{dd}$ is the power supply voltage and $f_c$ is the clock frequency, is then calculated (not simulated) by $P_d = \Sigma\ A_i S_i^2 C_i$, where $i$ is the node number and $C_i$ is the normalized node capacitance ($C/C_{\text{unit}}$).

Worst delays (WD), the larger one between propagation delays of p-latch (P) and n-latch (N) calculated from clock edges to data transitions at 50% points with $V_{dd} = 5$ V, normalized power dissipations (NP) and transistor counts (CT-clocked, T-total) are listed in Tables I–IV for the nondifferential dynamic, the differential dynamic, the semistatic, and the fully static flipflops (groups 1–4), respectively. Their power-delay products are plotted in Figs. 21–24, respectively. New flipflops are marked by †. The classic master-slave flipflop (no. 19) is fully static and formed by four transmission gates, four inverters, and a clock buffer to offer two-phase clocks internally [8]. A clear tendency is that the new flipflops

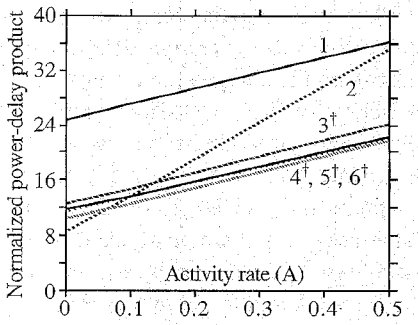


Fig. 21. Power-delay products of group 1.

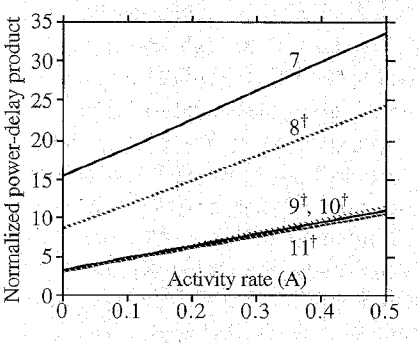


Fig. 22. Power-delay products of group 2.

are obviously faster and consume less power, which means significant improvements of power-delay-products. The new flipflops use fewer clocked transistors. In the new high-speed differential flipflops, logic-related transistors in both p-latches and n-latches are n-type, giving high logic operating speed to the circuit when logic is included in the flipflops.

## IX. CONCLUSIONS

In the proposed new TSPC flipflops, speed and power bottlenecks of the original TSPC and the existing differential

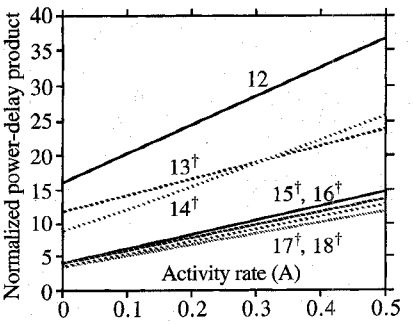


Fig. 23. Power-delay products of group 3.

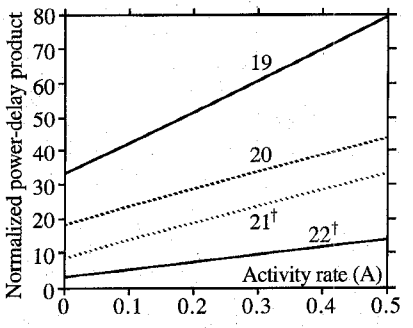


Fig. 24. Power-delay products of group 4.

flipflops are either alleviated or removed. In the best cases, delays are reduced by factors of 1.3, 2.1, 2.2, and 2.4 for the nondifferential dynamic, the differential dynamic, the semistatic, and the fully static flipflops, respectively. In the same time, power consumptions are also reduced compared to their original counterparts so the power-delay products are reduced by factors of 1.9, 3.5, 3.4, and 6.5 for an average activity ratio (0.25), respectively. Particularly, the new differential dynamic, semistatic, and fully static flipflops (Numbers 11, 17, 18, and 22 in the tables) are considerably superior in both speed and power saving.

Of course, the results are obtained by assuming differential outputs. When only a single output is needed, delays of the original TSPC nine-transistor flipflop [2] and the new nondifferential flipflops (no. 3–no. 6 with output inverters removed) are comparable to that of the new differential flipflops. However, the differential ones are completely nonprecharged, thus using less power. Moreover, the clock loads of the new differential flipflops are reduced or minimized, which allows smaller clock drivers reducing area and the total power consumption.

The new static flipflops (no. 17, no. 18, and no. 22) proposed here are well suited to replace existing types based on the classic master-slave flipflop [8] in standard cell libraries and full custom applications, resulting in high speed, power savings, and lower clock load. For highly pipelined structures, logic is integrated into latches. A unique feature of the proposed high-speed flipflops is then that the logic-related transistors are purely n-type in both n-latches and p-latches. This means that all logic operations can be done completely by n-transistors, which gives an additional speed advantage to this kind of CMOS circuits.

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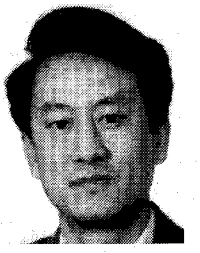

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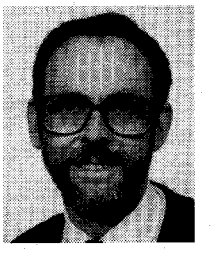

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