

Digital-to-Analog conversion

This worksheet and all related files are licensed under the Creative Commons Attribution License, version 1.0. To view a copy of this license, visit <http://creativecommons.org/licenses/by/1.0/>, or send a letter to Creative Commons, 559 Nathan Abbott Way, Stanford, California 94305, USA. The terms and conditions of this license allow for free copying, distribution, and/or modification of all licensed works by the general public.

Resources and methods for learning about these subjects (list a few here, in preparation for your research):

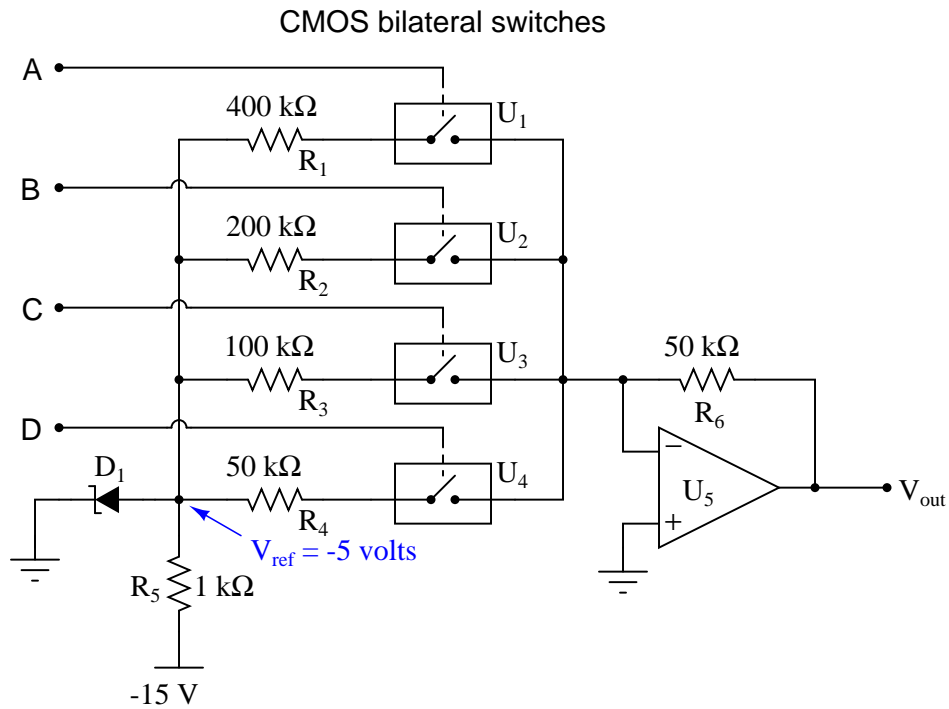
Questions

Question 1

Explain what the purpose of a *digital-to-analog converter*, or *DAC* circuit is, in your own words.
file 03997

Question 2

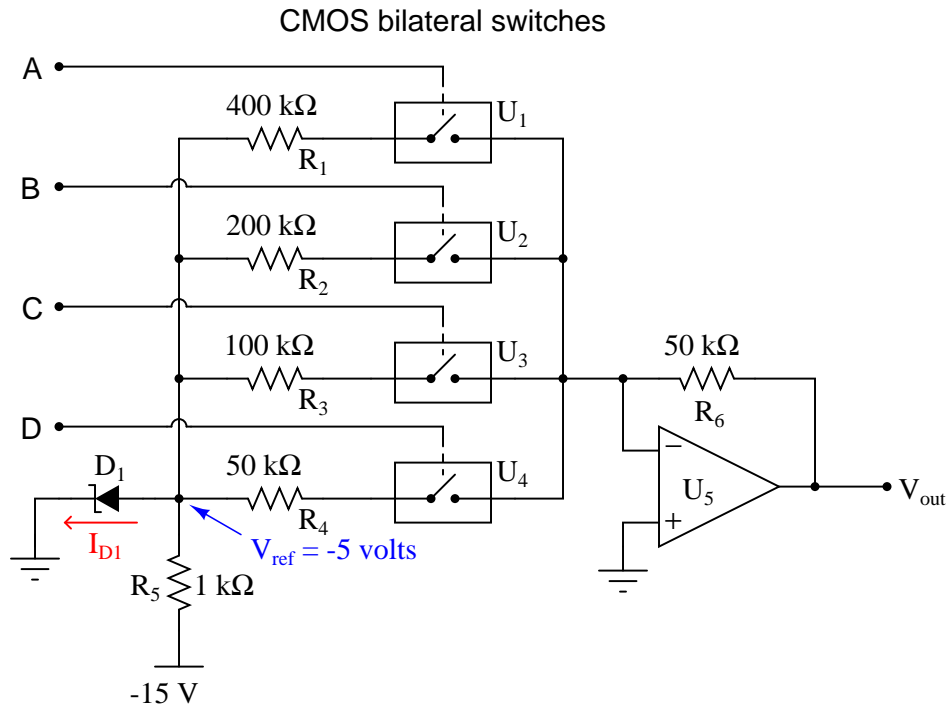
Explain how this *digital-to-analog converter* (DAC) circuit is supposed to function:



file 03996

Question 3

This *digital-to-analog* converter (DAC) circuit takes a four-bit binary input (input terminals A through D) and converts it to an analog voltage (V_{out}). Predict how the operation of this circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):

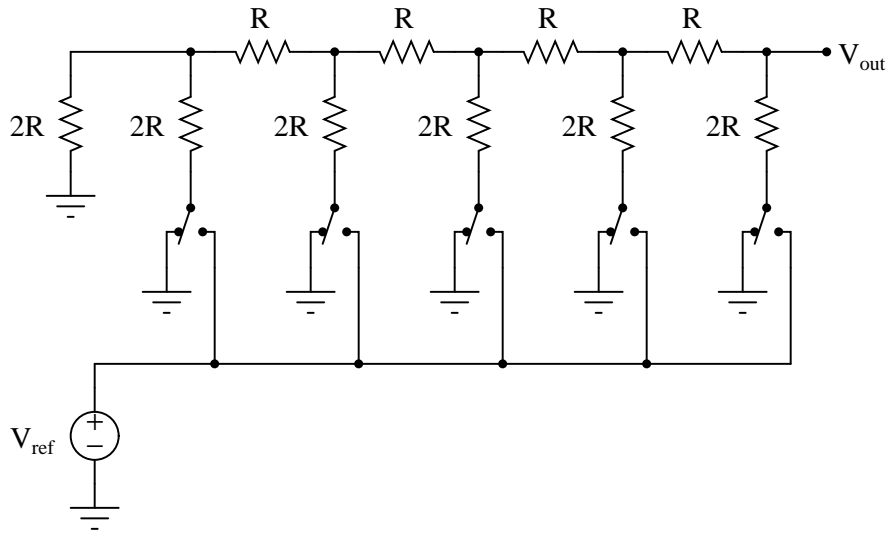


- Bilateral switch U_1 fails open:
- Zener diode fails shorted:
- Solder bridge (short) past resistor R_1 :
- Resistor R_6 fails open:

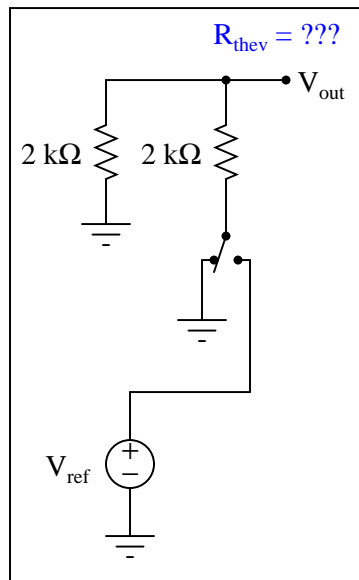
file 03849

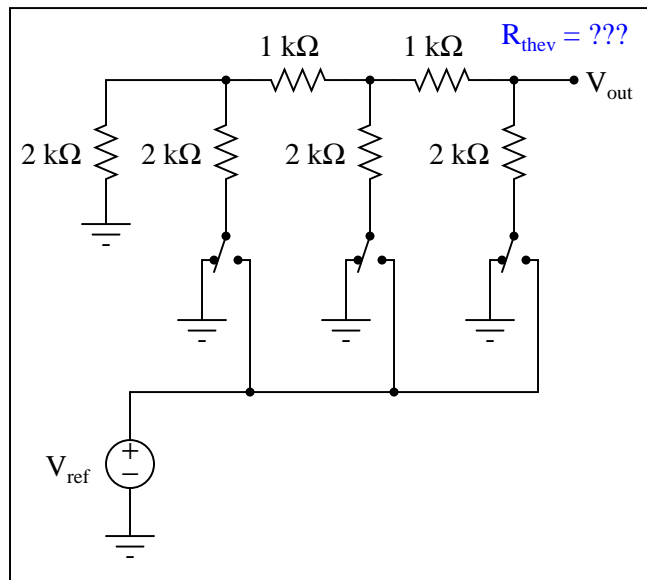
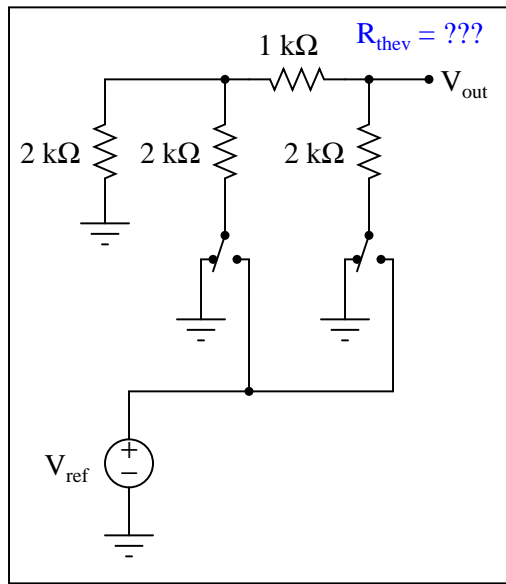
Question 4

A type of resistor network known as an R - $2R$ ladder is often used in digital-to-analog conversion circuits:



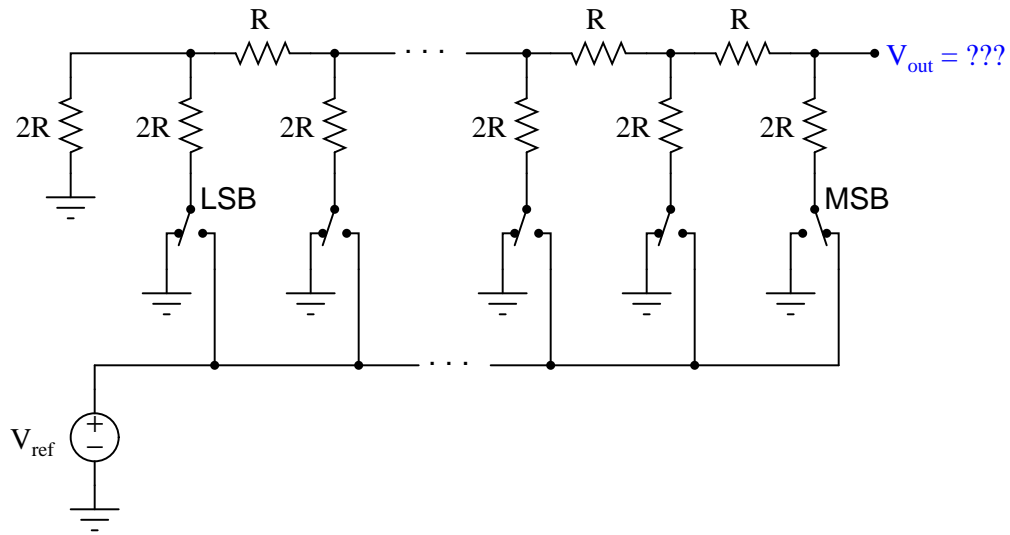
When all switches in the R - $2R$ ladder are in the "ground" position, the network has a very interesting property regardless of its size. Analyze the Thévenin equivalent resistance (as seen from the output terminal) of the following R - $2R$ ladder networks, then comment on the results you obtain:





Question 5

When only the most significant bit (MSB) of an R-2R ladder resistor network is activated (all other bits inactive, their switches connecting to ground), the output voltage will be the same, regardless of how many bits the network has:

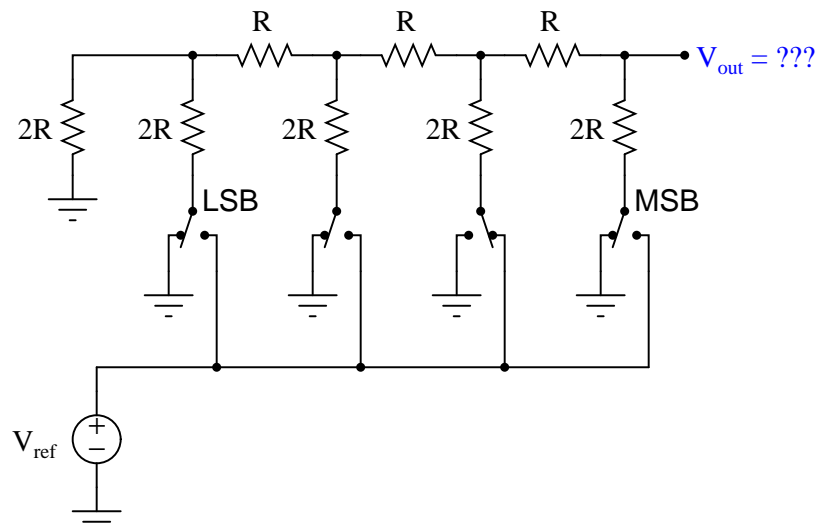


Explain why this output voltage magnitude stands independent of the number of bits (sections) in the R-2R ladder network.

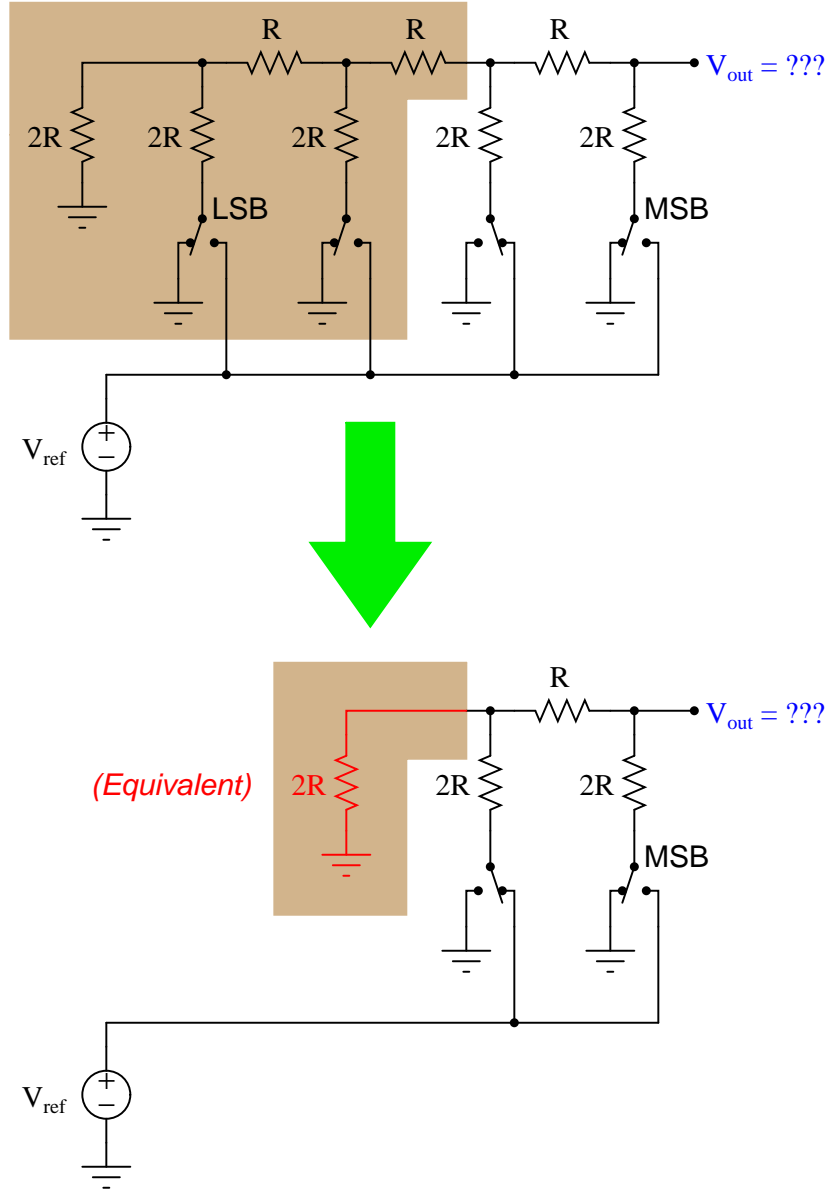
file 04000

Question 6

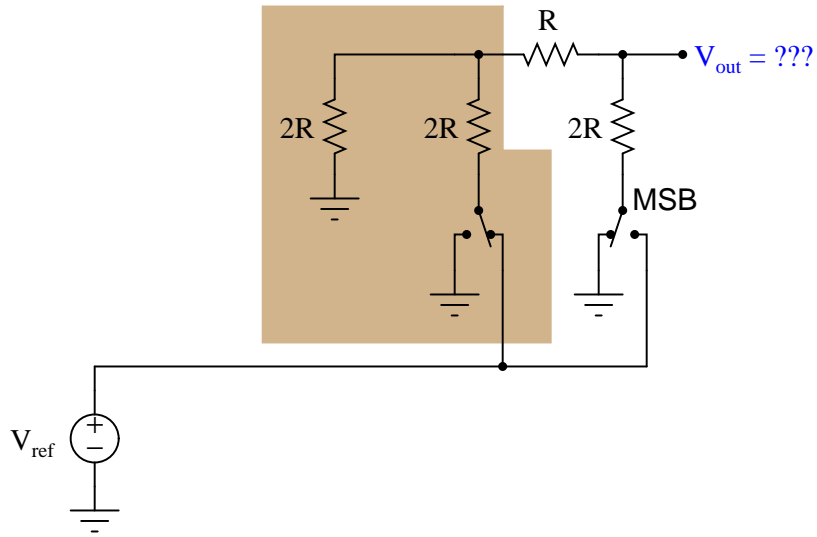
Thévenin's theorem is a powerful tool for analyzing R-2R ladder networks. Take for instance this four-section network where the next-to-most-significant "bit" is activated, while all the other "bits" are inactive (switched to ground):



If we Thévenize all sections to the left of the activated section, replacing it with a single resistance to ground, we see the network becomes far simpler:



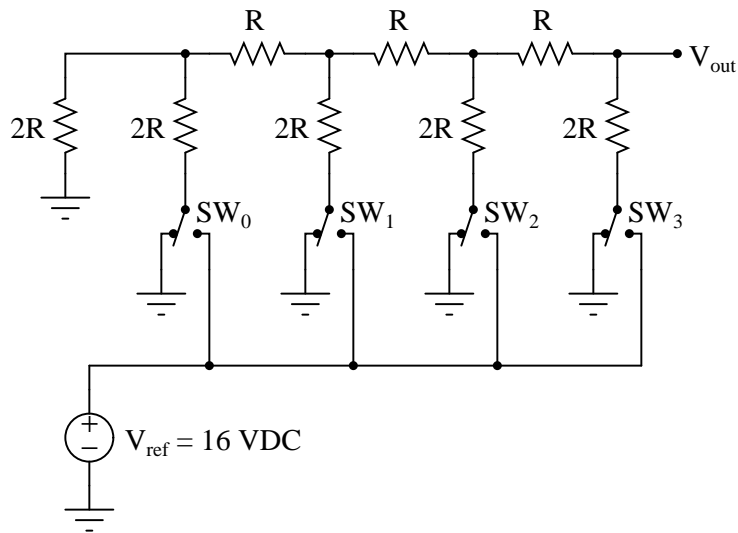
Explain how we may apply Thévenin's theorem once again to the shaded section of this next circuit (simplified from the previous circuit shown above) to simplify it even more, obtaining a final result for V_{out} :



file 04001

Question 7

Determine the voltage output by the following R-2R ladder network given the switch states shown in the table:



SW ₀	SW ₁	SW ₂	SW ₃	V _{out}
Ground	Ground	Ground	V _{ref}	
Ground	Ground	V _{ref}	Ground	
Ground	V _{ref}	Ground	Ground	
V _{ref}	Ground	Ground	Ground	
Ground	Ground	Ground	Ground	

file 04007

Question 8

Explain why DAC circuits based on R-2R ladder networks are more popular than binary-weighted resistor networks. Either one will work well if properly designed and built, so why would one design be more widely manufactured?

[file 04009](#)

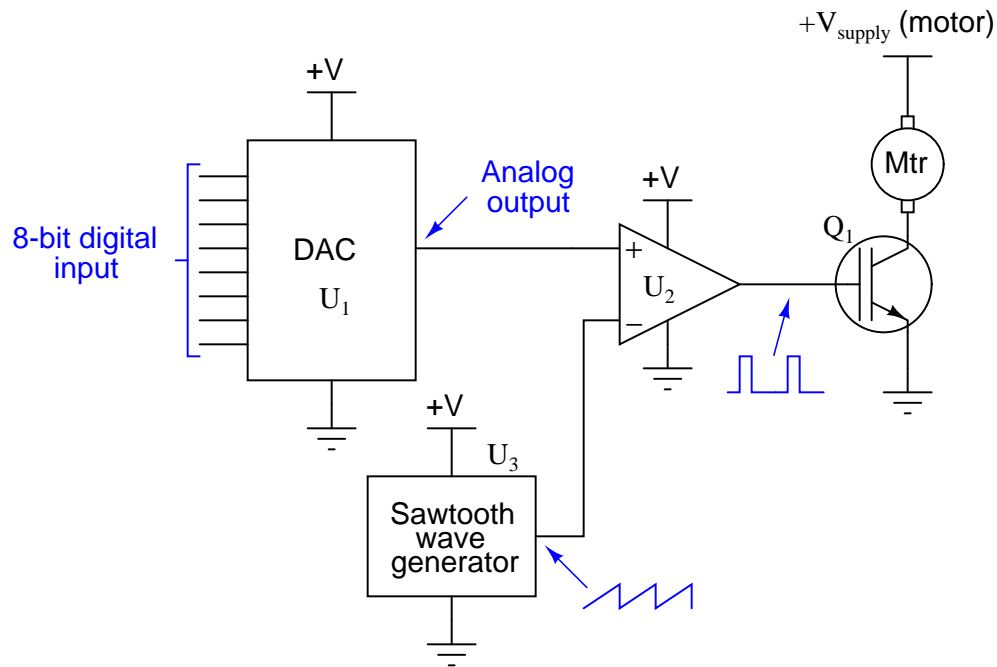
Question 9

Explain what a *digital potentiometer* is, and give one example of a digital potentiometer in integrated-circuit (IC) form.

[file 02817](#)

Question 10

This is a digitally-set motor speed controller circuit, using PWM to modulate power to the motor. Predict how the operation of this circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):

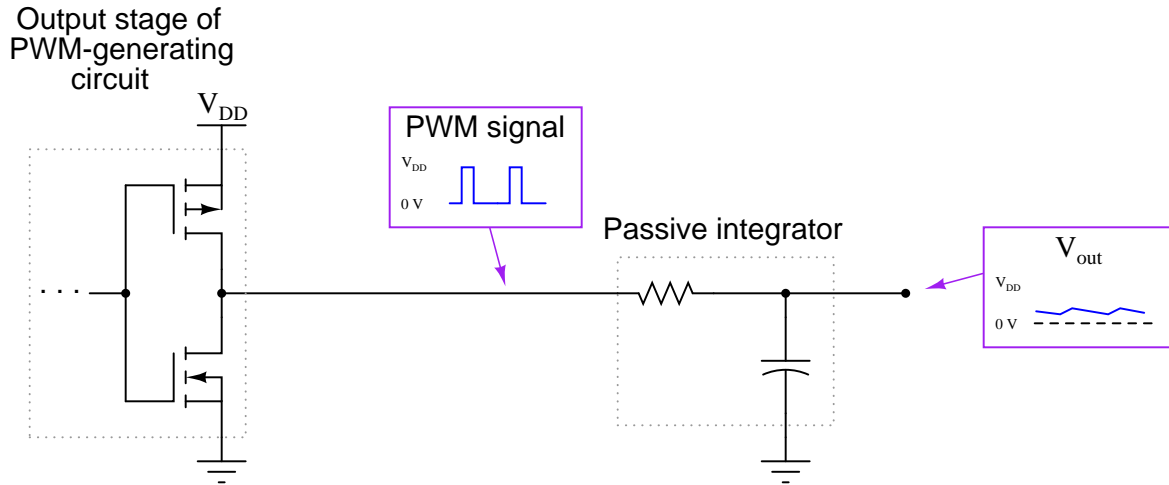


- DAC output fails low (output = 0 volts DC):
- DAC output fails high (output = +V):
- IGBT Q_1 fails open (collector to emitter):
- Solder bridge (short) between MSB input on U_1 and ground:

[file 03850](#)

Question 11

If a pulse-width modulated (PWM) signal is sent to a passive integrator circuit from a circuit capable of both sourcing and sinking current (as is the case with the dual-MOSFET output stage), the output will be a DC voltage (with some ripple):

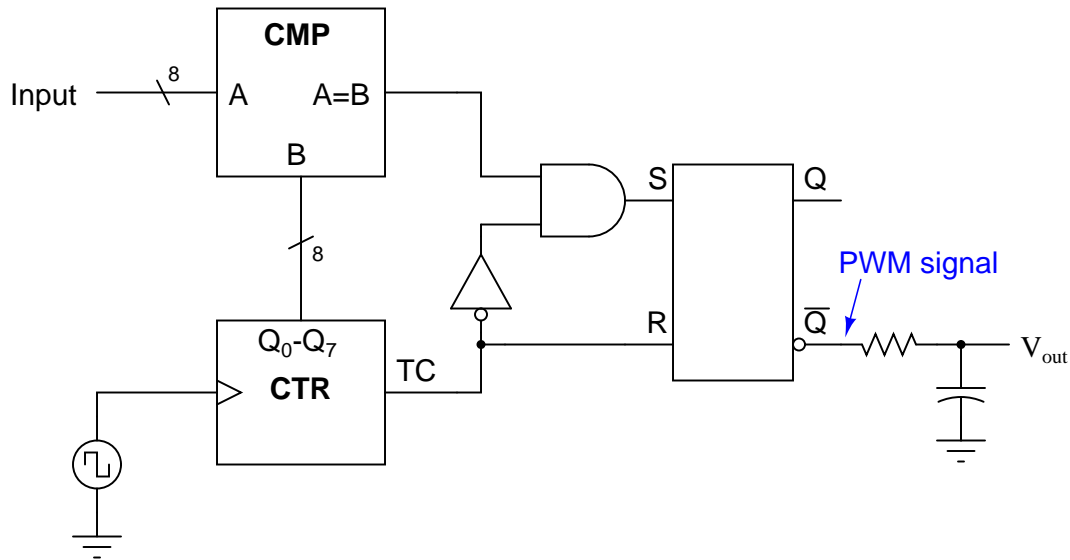


Determine the relationship between the PWM signal's duty cycle and the DC voltage output by the integrator. What does this suggest about PWM as a means of communicating information, such as analog data from a measuring device?

[file 02156](#)

Question 12

The following circuit generates an analog output voltage proportional to the value of the binary input, using pulse-width modulation (PWM) as an interim format. An eight-bit binary counter (**CTR**) continually counts in the "up" direction, while an 8-bit magnitude comparator (**CMP**) checks when the 8-bit binary input value matches the counter's output value. The AND gate and inverter simply prevent the S-R latch from being "set" and "reset" simultaneously (when both A and B are maximum, both at a hex value of \$FF), which would cause the output to be "invalid" when S and R were both active, and unpredictable when both S and R inputs returned to their inactive states:



Explain how this circuit works, using timing diagrams if necessary to help show the PWM signal at \bar{Q} for different input values.

[file 03998](#)

Question 13

What is meant by the word *resolution* in reference to an ADC or a DAC? Why is resolution important to us, and how may it be calculated for any particular circuit knowing the number of binary bits?

[file 04008](#)

Answers

Answer 1

The most basic definition for this device should be obvious: a circuit that takes a digital input and creates an analog output. What I'm looking for, though, is something a little less obvious. In your own words, explain what it means for a circuit to have a "digital input" and an "analog output." You may give an example of such a circuit if you find it easier to answer the question in context.

Answer 2

I'll let you figure out the operation of this circuit on your own!

Answer 3

- Bilateral switch U_1 fails open: V_{out} same for all odd numbered input conditions as it is for next lowest even-numbered input condition (e.g. input value of 5 gives same output as input value of 4).
- Zener diode fails shorted: V_{out} is nearly zero volts for any input condition.
- Solder bridge (short) past resistor R_1 : V_{out} saturates positive for any given odd-valued input condition.
- Resistor R_6 fails open: V_{out} always saturated.

Follow-up question #1: is the arrow showing zener diode current drawn in the direction of electron flow or conventional flow?

Follow-up question #2: which input bit is the most significant (MSB) and which is the least significant (LSB)?

Answer 4

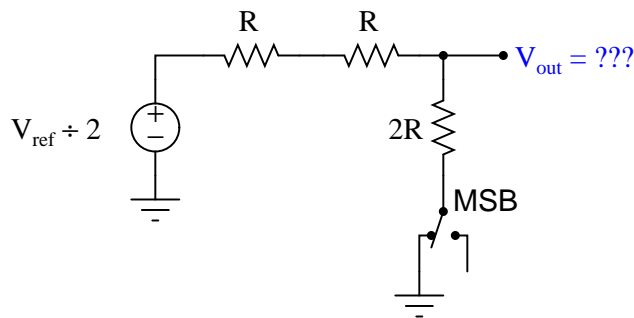
Did you honestly think I'd do all the work for you and just give you the answer?

Answer 5

$$V_{out} = \frac{V_{ref}}{2}$$

Answer 6

Once you get to this point, solving for V_{out} in terms of V_{ref} is trivial:



Answer 7

SW_0	SW_1	SW_2	SW_3	V_{out}
Ground	Ground	Ground	V_{ref}	8 volts
Ground	Ground	V_{ref}	Ground	4 volts
Ground	V_{ref}	Ground	Ground	2 volts
V_{ref}	Ground	Ground	Ground	1 volt
Ground	Ground	Ground	Ground	0 volts

Follow-up question: the fact that an R-2R resistor network is inherently linear, we may readily apply the *Superposition Theorem* to figure out what happens when more than one switch is moved to the V_{ref} position. Explain how you would apply Superposition to determine all output voltages for all possible combinations of switch positions.

Answer 8

The answer to this question has to do with business and production-line priorities. Just because two designs work equally well in theory does not mean they are equally easy to mass-produce!

Answer 9

Analog Devices manufactures a 64-position digital potentiometer under the part number AD5227, for example. This is by no means the only digital potentiometer in production!

Follow-up question: would you classify a digital potentiometer as an ADC (analog-to-digital converter) or as a DAC (digital-to-analog converter)?

Answer 10

- DAC output fails low (output = 0 volts DC): *Motor will not run.*
- DAC output fails high (output = +V): *Motor runs full speed all the time.*
- IGBT Q_1 fails open (collector to emitter): *Motor will not run.*
- Solder bridge (short) between MSB input on U_1 and ground: *Speeds 0 through 127 work normally, but speeds 128 through 255 just duplicate speeds 0 through 127, respectively.*

Answer 11

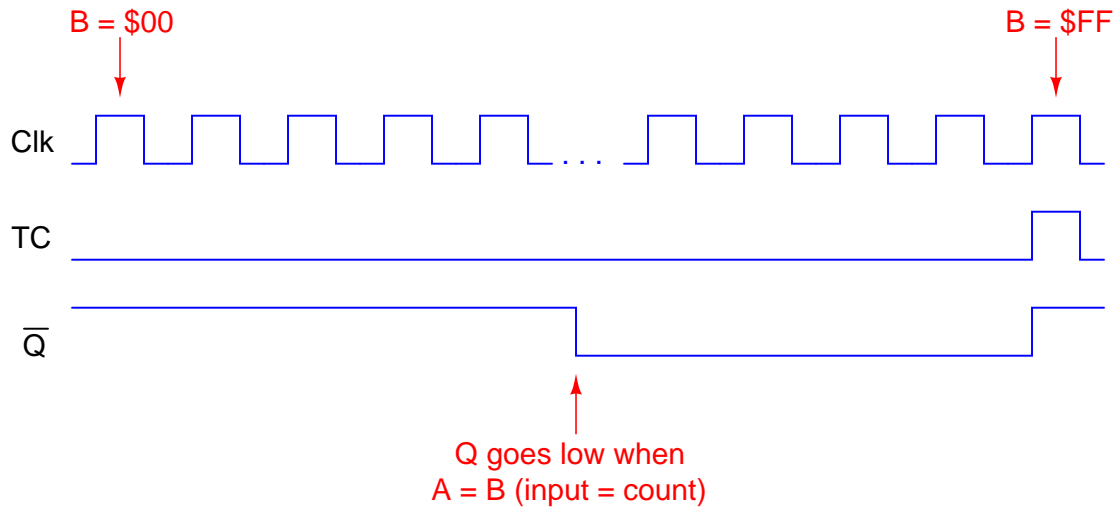
There is a direct-proportional relationship between duty cycle and DC output voltage in this circuit, making it possible for a PWM signal to represent analog data.

Follow-up question #1: why is it important that the circuit generating the PWM signal for the integrator be able to both source *and* sink current?

Follow-up question #2: what would have to be done to reduce the ripple voltage at the integrator's output?

Answer 12

Here is a timing diagram to help get you started on a complete answer:



I'll leave it to you to explain the relationship between the input value (A), the PWM duty cycle, and the analog output voltage.

Answer 13

The *resolution* of either a digital-to-analog converter (DAC) or an analog-to-digital converter (ADC) is the measure of how *finely* its output may change between discrete, binary steps. For instance, an 8-bit DAC with an output voltage range of 0 to 10 volts will have a resolution of 39.22 mV.

Notes

Notes 1

Informational sources abound which your students can research. Be sure to ask them to answer specifically, explaining what it means for a circuit to have a "digital input" and an "analog output."

Notes 2

This question is a good review of op-amp theory, especially for students who might not have studied operational amplifiers in a while.

Notes 3

Questions like this help students hone their troubleshooting skills by forcing them to think through the consequences of each possibility. This is an essential step in troubleshooting, and it requires a firm understanding of circuit function.

Notes 4

The answer is not difficult to obtain if you use each Thévenin equivalent resistance to model the left-hand portion of each successive R-2R ladder network as they become more complex! Those students who do not take this problem-solving step are doomed to perform a *lot* of series-parallel calculations!

Notes 5

The key to understanding the answer is to apply Thévenin's theorem to the "inactive" sections of the network. Here, the unique property of constant output impedance for an R-2R network yields a useful feature when applied to DAC circuitry.

Notes 6

Students might not realize it is valid to iteratively apply Thévenin's theorem to the solution of a circuit problem. You can, and this stands as a good example of how (and why!) you should do it.

Notes 7

As you can see, the reference voltage value of 16 volts was not chosen at random! I wanted students to see the pattern between single switch closures and binary place-weights for a four-bit number. The actual electrical analyses for each condition are best expedited by applying Thévenin's theorem repeated to the circuit, condensing sections to single resistances and voltage sources until a simple voltage divider circuit is obtained at the output terminal.

The follow-up question is quite important. Be sure to ask your students about it, for it holds the key to figuring out all output voltage values for all binary input possibilities.

Notes 8

It is important for your students to grasp basic principles and practices of business, because that is the arena their technical skills will most likely find challenge and value. This question is a way to get your students thinking about real-life, practical manufacturing concerns that go beyond basic principles of electrical theory.

Notes 9

Rarely is the digital potentiometer mentioned in introductory textbooks as a digital-to-analog converter device, but it is!

Notes 10

Questions like this help students hone their troubleshooting skills by forcing them to think through the consequences of each possibility. This is an essential step in troubleshooting, and it requires a firm understanding of circuit function.

Notes 11

Although it should not be difficult for students to discern the relationship between duty cycle and DC output voltage, the application of this relationship to data communication might be difficult for some students to grasp, especially on their own. Further elaboration on your part may be necessary.

An excellent example of this principle applied is the generation of an analog voltage by a 1-bit digital circuit. This technique is useful in microcontroller systems where output ports may be scarce, provided that ripple voltage (or slow response) is not a problem.

Notes 12

This circuit provides students with an interesting exercise in timing analysis, as well as being a simple means of converting large binary values into analog output voltages without resorting to using *large* resistor networks.

Notes 13

Note that I did not hint how to calculate the resolution of a DAC or an ADC, I just gave the answer for a particular example. The goal here is for students to inductively "work backwards" from my example to a general mathematical statement about resolution.

There are actually two different ways to calculate the resolution, depending on the actual range of the converter circuit. For the answer given, I assumed that a digital value of $0x00 = 0.00$ volts DC and that a digital value of $0xFF = 10.00$ volts DC. If a student were to calculate the resolution for a circuit where $0xFF$ generated an output voltage just shy of 10.00 volts DC (e.g. an R-2R ladder network where $V_{ref} = 10$ volts DC, and a full-scale binary input generates an output voltage just one step less than V_{ref}), the correct answer for resolution would be 39.06 mV.

You may want to bring up such practical examples of resolution as the difference between a handheld digital multimeter and a lab-bench digital multimeter. The number of digits on the display is a sure clue to a substantial difference in ADC resolution.