Accellera C Standard Group Meeting

August 3rd 2000
@ Intel Santa Clara CA

Attendees:
Brian Bailey Mentor Graphics Chair
Daniel Gajski UCI CoChair
Asa Ben Tzur Intel
Joe Daniels - phone
John Sanguinetti
David Springer
Peter Flake - phone
Paula Menzigian
Martin Baynes
Frederic Doucet Intel / UCI

Books brought by Dan Gajski:

Algorithmic and Register Transfer Level synthesis: The System Architect's Workbench D.E. Thomas, E.D. Lagnese, R.A. Walker, J.A. Nestor, J.V. Rajan, R.L. Blackburn

High-Level Synthesis. Introduction to Chip and System Design Daniel Gajski, Nikil Dutt, Allen Wu, Steve Lin

The Synthesis Approach to Digital Design. Edited by Petra Michael, Ulrich Lauther, Peter Duzy

High Level Synthesis of ASIC's Under Timing and Synchronization Constraints. David C. Ku, Giovanni De Micheli

Behavioral Synthesis and Component Reuse with VHDL Ahmed Amine Jeraya, Hong Ding, Polen Kission, Maher Rahmouni

Behavioral Synthesis. Digital System Design Using the Synopsys Behavioral Compiler. David W. Knapp

Principles of Digital Design Daniel Gajski

Meeting Convened at 9:00

Joe reported that Accellera/OVI had confirmed continued funding for Joe so that he would be available for documentation work.

Minutes from previous meeting. Since Kevin was not present this could not be fully discussed but the group felt that it was good to leave both views in the minutes. Dan Gajski said that while it was probably premature to consider the long term position with the SpecC consortium, he thought it would be a good idea for me to formally invite them to join the group and to participate.

ALC update. There had been a lot of confusion surrounding Vassilios's activities and he was expected to be at this meeting to respond to requests for a full description of the ALC and its activities. However, his travel plans had not included this meeting, so Brian and Martin gave a brief description. One item that did emerge from this is that since Joe is now available for Accellera work, it was suggested that he could start making the changes discussed in the previous ALC meeting. He was to pick up an annotated copy of the documents from Martin.

Review of previous Action Items:

- **A-1** The chair should establish and maintain two reflectors. One for active members and one for audit members. Both of these lists should be managed as described above. Brian Bailey.
  Action Completed. The new list for active members is also archived on the web site. The audit members will continue using the existing audit list.

- **A-2** The chair should establish and maintain a web site contained the above specified documents. If Accellera cannot provide this in a timely fashion (within 2 weeks) a temporary site will be created and hosted by C-Level Design. Brian Bailey & Dennis Brophy.
  Action Completed. The new web site is at www.eda.org/alc-cwg

- **A-3** A formal charter for the group needs to be written and balloted. Brian Bailey
  Action Completed. Two changes were requested in the proposed charter. These changes were made and the group approved the charter by a unanimous vote after.

- **A-4** Accellera tasked Kevin Kranen (System C) to meet with the Open SystemC steering committee and discuss possible areas of collaboration, e.g. critique of proposals/technology & possible future closer collaboration.
  Action Completed. Kevin sent email 7/5/2000. Grant, Vassilios and I did go back and begin the process of working out what kind of formal collaboration might benefit both SystemC and Accellera. Bottom line - Steering Group believes that we should at least have simple asynchronous information exchange in place, similar to that that has produced successful results with VSIA SLD. Both groups provide key contact people for sharing information asynchronously, and for working through technical questions/issues to get alignment. We didn't have a chance to go any further in this in 6/29 Steering Group meeting.

- **A-5** Accellera tasked Prof Gajski (Spec C) to talk to the SpecC consortium and have similar discussions to action A-4.
  Action Completed. Dan has talked to the consortium and reported that they are interested in the Accellera effort. New action created to send formal invitation for participation.

- **A-6** Need to establish a viable licensing mechanism with Accellera. Dennis
  Open. While I have talked to Dennis regarding the importance of this, they are still trying to create the official Accellera entity and will not be able to get to this immediately.

- **A-7** Need to re-establish the role and charter of the ALC and it interaction with sub-groups. Also look into the best working structure for the ALC. Brian Bailey and Vassillios Gerousis.
  Open. It remains unclear how the ALC will operate going forward and the outcome of the DCDN semantics.

- **A-8** Establish a working group to define RTL semantics (in Verilog, VHDL) – Dan G to recommend a book – due week of July 3rd.
  Action Completed. The relevant section of the book is available on the web site. Dan also brought along a number of other book on the subject, a full list appears at the top of these minutes. The working group will meet in August.

- **A-9** Find out common subset & document differences in existing models – an expert from each company to meet (SystemC, CynApps, C Level, with reference to Verilog, VHDL) – e.g. to define how interact with Verilog or VHDL model. Meet next week, Kevin (contact point), John (contact point), Martin (contact point).
  Open. This will be the topic of the next meeting.

Other Discussion Items.
Brian reported that in a conversation with Dennis, that voting rights as described may not completely fit within the allowable framework of OVI/Accellera. However the group felt that since non-Accellera members were making such an important contribution, that it was necessary for the group to treat them as first class citizens. We have thus agreed that we do not ‘vote’ on things, we reach consensus according to

the ‘voting rules’ that we have established and then when necessary we will forward our recommendation to the ALC, or formal OVI/Accellera voting mechanism for approval.
We also discussed the role of audit members and inactive members. It was decided to create a third class of person. Those that did not have voting rights (because of lack of active participation) but would have access to all of the internal documentation. It was agreed that both Chris Lennard and Joe Daniels should both be elevated to this status.

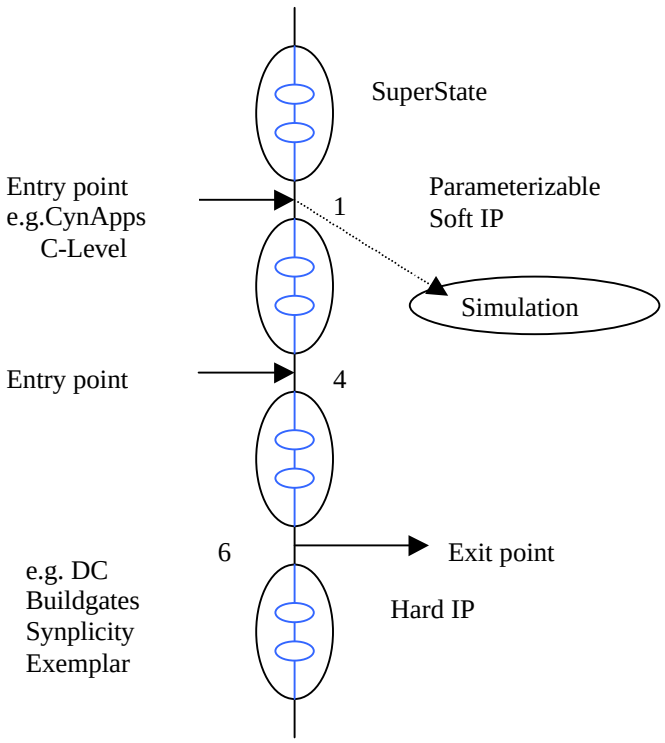
Dan Gajski. Presentation of the RTL Semantics
A lot of discussion centered on what is RTL, what is Boolean optimization and what is at the higher level. Arbitrary lines were drawn on Dan’s 5 stages between 1 and 2 and then between 3 and 4. Above level 1 there is no specific clock but a synchronization event. Dan’s superstate category is above level 1. Above the superstate you also lose the state machine and you are at pure C. Martin said there are different levels required of Superstate that include unclocked and clocked which means that the ‘C’ has been allocated to clock cycles. This is where we want to get to, but for now have to deal with the things below. So 1 is the highest point we will consider at this time.

At 4 all buses will have the actual implementation clock defined and is a fully defined RTL description. All that is left is Boolean optimization. We as a committee should not define anything below level 5 as this is logic synthesis.
We do limit that at 1 we have the real clock and not a flexible clock. However with a clock it is possible to have a multiple phase clock.

We need to define the points at which we wish to allow interchange to occur. This may not be at all of the defined levels. We know that the output is at the logic synthesis level and is covered by an IEEE standard. It may not fully spell out the semantics as it concentrates on syntax. (Verilog / VHDL)

Asa suggested that as part of this effort, it may become important to define the Verilog and VHDL semantics. This was generally agreed by the committee, but would require more effort than this committee could muster. It would be passed as a suggestion up to the ALC.

It seems that we do need to handle the Behavioral RTL level and in the longer term may need to move to a time partitioned superstate level.
We may need to instead exit at level 4 or 5 for example for an FPGA there is nothing below 4 since an adder for example is an instantiation of a cell. For a full description of the levels refer to Dan’s presentation



Question from John:
When you have a module that is called, should the output port be a deferred or immediate assignment. Dan says that it depends if it is an operator or a storage element. This was seen as being an importantr semantic difference between SystemC and Cynlib and is centered on when and why registers are infered. John felt they should be specifically stated and not left to intepretation. Dan said that any functional block needed to have the ability to output either to a register or provide combinatorial output to be used by either other blocks in the datapath or in the control path.

There are a number of open questions regarding the semantics of communicating FSMD's. This has not been fully discussed.
In RTL is a clock a single event or does it have multiple phases that can be used. It appears to be that at behavioral level there should only be one, but at lower levels of implementation multiple are required so that states can settle.

The meeting concluded by establishing a plan and dates for the next two meetings with the goal of having a draft semantic description available at the end of these meetings.

Dan to write a draft available in 2 weeks.
1 week to review.

Defered Actions

- **A-6** Need to establish a viable licensing mechanism with Accellera. Dennis
- **A-7** Need to re-establish the role and charter of the ALC and it interaction with sub-groups. Also look into the best working structure for the ALC. Brian Bailey and Vassillios Gerousis.
- **A-9** Find out common subset & document differences in existing models – an expert from each company to meet (SystemC, CynApps, C Level, with reference to Verilog, VHDL) – e.g. to define how interact with Verilog or VHDL model. Meet next week, Kevin (contact point), John (contact point), Martin (contact point).

New actions

- **A-10** Formal invitation to the SpecC consortium to join and participate in the Accellera effort. Brian Bailey
- **A-11** Perform modification of SRM documents as discussed in previous ALC meeting. Joe Daniels to get these from Brian and Martin.
- **A-12** Formal invite to Chris and Joe to regsiter. Brian Bailey
- **A-13.** The ALC should consider looking into the incorporation of pure Verilog and VHDL semantics into the SRM. This could possible be farmed out to other groups within Accellera. Vassilios Gerousis.
- **A-14.** Create a draft set of semantics for review by a small working group.
- **A-15.** Small working group to review draft semantics, look at differences between them and internal implementations and report back to the full group.

Next meetings

Working Group meeting August 24th to be hosted by Asa at Intel Representatives from Cynapps, C-Level and SystemC should be present. All others can attend but should be prepared for highly technical exchange.

Full member meeting September 7th to be hosted at Mentor.