C Working Group Meeting October 5th 2000
Mentor Graphics – San Jose

Present
Brian Bailey
Dan Gajski
Dave Springer
Asa Ben-Tzur
John Sanguinetti

Objective of today's meeting.
- Reestablish the high level perspective
- Get a clear understanding of the levels and what this means
- Outline a document covering all of the aspects that we need to deal with.

We had a discussion surrounding the algebraic notation that Martin had started on. We found a number of errors in this. Dan liked the notation, but thought that perhaps we needed to take a step back and look at the big picture.

Dan drew a great table on the board that showed the transformations at each stage. The main point of this is that the semantics do not change and a description can bridge all of the levels. However, if we want to allow interchange, we only permit everything to exist at a single level. A copy of this table was distributed in the meeting and will be transcribed as part of the section writeup for the RTL introduction.

Dwe had a lengthy discussion about if a variable in level 1 is used in more than one state, is it the same variable ? For optimization reasons may want to consider the lifetimes of the variable to see if they can be combined with other variables in a register. If a variable is both used within the same state and in another state then it is both a wire and a register.

In Level 2 we have explicit registers, implicit wires. Temporary variables may still exist but their scope is within that state and cycle only. In fact, all variables, functions etc, should probably be marked with the cycle in which they are true to be complete.

Below is the start of a document outline

RTL semantics
    Functional subset

What is RTL – chapter owner Brian Bailey
        Abstraction levels
        Transformation between levels

FSMD – chapter owner Dave Springer
This is basically what we have been talking about so far
        State Transfers
        Expressions
        Exceptions
                Async reset
                Latches

Communicating FSMD's – chapter owner Dan Gajski
        Ports

Hierarchy

May need to be able to recognize the difference between control and dataports. It may be derivable and would affect the synthesis tools. This was not universally agreed. Need an example to show the need for it. Dan to think about it.
Port – this is a new type along with Wires and Register.
- Behavioral
- Structural

Dan to do a first cut at this

DataTypes
- X, Z ??
- aggregation

Implementations – chapter owner Asa
This may not be a chapter but the information needs to exist somewhere within the document.
Things that the semantics can be used for
- Simulation
- Synthesis
- Spec
- Formal – probably defer
- ATG
- Coverage

Semantics v Syntax
- What we have ignored in the semantics because we feel that it is a syntax issue.

Testing
- Of the design
- Of the semantics

Attributes
We may need to be able connect or reference other facets such as timing, power, constraints etc
Connection points
The only attributes that we should be directly involved with are those than modify functionality. But since this implies a change in the semantics, they cannot be attributes. However, since attributes are so important to the flows and tools, we need to be able to attach them and a mechanism to control the meaning of them. Suggestion XML with a data definition for each domain that it could get used in such a synthesis. Not agreed as a good idea. Needs to be extensible but simple.
**Action – invite Steve Shultz to talk to us about this.

Multiple Clock Domains
- Synchronous
- Asynchronous

An FSMD exists within a single clock domain. When coupling FSMD
There are number of possible relationships.
These need to be enumerated
Does a FIFO create a situation that requires that a single FSMD have multiple clocks. This is used many times for communication between asynchronous systems.

Deliverables
- Reference Manual / implementation
- Semantics Doc

Fit into ALC SRM

Compliance

Restrictions on the bounds of the semantic model. What does it mean to be compliant. We need to create a policy for compliance. In the case of disagreement between the doc and the reference implementation, the document is the master.

Next meeting either 10th or 7th @ CynApps
October 18th for phone conference