Library Characterization and Modeling for 130nm and 90nm SoC Design

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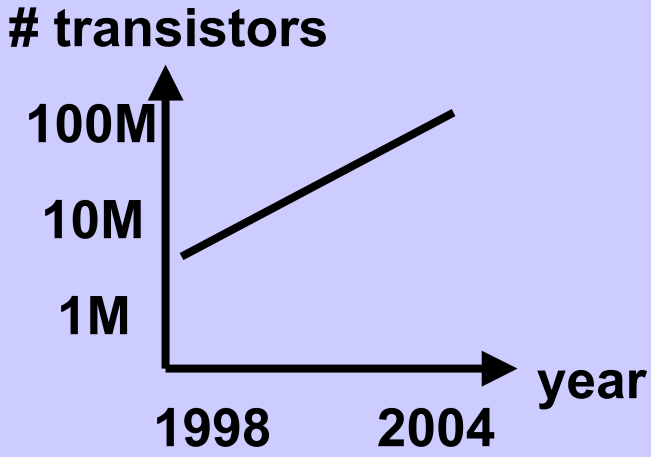
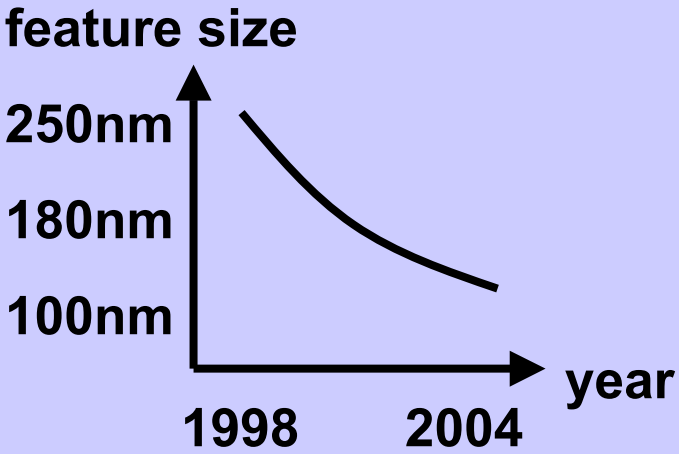
NEC Electronics America

Introduction

Model requirements for system on chip





need more abstraction

Design complexity

Nanometer physics

need more detail

Challenges in System on Chip

- Design complexity
  - Hierarchical design
  - IP cores and macros as building blocks
- Nanometer physics
  - Signal integrity
  - Manufacturability
- Combination of both
  - High performance requirements
  - High power consumption
  - Significant voltage drop

Accurate and efficient library modeling required

Library modeling domains

- Electrical performance modeling
  - Timing, Noise
  - Power, voltage drop
- Reliability
  - Electromigration, hot electron
- Manufacturability
  - Process antenna, Metal density
  - Design rules for sub-wavelength patterns

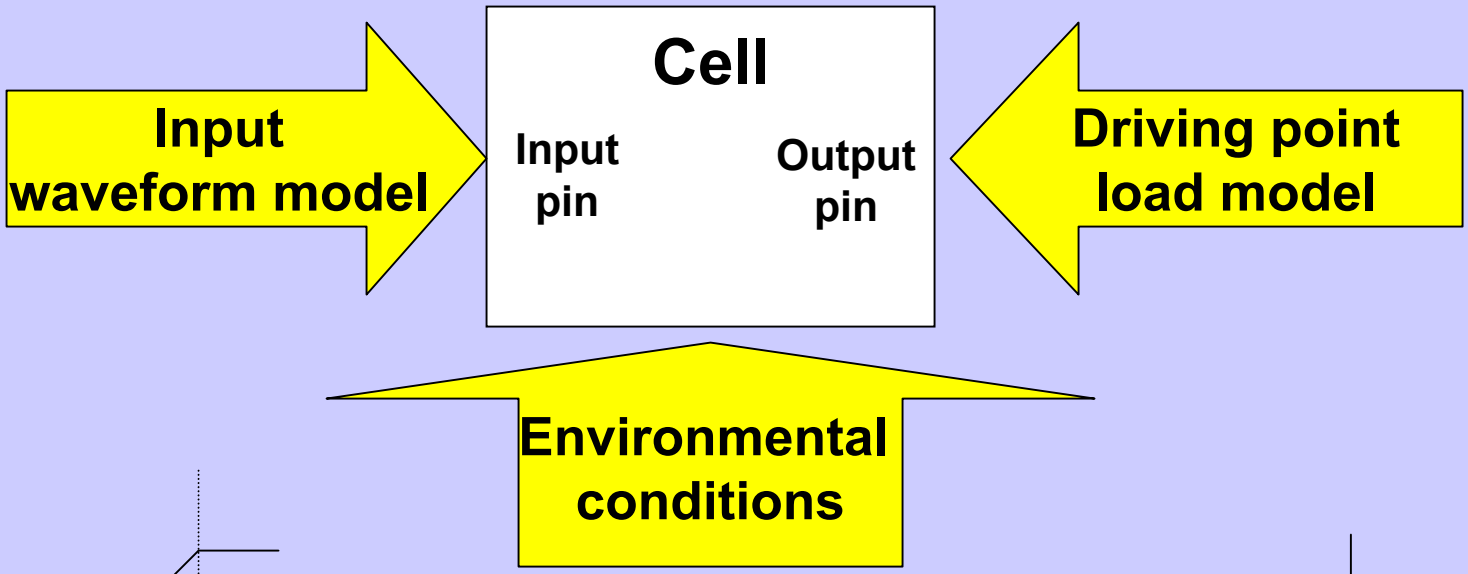
Library modeling formats

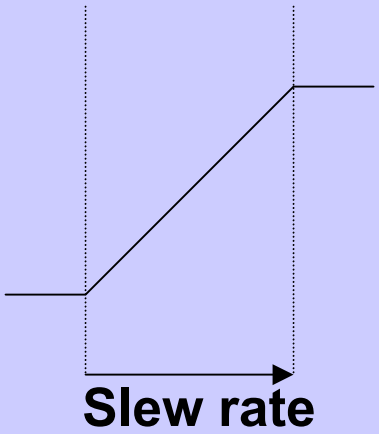
- .lib from Synopsys
  - Predominantly used in the industry, but does not cover all modeling domains
  - Many EDA vendors invent customized extensions or even new tool-specific library formats
- IEEE 1603-2003 Advanced Library Format (ALF)
  - Approved by IEEE on Sept. 11 2003
  - Supports all modeling domains
  - Will be sparingly used in this tutorial to explain new modeling concepts

Timing modeling

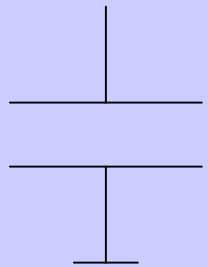
- Characterization conditions are idealized
  - Input waveform is linear ramp
  - Output load is lumped capacitance
  - PVT is constant
- Issues
  - Characterization for variable PVT
  - Need to consider non-linear waveform
  - Need to consider distributed load
  - Interdependency between cell timing and interconnect timing

Timing characterization





Discrete process corner
Supply voltage = constant
Temperature = constant

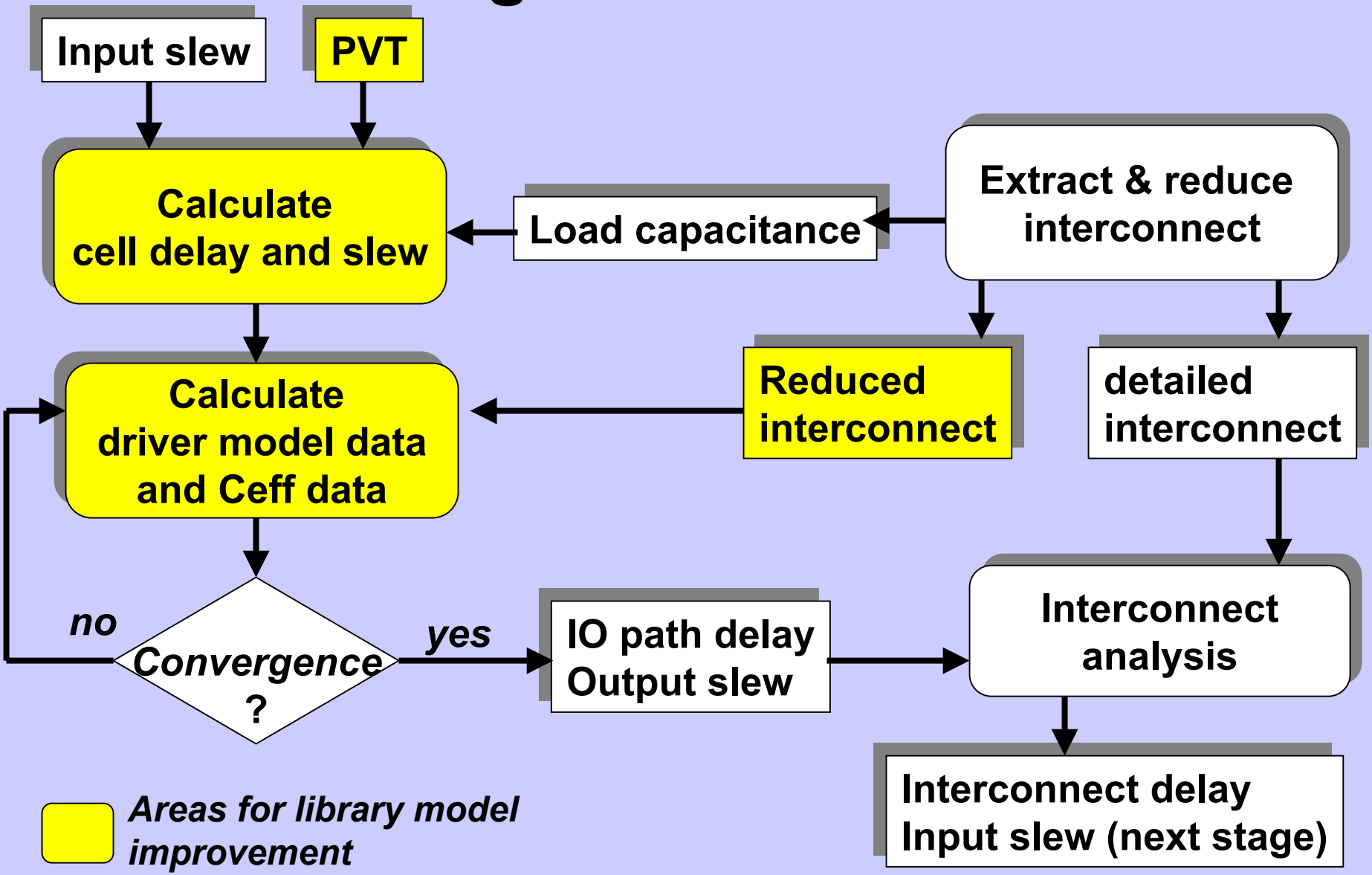


Delay (input to output) & Slew rate (output)
= f (Slew rate (input), Load capacitance) @ constant PVT

Characterization with variable PVT

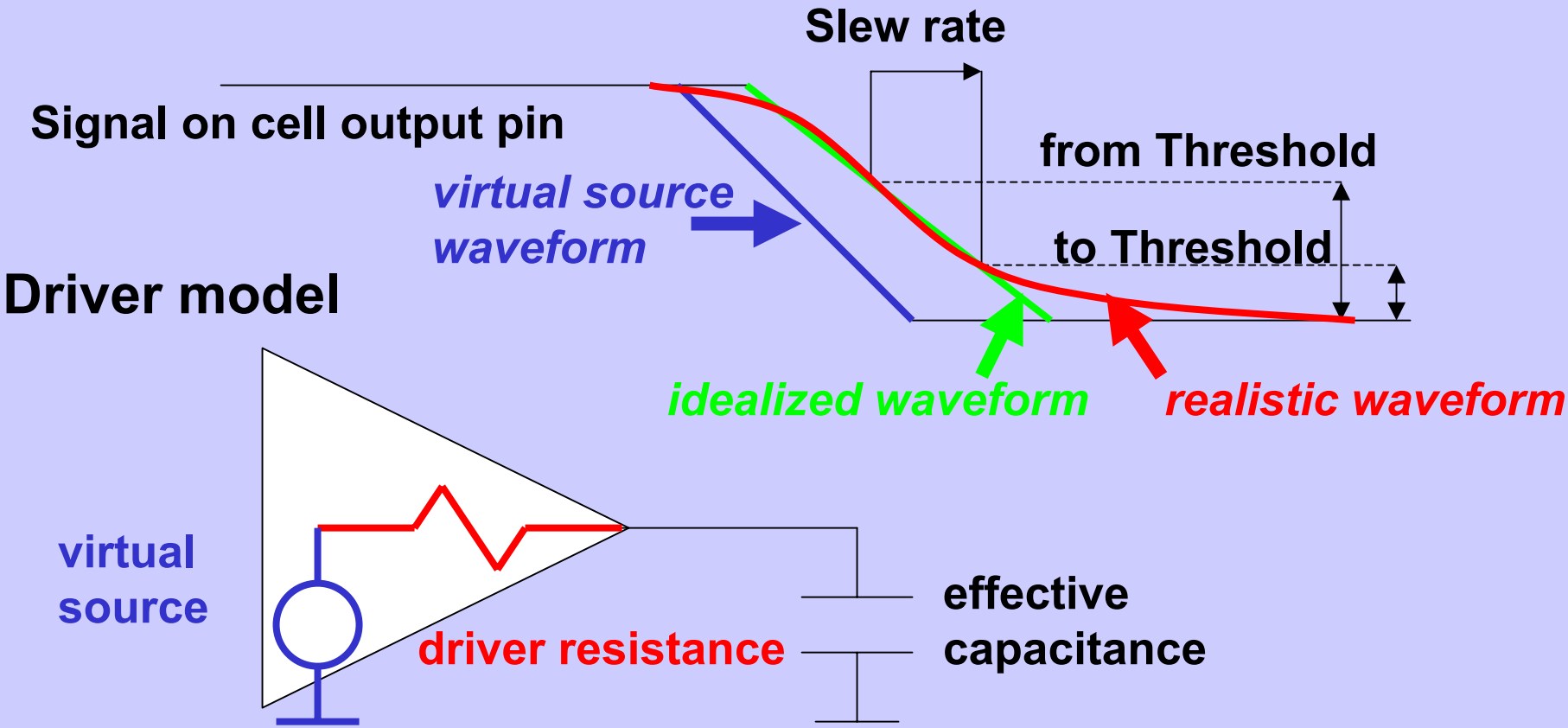
- Low effort
  - Calculate derating factors by sparse characterization for P, V, T as independent variables
- Medium effort
  - Characterize entire library for selected set of PVT conditions (e.g. best, normal, worst)
  - Apply derating factors at each condition
- High effort
  - Characterize entire library with P, V, T as independent dimensions

Timing calculation flow



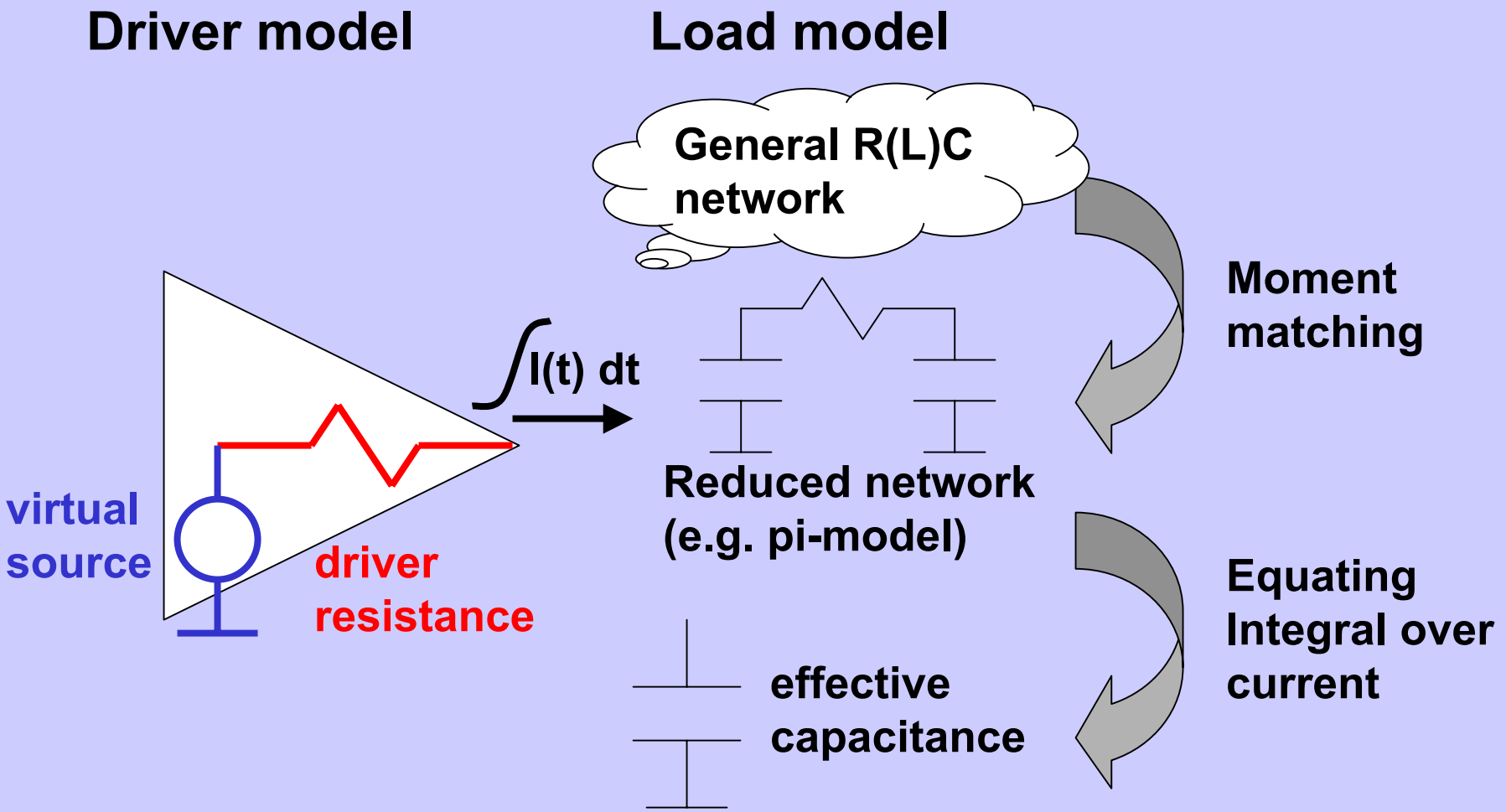
Non-linear waveform

- Linear slew rate not accurate
- Driver resistance for realistic waveform

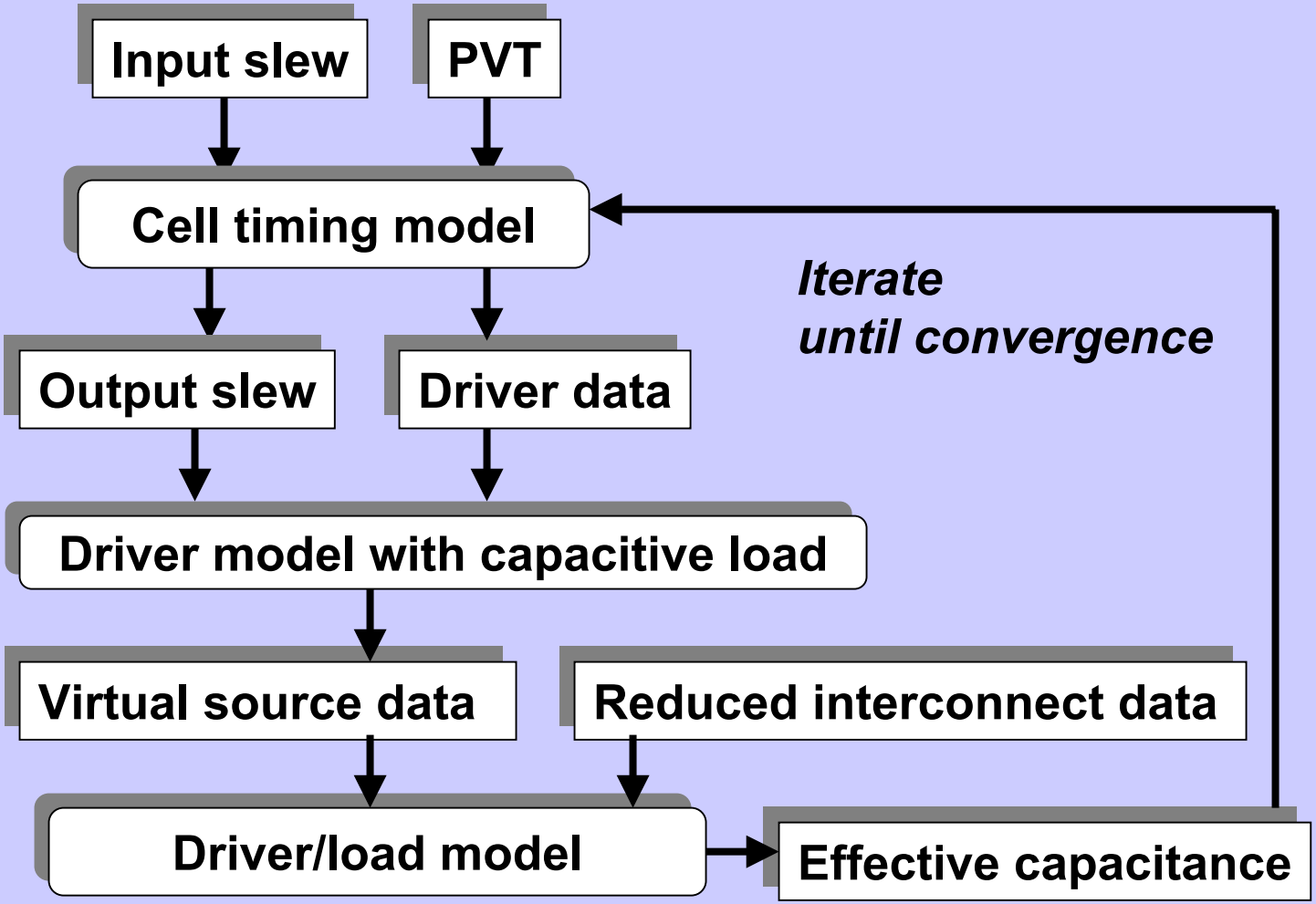


Distributed load

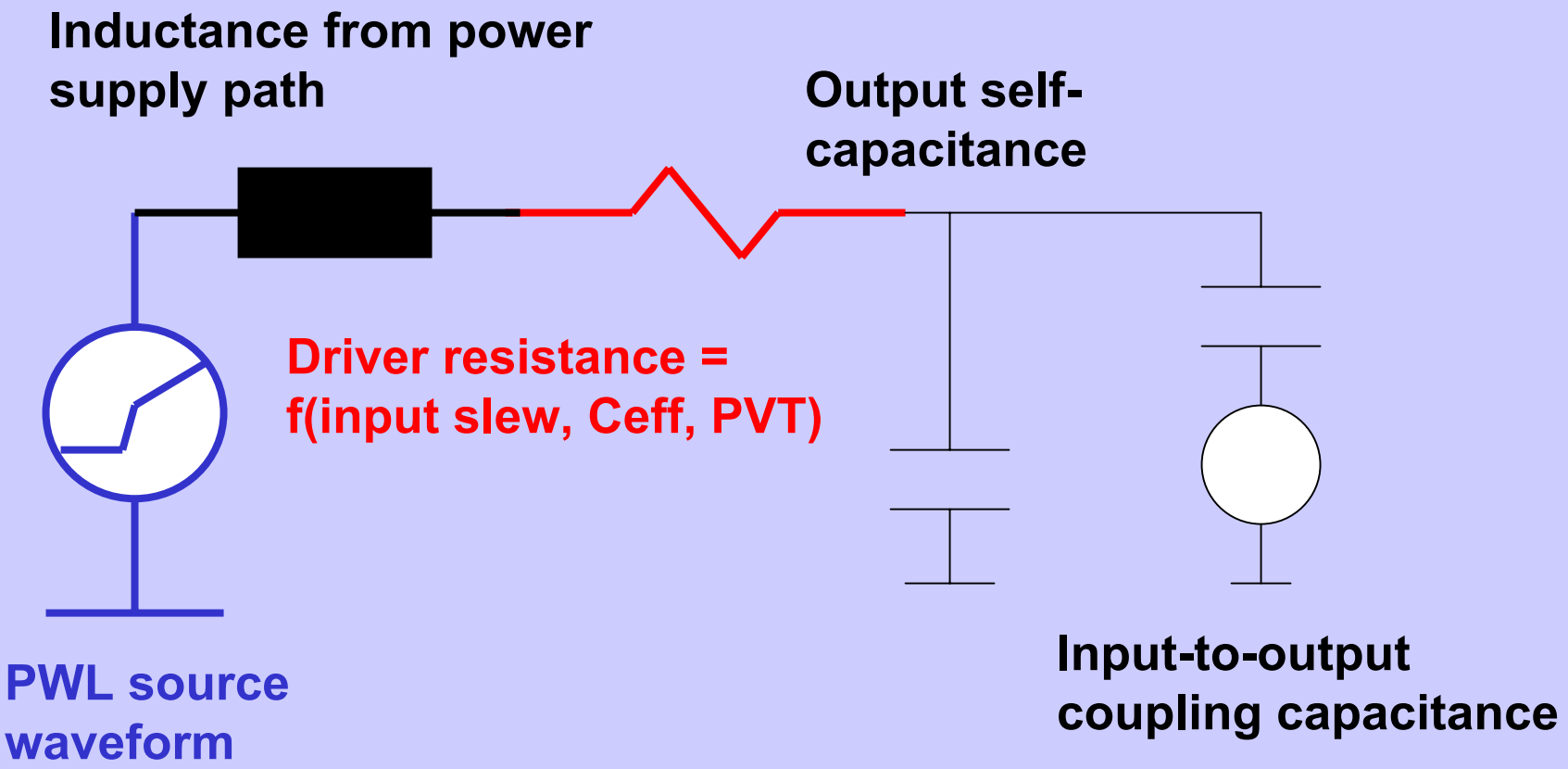
- General R(L)C network is reduced in 2 steps



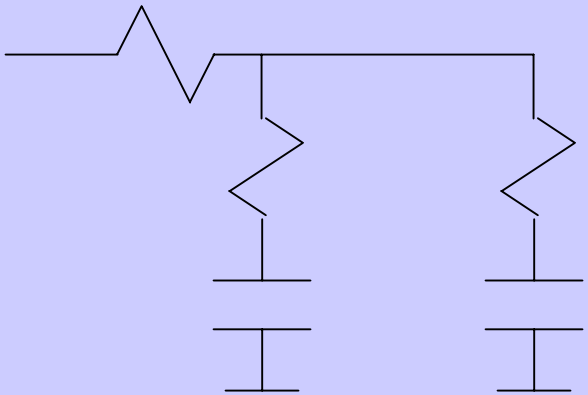
Interdependent cell/interconnect timing



Improvements for driver model

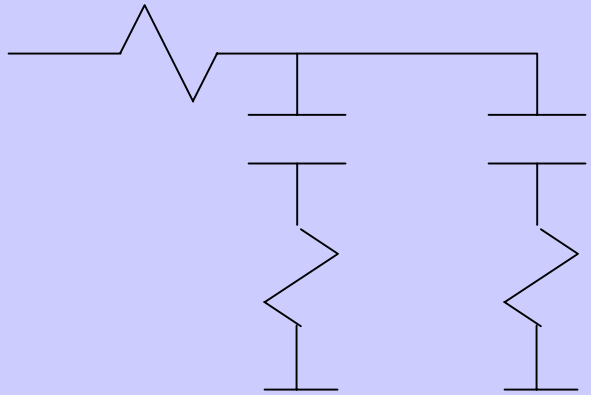


Improvements for load model

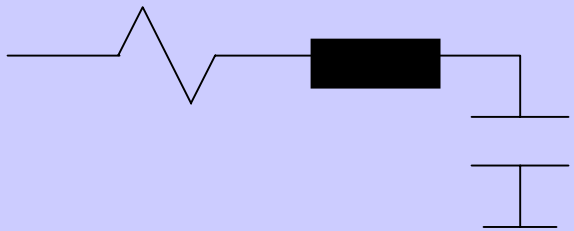


Multi-fanout with unbalanced load

equivalent



Non-grounded load capacitance



Load with inductance

Characterization of improved models

- Chose driver model
  - Characterize independent parameters of driver model for each cell
    - Simplest example: driver resistance **Rdriver**
  - Characterize dependent parameters of driver model under capacitive load
    - Simplest example: virtual source ramp time **deltaT**
- Chose driving point load model
  - Characterize effective capacitance as function of driver model parameters and driving point load model parameters
    - Example: **Ceff** = f(**deltaT**, **Rdriver**, **pi-model** params)

Timing summary

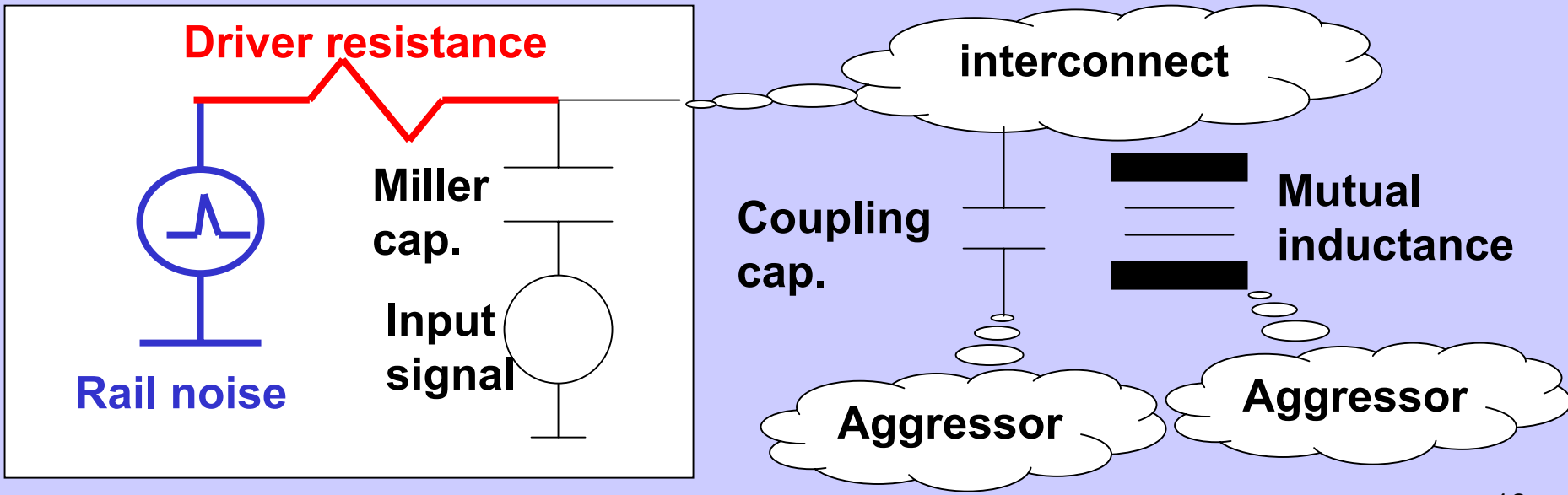
- Enhancement of 2-dimensional delay, slew models
  - Existing dimensions: input slew, load capacitance
  - New dimensions: Voltage, Temperature
- Enhancement of effective capacitance model
  - Generalized calculation scheme for Ceff
  - Cell-specific characterization of driver model parameters
  - Load model dependent on interconnect topology

Noise

- Noise calculation involves
  - Noise generation and propagation
  - Noise margin check
- Noise margin characterization
  - Functionally correct output for flops and latches
  - No noise amplification through combinatorial cells
- Noise propagation characterization
  - Similar to slew propagation in timing
  - Noise rejection data can be derived

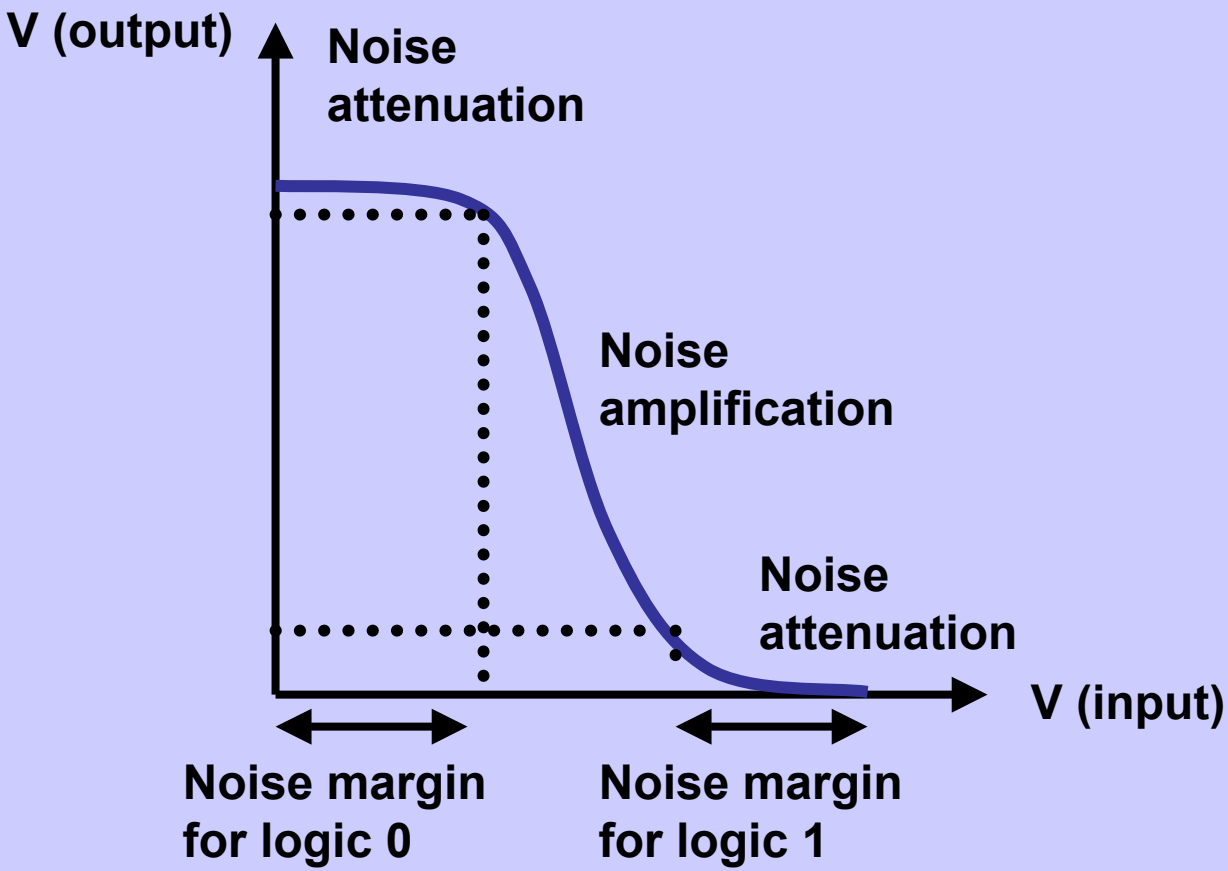
Noise generation

- Noise sources
  - Capacitive coupling on interconnect or between cell pins
  - Inductive coupling
  - Resistive coupling through power/ground rail
- Noise calculation requires driver model of victim cell



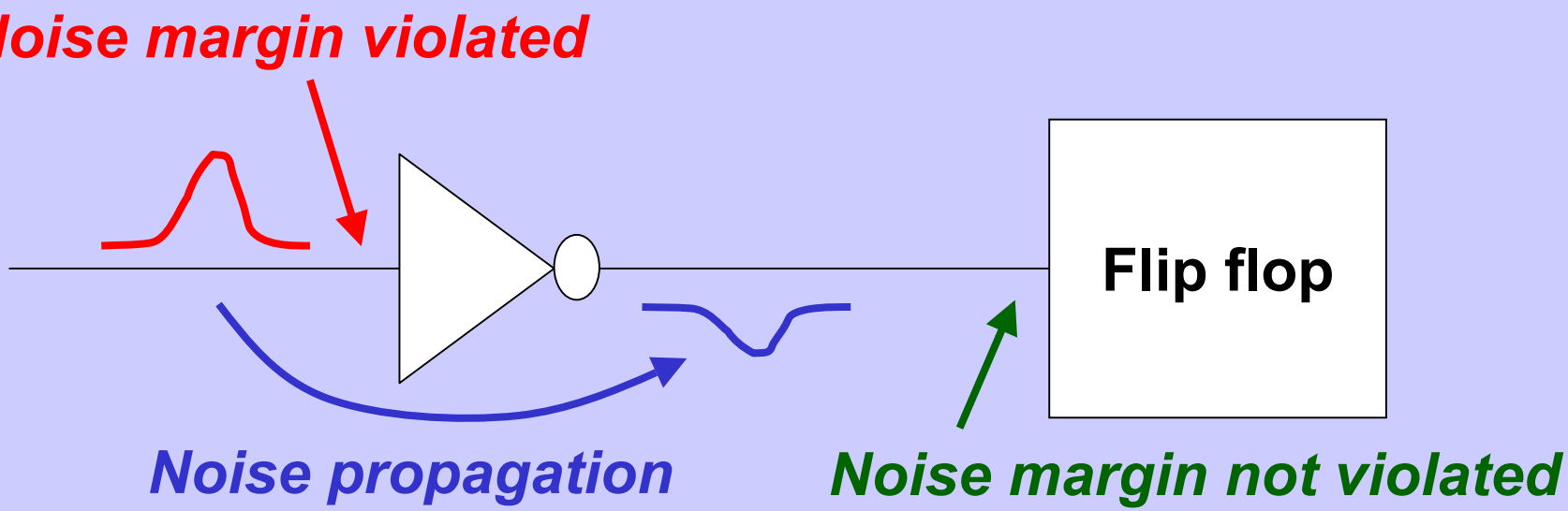
Noise margin characterization

- Use input-to-output voltage transfer characteristic
- Noise margin is PVT-dependent



Noise margin check

- Noise margin checked at every cell input pin
  - Many potential violators
- Alternative:
  - Propagate noise through combinatorial cells
  - Noise magnitude diminishes
  - Check noise margin only for flip flops and latches

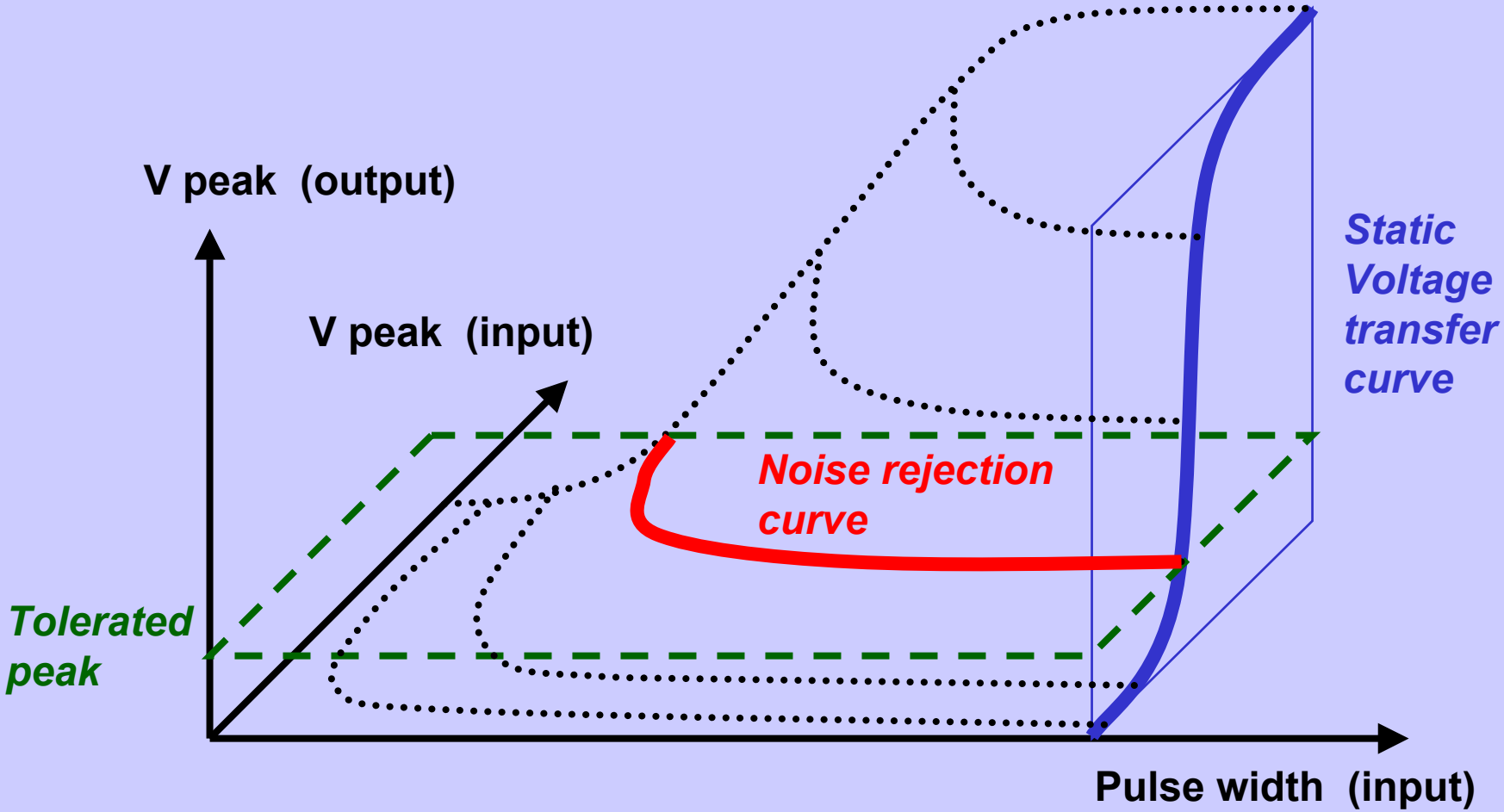


Noise propagation

- Noise waveform model parameters
  - Peak magnitude
  - Pulse width
- Characterization variables
  - Noise waveform parameters at output pin
  - Noise waveform input-to-output delay
- Characterization dimensions
  - Noise waveform parameters at input pin
  - (effective) load capacitance
  - PVT

Noise rejection

- Intersect noise propagation curve with tolerated peak magnitude plane

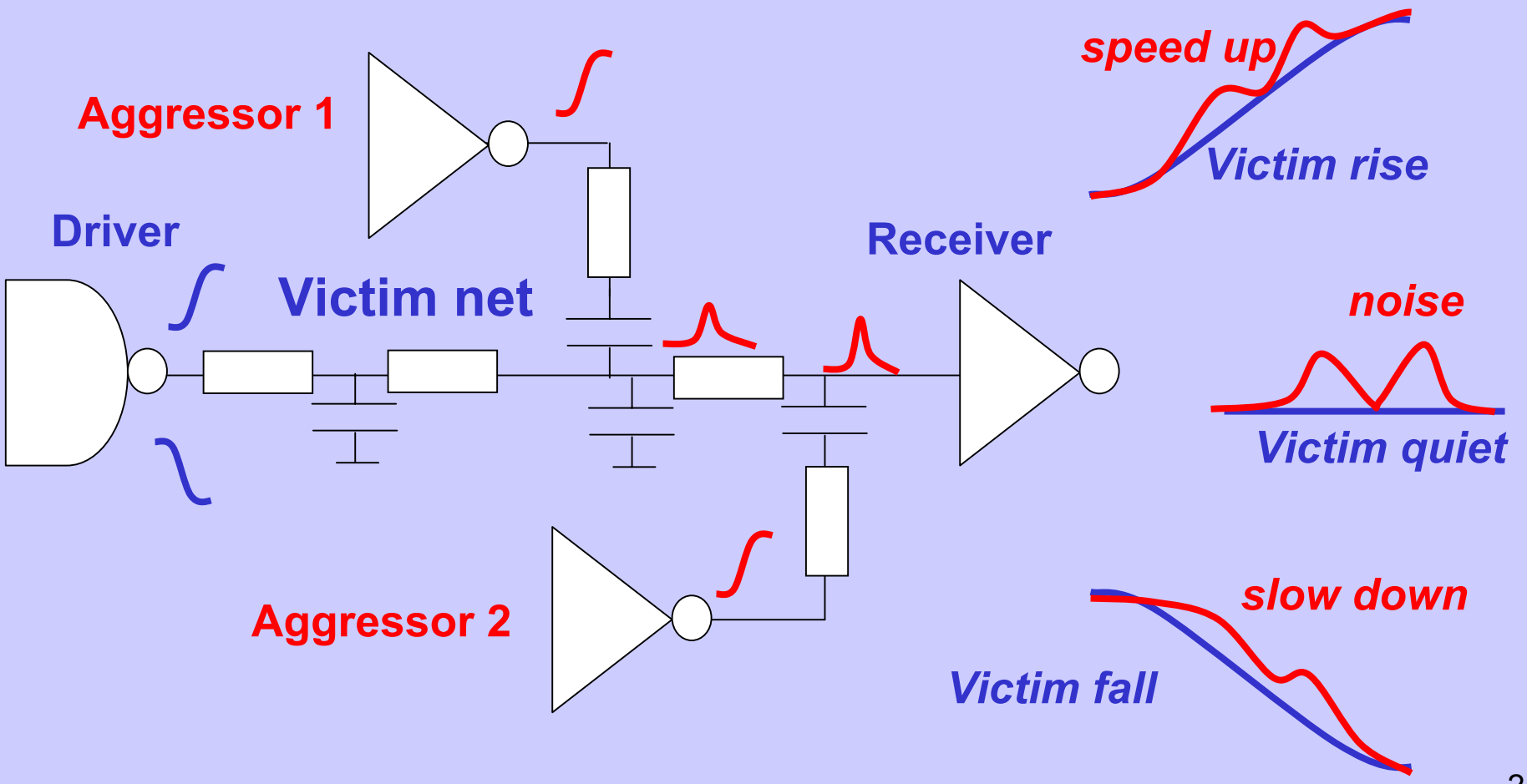


Time window concept

- Time window definition
  - Temporal region where a signal can switch
  - Pessimistic model: interval between earliest and latest possible switching time during clock cycle
  - More accurate model: also include intermediate regions where switching is impossible
- Time window prerequisite for evaluation of
  - Cumulative noise of multiple aggressors
  - Crosstalk-induced delay
  - Concurrently activated timing arcs

Multiple aggressors for crosstalk

- Evaluate effect of each aggressor individually
- Cumulative waveform by superposition in time

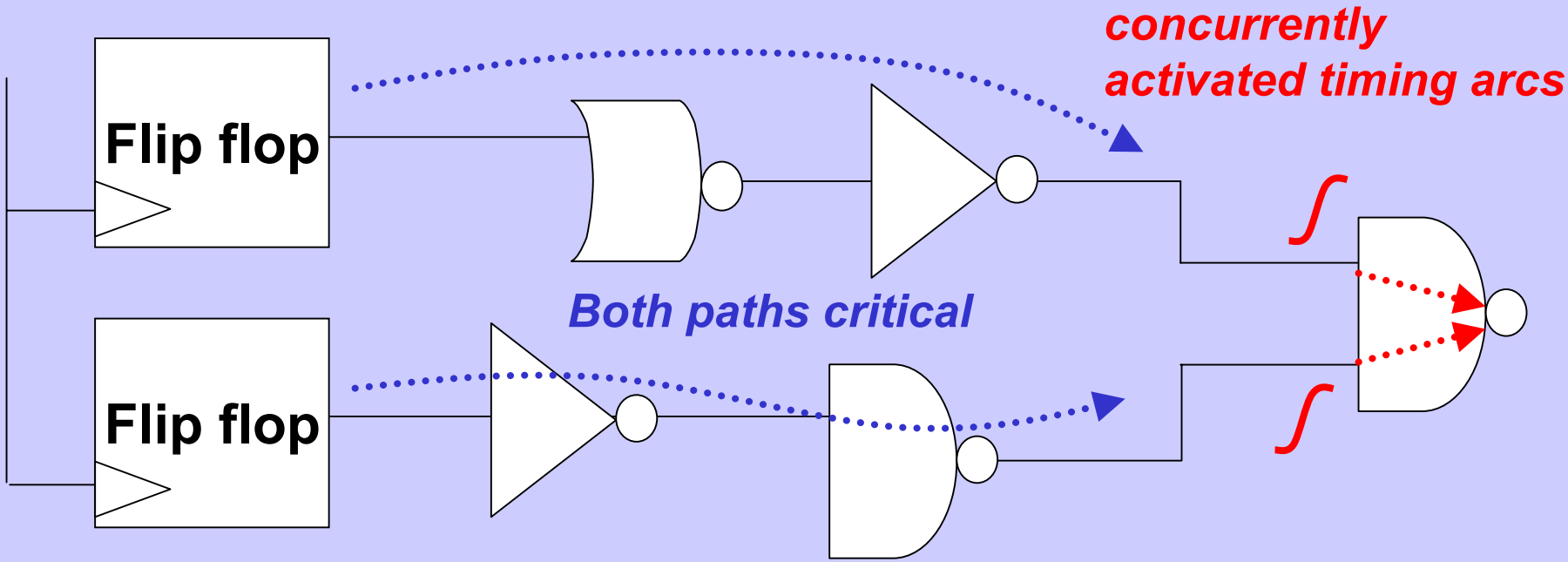


Issues with multiple aggressors

- Driver resistance is non-linear
  - Need good linear approximation
  - Otherwise, superposition principle does not work
- Interdependency between time windows and crosstalk-induced delay
  - Need iterative calculation
  - Initial assumption: all signals with coupling are subjected to crosstalk-induced delay
  - Calculate time windows with this assumption
  - Eliminate crosstalk for signals with non-overlapping time window
  - Narrow down time windows in subsequent iteration

Concurrently activated timing arcs

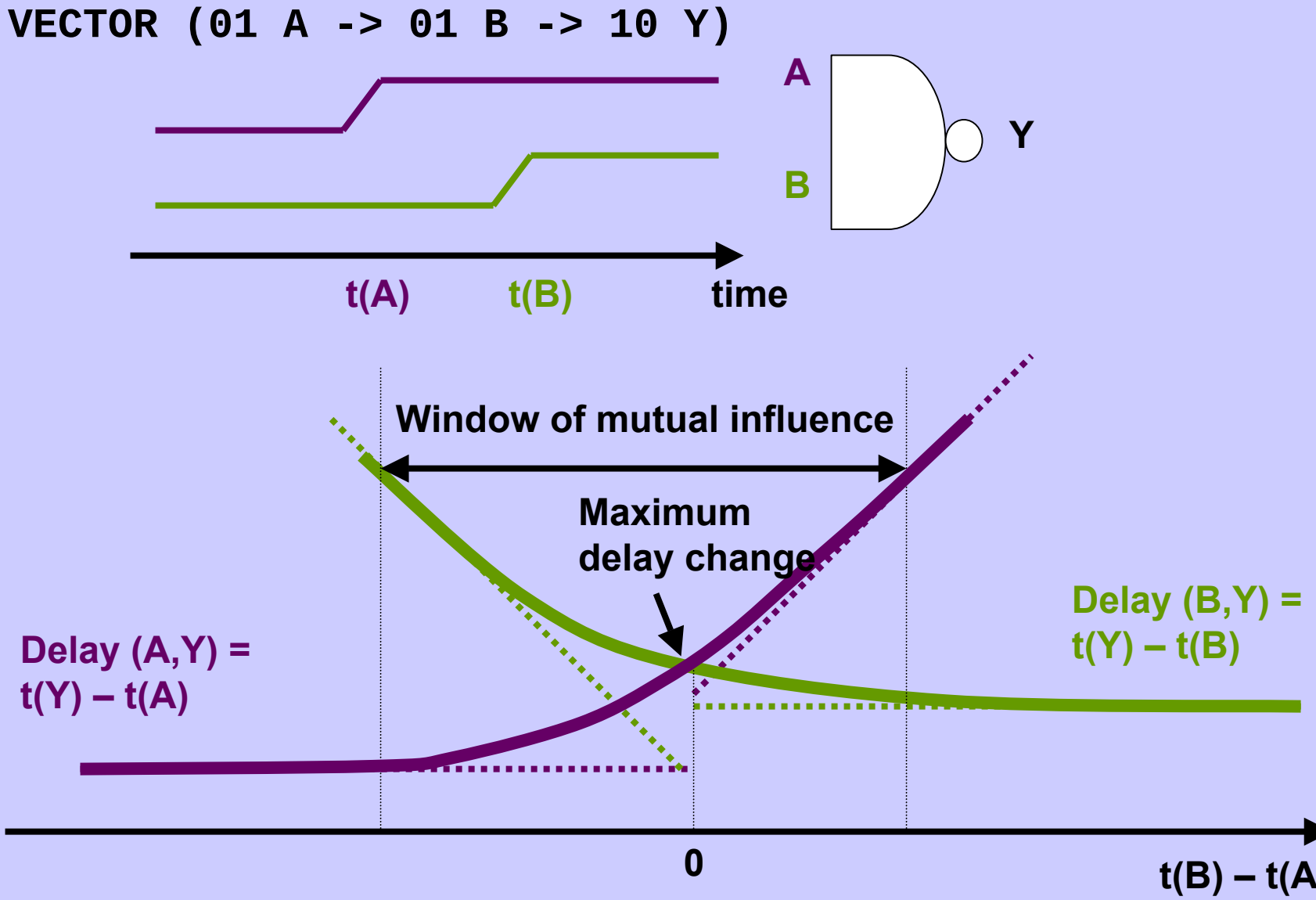
- Time windows on critical paths do overlap
  - Multiple timing arcs at cell inputs activated simultaneously
  - Significant delay change compared to single timing arc



Issues with multi-input timing arcs

- Effect is not trivial to model
  - Effect is non-linear
  - Depends on logic function of cell
  - Requires more cell characterization
    - Additional dimension: time between adjacent input signal transitions
- Requires enhancement of timing analysis
  - Extension of timing arc concept to ALF vector
    - ALF vector specifies stimulus for which the effect is characterized

Multi-input timing characterization



Noise summary

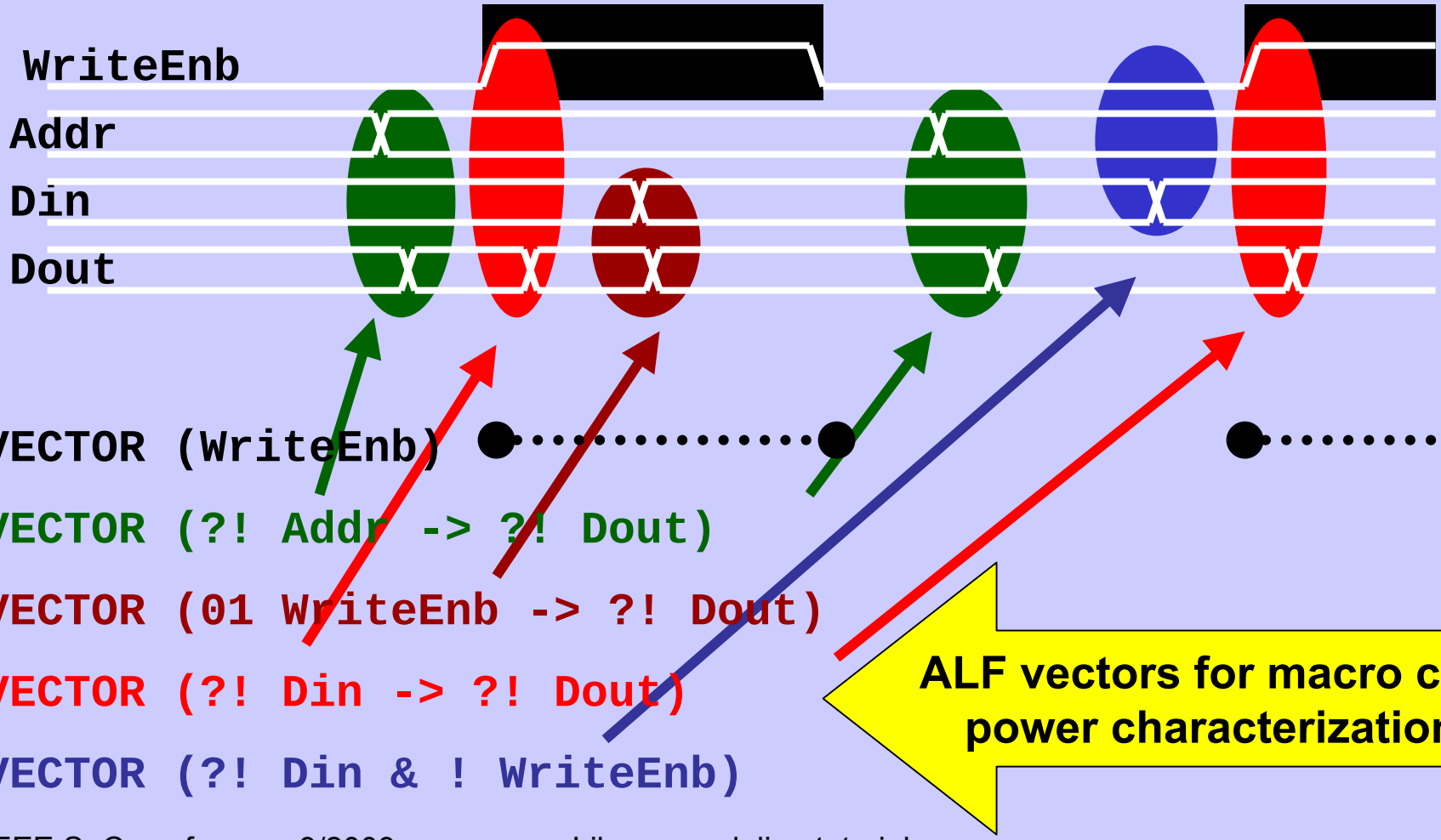
- New characterization variables for noise
  - Noise margin
  - Noise propagation
  - Noise rejection can be derived from noise propagation
- Timing and noise analysis inseparable
  - Need time windows to calculate cumulative noise and effects of noise on timing
  - Time window concept offers opportunity for multi-input timing arc modeling

Power

- Static power
  - Dependent on the logic state of the circuit
  - PVT is a characterization dimension
- Transient energy
  - Dependent on the logic operation of the circuit
  - Characterized for same dimensions as timing and noise
  - Can be divided into internal and external energy
  - External energy is the exact product of load capacitance (not effective capacitance) and supply voltage
  - Internal energy depends on input waveform and load model, in a similar way as timing and noise

ALF vector concept for power

- Vector represents characterization stimulus
- Vector occurrence is monitored during analysis



Power analysis

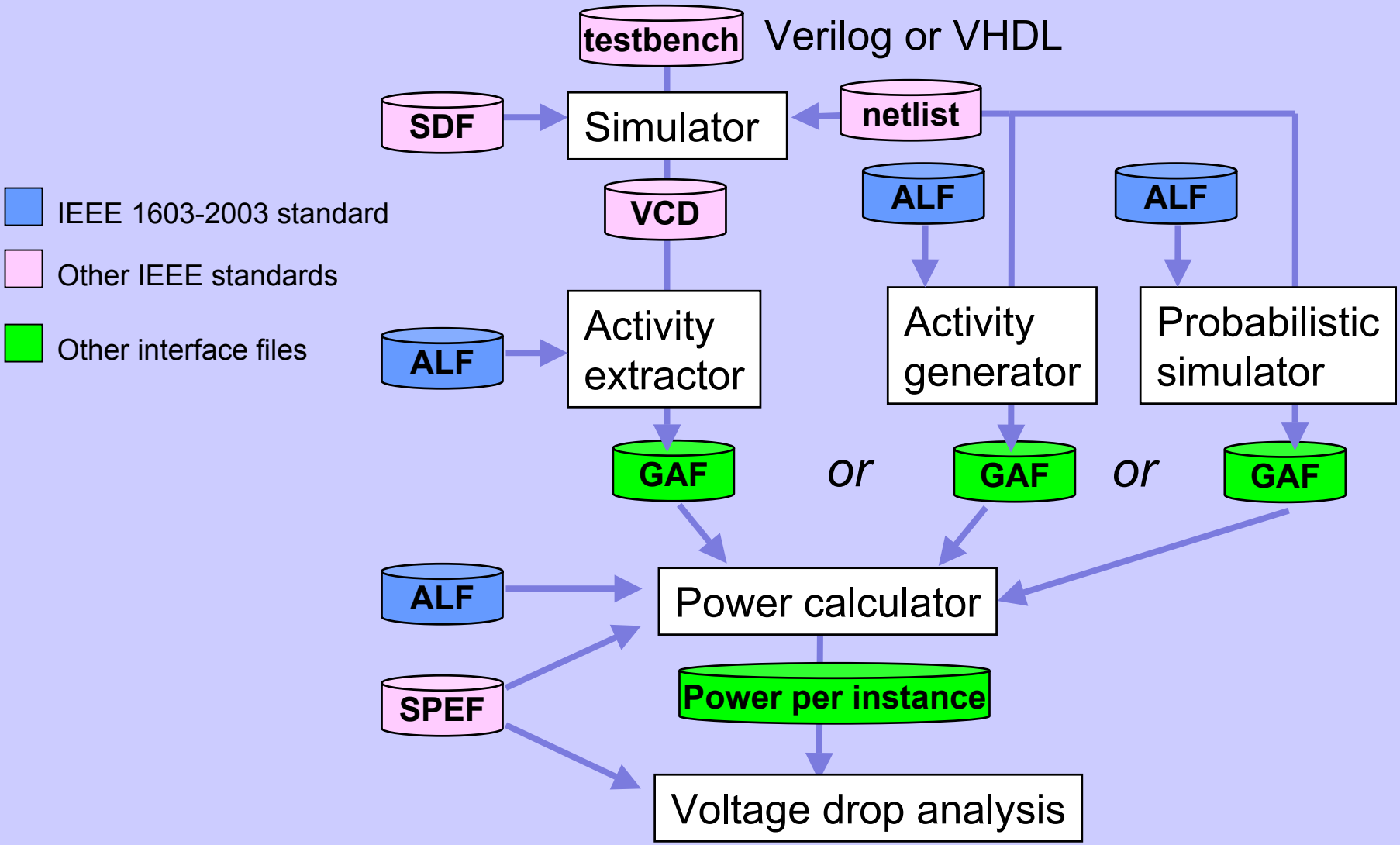
- For each cell instance in design:
  - Calculate ENERGY or POWER for each VECTOR
  - Get frequency or probability or each VECTOR
- Global Activity File (GAF) contains instance-specific frequency or probability for VECTOR
  - More accurate than frequency and probability per net
  - Logical correlations are preserved
  - Exact power results in conjunction with ALF library

Total power = $\sum_{\text{All transient vectors}}$ **ENERGY(VECTOR)** * **frequency(VECTOR)**

\+ $\sum_{\text{All static vectors}}$ **POWER(VECTOR)** * **probability(VECTOR)**

ALF **GAF**

Power analysis flow

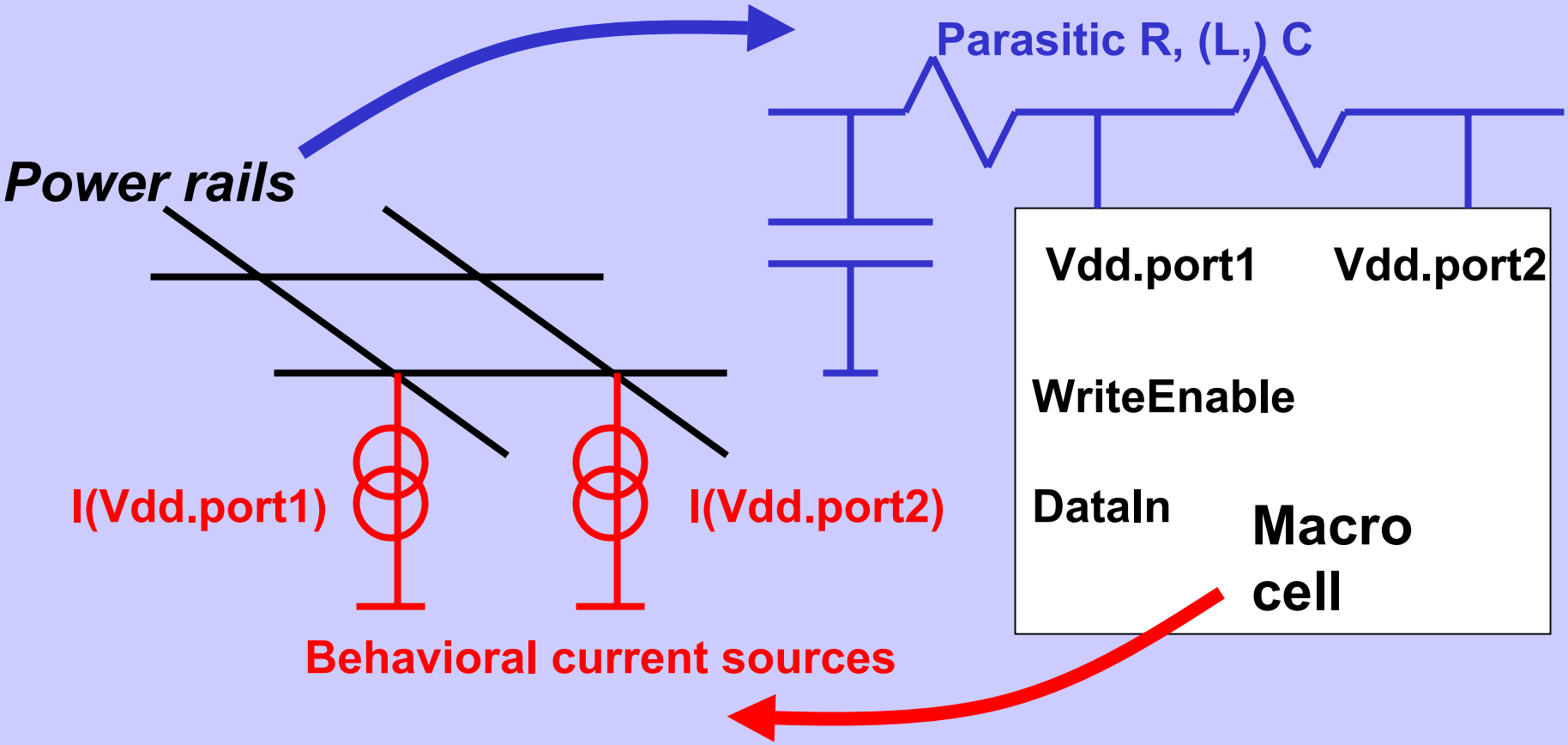


Voltage drop

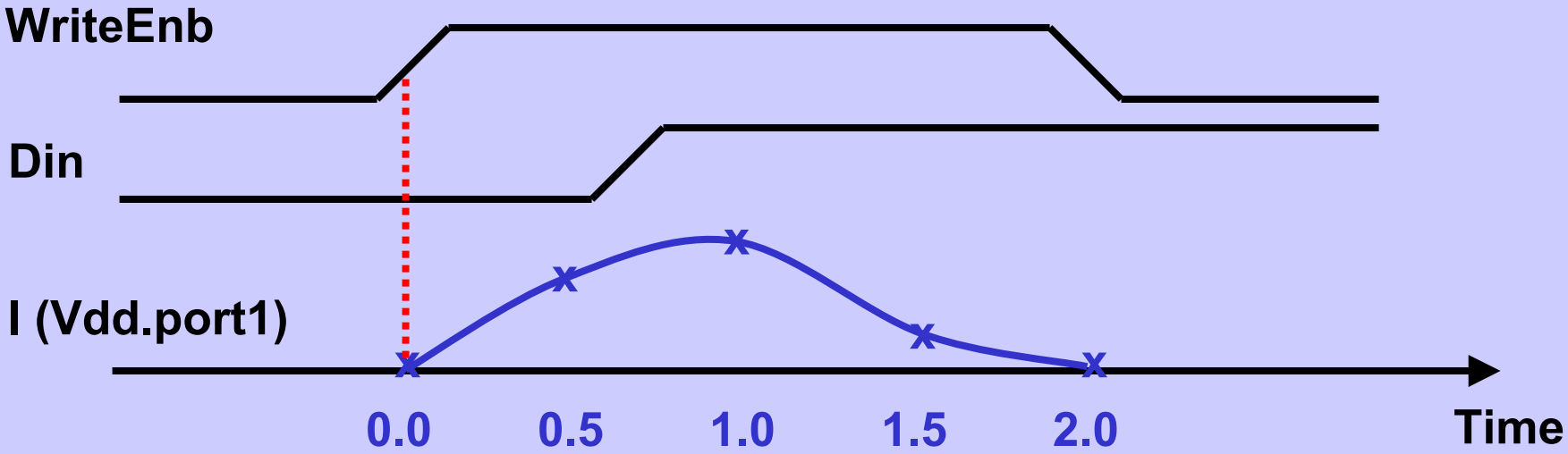
- Cause of voltage drop
  - Current consumption of cells
  - RLC parasitics of power supply network
- Effect of voltage drop
  - Change in timing and noise waveforms
  - Change in setup, hold, noise margin
- Cell characterization requirements
  - Supply current waveform for logic operation
  - Self-decoupling capacitance

Modeling of transient voltage drop

- Transient current sources associated with cell
  - Temporal granularity: current for each ALF vector
  - Spatial granularity: current for each supply port



Current waveform description in ALF



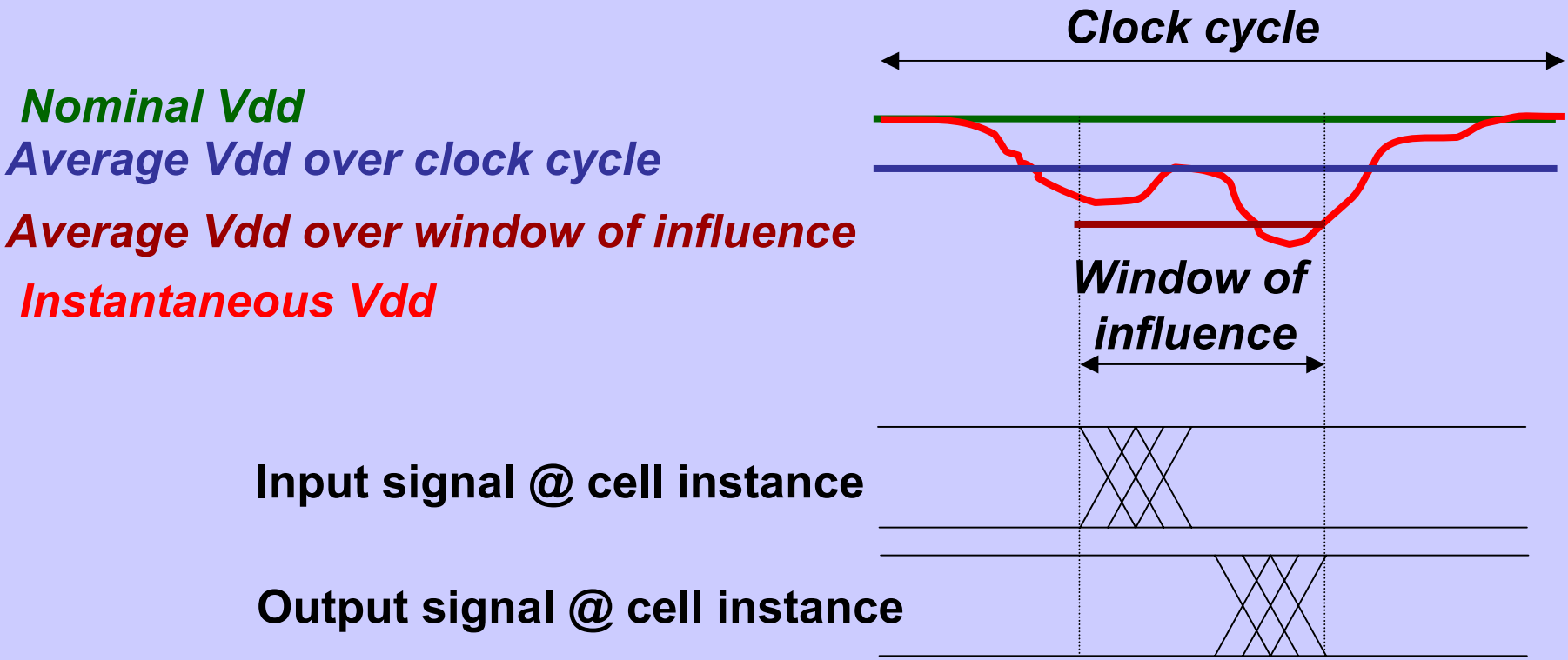

```
VECTOR ( 01 WriteEnb -> 01 Din -> 10 WriteEnb ) {
  CURRENT { PIN = Vdd.port1; MEASUREMENT = transient;
    HEADER {
      TIME { FROM { PIN=WriteEnb; EDGE_NUMBER=0; }
        TABLE { 0.0 0.5 1.0 1.5 2.0 }
    } }  TABLE { 0.0 0.4 0.5 0.2 0.0 }
} }
```

Time scale relative to event in VECTOR

1D table for current = f(time)

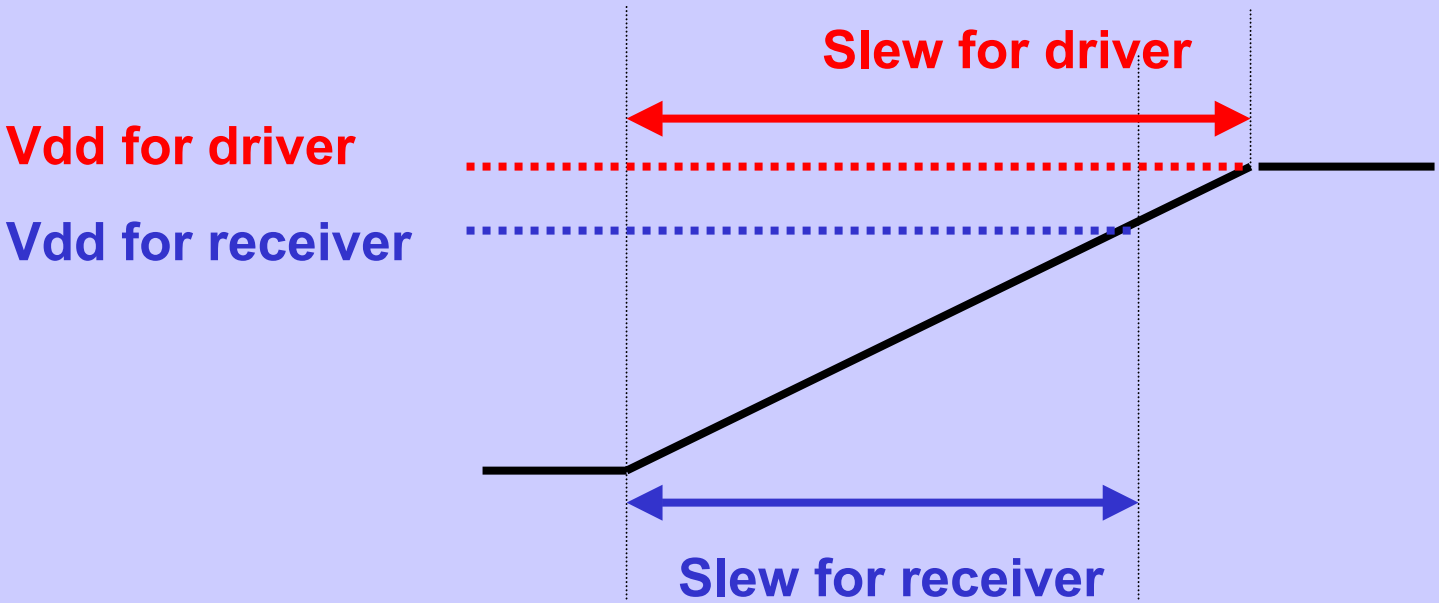
Voltage-drop based timing

- Need voltage drop during window of influence
- Window of influence is bound by time windows for input and output signals of cell instance



Interconnect analysis with voltage drop

- Supply voltage difference between driver output pin and receiver input pin
  - Reference for slew rate measurement changes
  - Signal appears to be faster or slower



Power and voltage drop summary

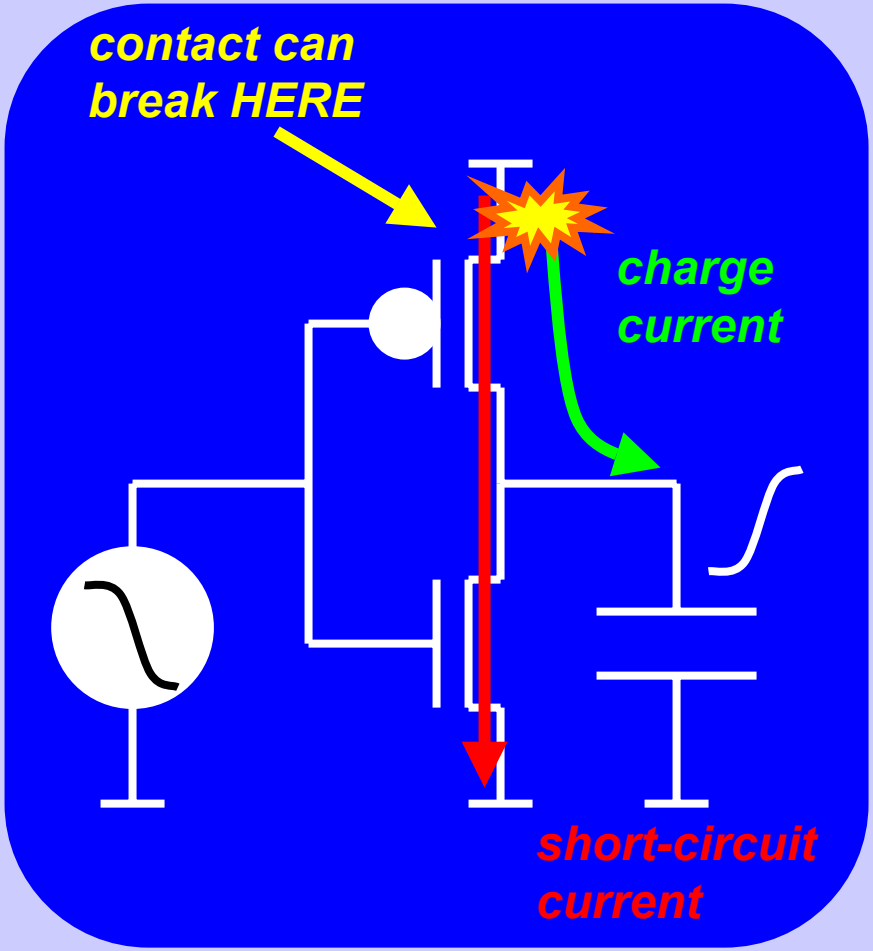
- Vector concept pertinent for power calculation
  - Characterization variables and dimensions for each power vector similar as for timing
  - No specific library characterization required for static voltage drop
- Transient voltage drop requires extensive library characterization and modeling
  - Transient current waveforms for each vector
  - Driver/receiver characterization for different signal voltage levels due to voltage drop
  - Time window concept pertinent for timing calculation with transient voltage drop

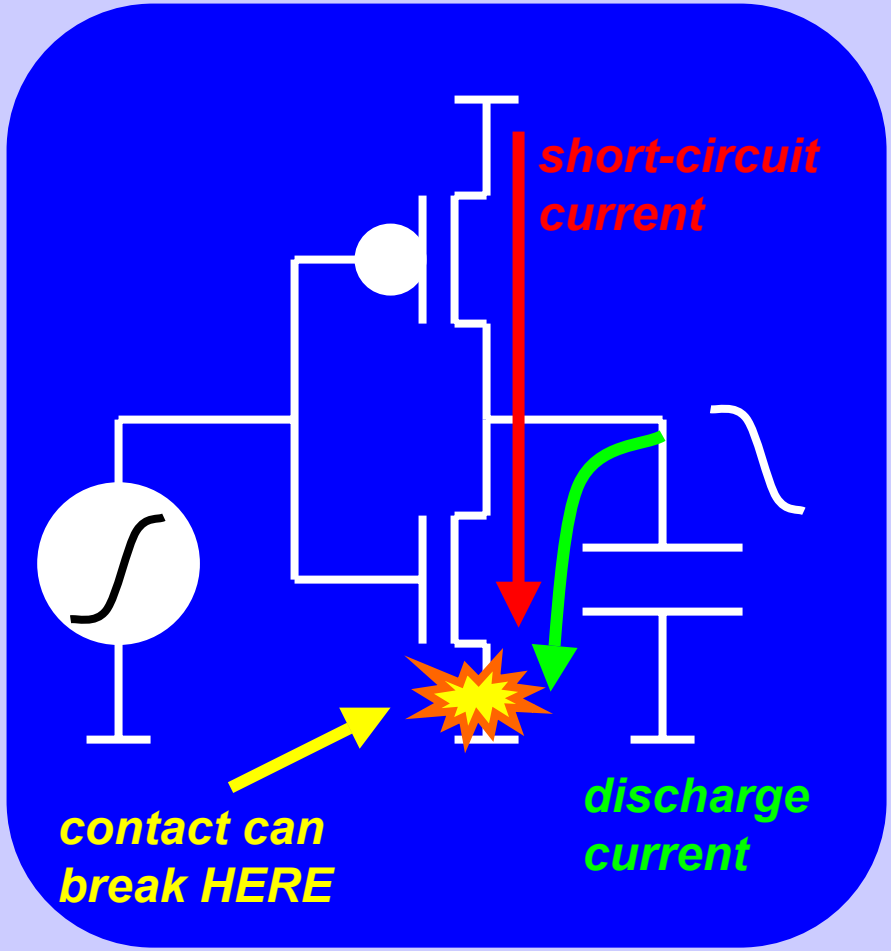
Reliability

- Electromigration
  - Process rules for electromigration
  - Interconnect analysis for electromigration
- Transistor performance degradation
  - Hot electron effect (NMOS)
  - Thermal instability (PMOS)
- Abstract cell modeling for reliability

Electromigration illustration

- Excessive current density leads to metal displacement
- Contacts or wire segments can break





Process rules for electromigration

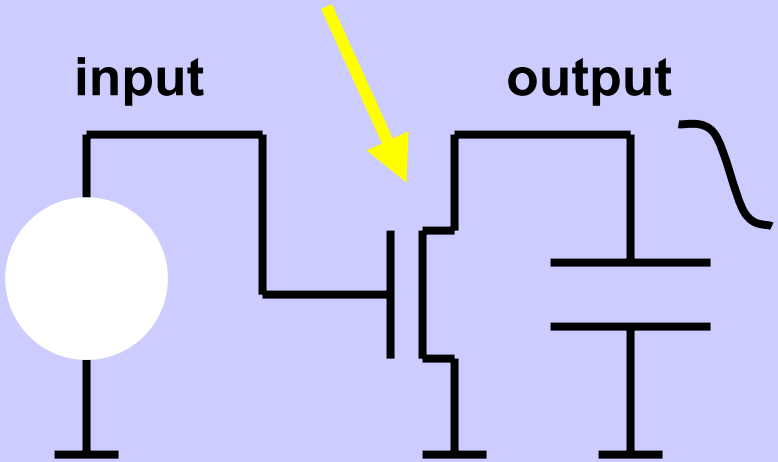
- Current density limits for each layer
  - Average current for time-variant unidirectional current flow
  - Absolute average current for time-variant bi-directional current flow
  - RMS current for joule heating of wire
  - Peak current against fuse breaking
- Current limits can be frequency-dependent
  - Low frequency: little or no self-healing effect
  - High frequency: self-healing effect

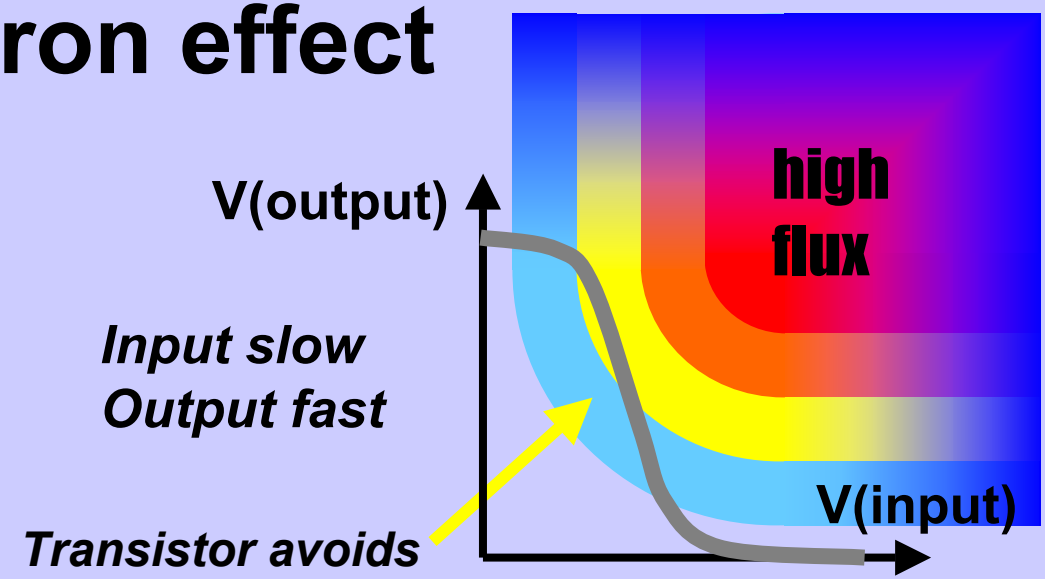
Interconnect analysis for electromigration

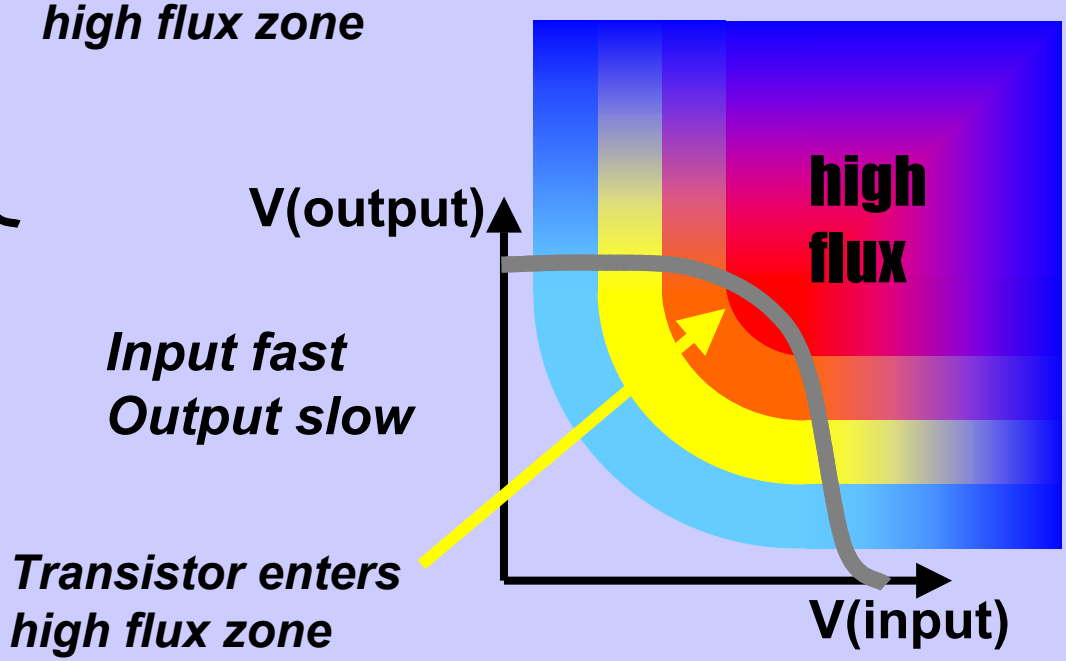
- Current through each physical object needs to be evaluated
  - Physical objects are vias and routing segments
- Need to preserve correspondence between electrical parasitics and physical objects
- Signal electromigration
  - Extension to interconnect timing analysis
- Power electromigration
  - Extension to voltage drop analysis

Hot Electron effect

Hot electron effect occurs only when NMOS transistor switches "on"



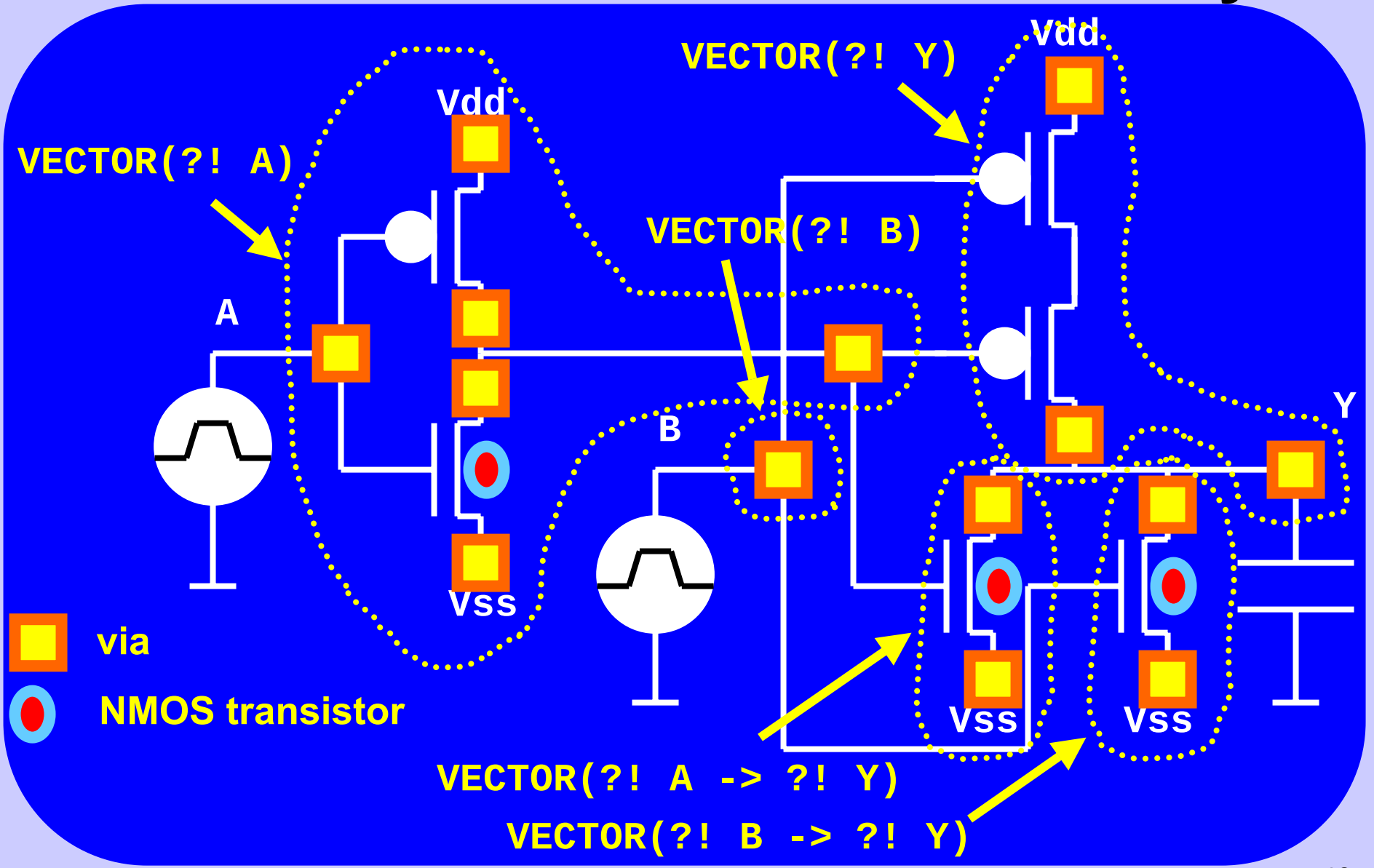




Cell characterization for reliability

- Put current meters on all sensitive structures within cell
  - Find set of stimuli (I.e. ALF vectors) that expose each structure to stress
- For each vector
  - Measure the stress (e.g. current, flux etc.) for variable characterization dimensions (input slew, output load etc.)
  - Calculate repetition frequency of stimulus for which the stress equals the limit

Cell characterization for reliability



Reliability summary

- Reliability must be insured throughout
  - Inside cells
  - On signal interconnect
  - On power rails
- Reliability rules can be pre-characterized and transformed into abstract models for cells and macro cells
  - Frequency limits associated with ALF vectors
  - This covers electromigration, hot electron and any other frequency-dependent stress

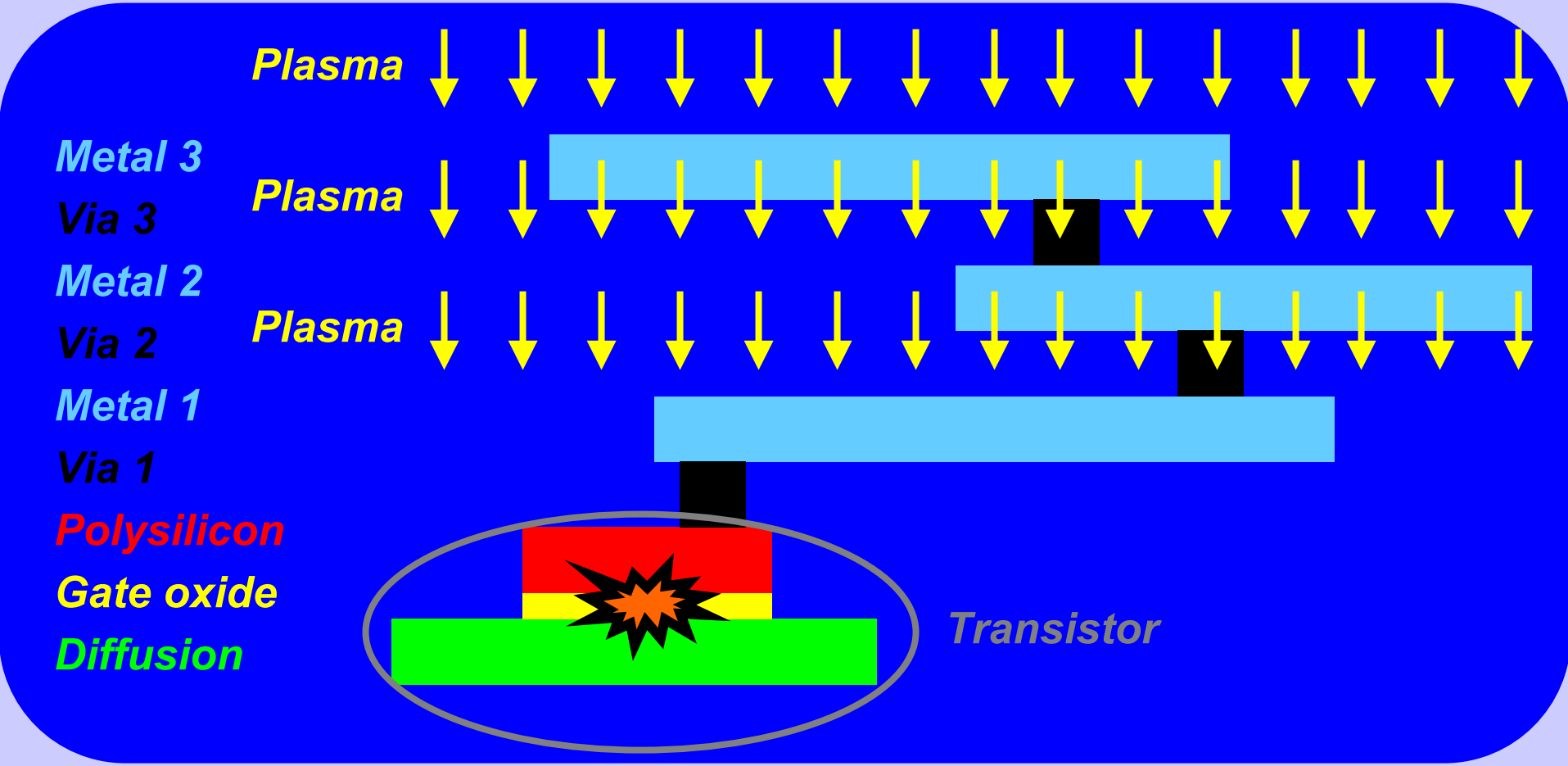
Manufacturability

- Process antenna rules
- Metal density rules
- Design rules for sub-wavelength patterns
- Abstract cell model for manufacturability analysis

Process antenna rules

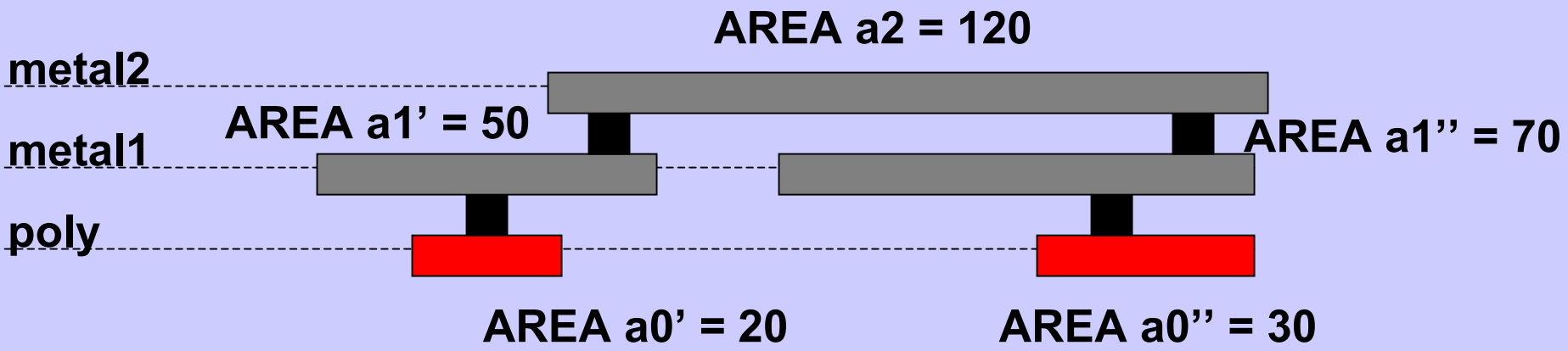
- Transistor collects charge during etching of metal structures
- Cumulative effect can destroy the transistor
- Likelihood of destruction
  - Proportional to area and perimeter of structures being etched (aggressor)
  - Inverse proportional to size of transistor being exposed (victim)
  - Limit against destruction often expressed as ratio between aggressor and victim area

Process antenna illustration



Antenna rule evaluation

- Account for manufacturing order
- Count only top-down connections
- Combine poly areas connected top-down

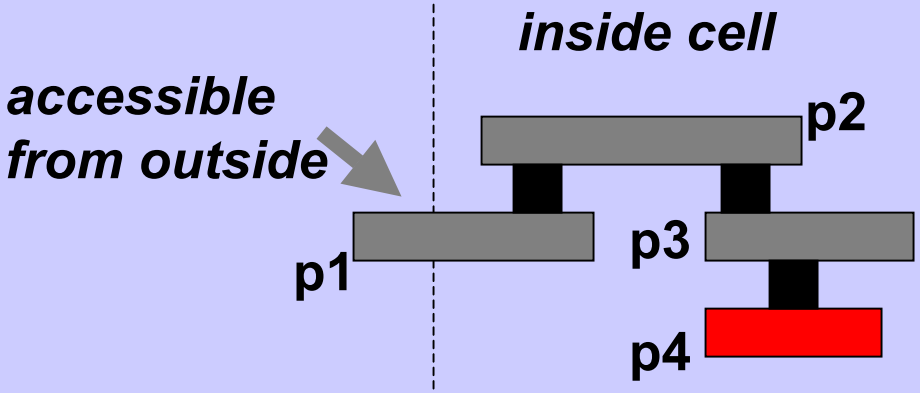


When metal1 is fabricated: check a1'/a0' = 50/20 and a1''/a0''=70/30

When metal2 is fabricated: check a2/(a0'+a0'') = 120/(20+30)

Antenna model abstraction for cell

- Antenna checker must look inside cell
  - Pins of the cell are accessible for connection
- Abstraction of artwork required
  - Geometry of accessible structure must be exposed
  - Geometry of internal artwork can be reduced to connectivity and area of artwork structures



Example:
Describe full geometry of p1
Specify area of p2, p3, p4
Connection between p2, p3, p4
Connection between p1, p2

Metal density rules

- Definition of metal density
  - Total area within a region on a layer = A
  - Sum of all subregions covered with metal = M
  - Metal density = M divided by A
  - Regions can be small (local metal density) or large (global metal density)
- Rule for minimum metal density
  - If not satisfied, metal has to be added
- Rule for maximum metal density
  - If not satisfied, metal has to be removed
- Reason for metal density rules
  - “Hills” and “valleys” on layer surface evenly distributed
  - Eliminate risk of scraping off metal during planarization

Density model abstraction for cell

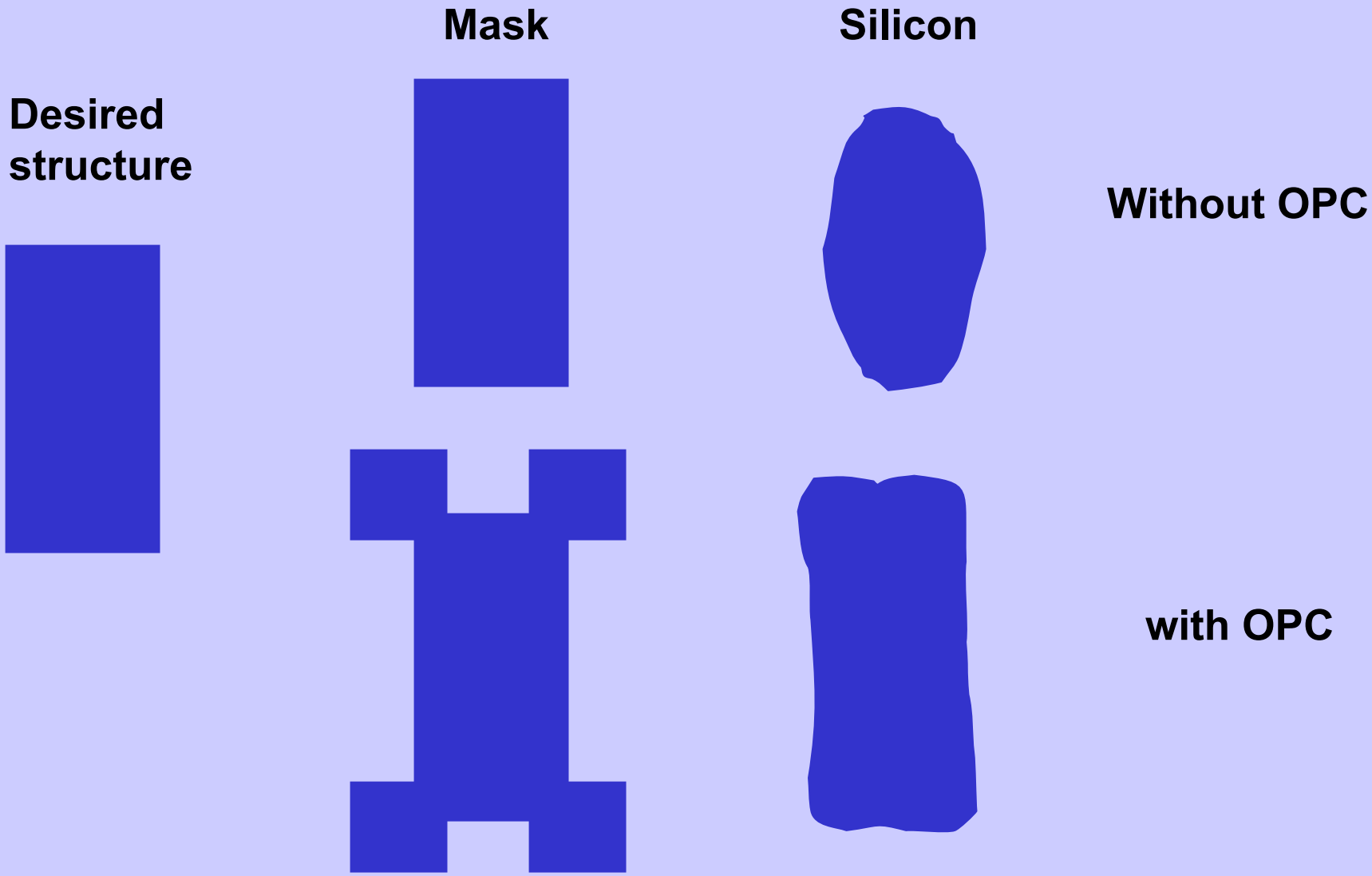
- Calculate density for each layer within the bounding region of a cell
  - Represent density of each layer and total area of bounding region in library model of the cell
- Metal density can then be evaluated in larger context

Example:
Cell bounding box area = 100
Density of metal1 within cell = 0.5
5 cells are placed in a region with area = 1000
Density of metal1 within region = 5*0.5*100/1000 = 0.25

Design rules for sub-wavelength patterns

- Lithography has limited resolution
  - Geometry size smaller than the wavelength
  - Optical low-pass filter
  - Structures become “dull” or disappear
  - Structures may “flow” into each other
  - Countermeasure: optical proximity correction (OPC)
- Interference of fractioned waves
  - Structures subjected to destructive interference can not be produced on silicon
  - Countermeasure: phase shift mask

Illustration of OPC



Consequences of OPC and phase shift

- Limitations of mask enhancements
  - Works only for limited set of patterns
  - Works only in limited context
- Rules required to describe the legal range of geometries within their context
  - Codependent min/max length of a geometry
  - Width-dependent distance between geometries

Physical abstraction summary

- Hierarchical physical design
  - Cell layout is created by custom design tool
  - Cell layout is abstracted to a physical model
  - Chip layout is created by assembly of standard cells and interconnect
- Abstract physical model must preserve enough information to evaluate
  - Process antenna rules
  - Metal density rules
  - Pattern-and context-dependent rules for spacing, width, length, overhang etc.

Summary

- Modeling domains are inter-related
  - Accurate timing calculation requires characterization effort for noise, power, voltage drop
- Abstraction is a pertinent concept in all modeling domains
  - Required for SoC design
  - The ALF vector concept is key for electrical characterization and abstract model creation

EDA industry situation

Domain	Library support	EDA tool readiness
Timing with PVT	.lib ALF	Production
Driver/load model	Tool-specific ALF	Production, Research
Noise	ALF .lib other	Production
Multi-input timing	ALF	Research
Power	ALF .lib	Mainstream
Static voltage drop	N/A	Mainstream
Transient voltage drop	Tool-specific ALF	Emerging production
Reliability	ALF .lib other	Production
Manufacturability	LEF other .lib ALF	Production, continuous change

What's next

- Library harmonization and interoperability
  - Formal cross-reference between .lib and ALF
  - Reduce library fragmentation
  - Facilitate more streamlined development of new libraries
  - Facilitate development of next-generation EDA tools with support for better library modeling
- This project is supported by 

  - Successful incubator for future IEEE standards

References

http://www.eda.org/alf

http://www.accellera.org

Thank you