Open Kit Project

Description of Physical Design Rules and Technology

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Version	Date
0.0	2004-05-13

Purpose and scope

This document specifies a method of describing physical design rules and technology as needed by custom design tools. The organization of topics follows the OpenKit Design Objective document. The Advanced Library Format [IEEE std 1603-2003] is used as a description vehicle for each topic.

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1.0 Layer information

This section specifies how to describe layer types and purpose, layer sourcing and naming.

1.1 Layer terminology

TABLE 1. Layer terminology

Term	Explanation	Comment
Layer	A surface in the x-y plane, subject to description of layout geometry	
Layer, fabricated	A layer wherein layout geometry is created using a silicon manufacturing process technology, by selectively depositing and/or removing material on the surface.	
Layer, virtual	A layer wherein geometry is described for the purpose of expressing relationships and/or constraints between other layout geometries. A virtual layer is not fabricated.	
Layer type, layer purpose, layer sourcing	A way of classifying layers from an application standpoint	
Layer naming	A way of identifying a layer, including the capability to refer to a layer by name.	

1.2 Layer description in ALF

A *layer* (see IEEE Std 1603-2003, 8.16) is declared as a named object within a technology *library* (see IEEE Std 1603-2003, 8.2). The layer which is fabricated first, i.e., the layer closest to the silicon substrate, is declared first. A virtual layer is declared after the declaration of the uppermost fabrication layer.

FIGURE 1. Layer declaration template in ALF

```
LIBRARY <libraryname> {
   /* put global information (e.g. units) here */
   LAYER <layername> {
      LAYERTYPE = <layertype> ;
      /* put layer-specific information
      (detailed in other sections) here */
   }
}
```

In the ALF template, <libraryname> and <layername> are placeholders for the actual name of the library (e.g. my90nm) and the layer (e.g. poly, metal1, cut12), respectively.

The <layertype> is the placeholder for a keyword specifying the purpose of a layer. The predefined ALF keywords (see IEEE Std 1603-2003, 8.17.2) are listed below.

TABLE 2. Layertype in ALF

<layertype>	**Explanation**	**Comment**
routing	a fabricated layer providing electrical connections within a plane	
cut	a fabricated layer providing electrical connections between planes	
substrate	a fabricated layer at the bottom	
dielectric	a fabricated layer providing electrical isolation	
reserved	a fabricated layer wherein the geometry cannot be changed by the layout designer	
abstract	a virtual layer	

A typical sequence of layer types might be *substrate*, *reserved*, *routing*, (one or more) *dielectric*, *cut, dielectric* (one or more), *routing*, (one or more) *dielectric*, *cut*, etc., followed by (one or more) *abstract*.

2.0 Layer and Structure Specification

2.1 Layer and structure terminology

TABLE 3. Layer and structure terminology

Term	Explanation	Comment
via	a predefined structure of geometries for electrical connection between layers	
electrical characteristics of a layer or a structure	calculation rule for resistance and capacitance involving the layer or structure	
physical characteristics of a layer or a structure	geometric measurements involving the layer or structure	

2.2 Layer and structure description in ALF

The electrical and physical characteristics of a layer are described within the context of the layer declaration (see Figure 1 on page 3). The quantities describing electrical characteristics are *resistance* and *capacitance*. The quantities describing physical characteristics are *thickness* and *height*. A quantity can be a single number, a discrete set of numbers, a continuous range of numbers, or a function of another quantity. All these descriptions use the *arithmetic model* construct (see IEEE Std 1603-2003, 10.3), which supports a scalar value, a *table* of values with an associated *interpolation* scheme, or an *arithmetic expression*.

TABLE 4. Quantities for electrical and physical characteristics of a layer

Keyword	usage	See IEEE Std 1603-2003
CAPACITANCE	describe capacitance of a layer as a function of width, length, or area	10.15.3
RESISTANCE	describe resistivity of a layer, i.e., resistance as a function of width, length, or area	10.15.4
THICKNESS	describe the thickness of a layer	10.19.5
HEIGHT	describe the height of a layer above the substrate	10.19.6

A *via* (see IEEE Std 1603-2003, 8.18) is declared as a named object within a technology *library* (see IEEE Std 1603-2003, 8.2). It is a predefined set of geometries, each of which is defined as a *pattern* (see IEEE Std 1603-2003, 8.29).

A *pattern* is a geometry or a collection of geometries associated with a particular layer (referenced by <layername>). The geometry of a pattern is described using the *geometric model* construct (see IEEE Std 1603-2003, 9.16), which features the exact coordinates of the geometry.

FIGURE 2. Via template in ALF

```
LIBRARY <libraryname> {
   /* put global information (e.g. units) here */
   /* put layer declarations here */
   VIA <vianame> {
      VIATYPE
      PATTERN <patternname> {
         LAYER = <layername> {
         /* put geometric description of the pattern here */
      }
      /* put more pattern declarations here */
   }
```

A via declaration typically consists of three patterns, involving two adjacent routing layers and the cut layer in-between. A stacked via can involve five, seven, or more patterns.

The <viatype> is the placeholder for a keyword specifying the purpose of a via. The pre-defined ALF keywords (see IEEE Std 1603-2003, 8.19.2) are listed below.

TABLE 5. Viatype in ALF

<viatype>	**Explanation**	**Comment**
default	via can be used freely	
non-default	usage of the via is constraint by a rule (see Section 3.2 on page 7)	
partial_stack	via is used to construct a stacked via	
full_stack	via describes the full stack	

3.0 Design rule description

3.1 Design rule terminology

TABLE 6. Design rule terminology

Term	Explanation	Comment
Design rule	A constraint and/or a limit for measurable quantity related to a design object.	
Design rule, geometric	A constraint/limit for length/width/height/ area/perimeter of an object or for distance/ overhang between objects.	
Design rule, electrical	A constraint for connectivity between objects. A violation of the rule will lead to electrical malfunction of a circuit.	
Design rule, reliability	A constraint/limit for geometry, electrical current or other quantity imposed by electromigration or other stress. A violation of the rule will shorten the lifetime of a circuit.	
Design rule, manufacturability	A constraint/limit for geometry imposed by manufacturing, such as process antenna, pattern density, litography. A violation of the rule will reduce the yield of a fabricated circuit.	

3.2 Design rule description in ALF

The description of a design rule depends on the type of objects involved. A rule involving only one particular object, for example a *layer*, can be described within the declaration of the object (see also Figure 1 on page 3).

FIGURE 3. Template for layer-specific design rule in ALF

```
LIBRARY <libraryname> {
   /* put global information (e.g. units) here */
   LAYER <layername> {
      LAYERTYPE = <layertype> ;
      LIMIT <quantity> {
         /* put measurement definition of the quantity here */
         MIN {
            /* put calculation rule for lower limit here */
         }
         MAX {
            /* put calculation rule for upper limit here */
         }
      }
   }
}
```

A design rule involving multiple objects is described by declaring a *rule* (see IEEE Std 1603-2003, 8.20) as a named object within a technology *library*. Within the rule, other named objects, such as a *pattern*, a *region*, or an instance of a *via*, are declared. Constraints and limits involving measurable quantities related to those objects (e.g. *distance* between two patterns, *area* of a region) are then described.

FIGURE 4. Design rule template in ALF

```
LIBRARY <libraryname> {
   /* put global information (e.g. units) here */
   /* put layer declarations here */
   /* put via declarations here */
   RULE <rulename> {
      PATTERN <patternname> {
         LAYER = <layername> ; /* reference to a declared layer */
         /* put geometric description of the pattern here */
      }
      <vianame> <viainstancename> { /* via must be declared before */
         /* put location of the via instance here */
      }
      REGION <regionname> {
         /* put geometric description of the pattern here */
      }
      LIMIT <quantity> {
         /* put measurement definition of the quantity here */
         MIN {
            /* put calculation rule for lower limit here */
         }
         MAX {
            /* put calculation rule for upper limit here */
         }
      }
   }
}
```

A *pattern* (see IEEE Std 1603-2003, 8.29) is a geometry or a collection of geometries associated with a particular layer (referenced by <layername>).

A *region* (see IEEE Std 1603-2003, 8.31) is a geometry or a collection of geometries encompassing all layer geometries within the boundaries of the region.

The geometry of a pattern or a region is described using the *geometric model* construct (see IEEE Std 1603-2003, 9.16), which features the exact coordinates of the geometry. Alternatively, a routing geometry (i.e. a pattern related to a layer with layertype *routing*) can be described in a more abstract way using the *shape*, *vertex*, and *route* annotation (see IEEE Std 1603-2003, 8.30.2, 8.30.3, 8.30.4).

The calculation rule for the quantity subject to the design rule is described using the *arithmetic model* construct (see IEEE Std 1603-2003, 10.3). This construct supports a scalar value, a *table* of values with an associated *interpolation* scheme, or an *arithmetic expression*.

A design rule for reliability use the same template as a design rule for geometry, only the quantity is electrical *current*, as opposed to a geometric quantity *length*, *width, distance*, or *overhang*. However, the limit for electrical current can be a function of a geometric quantity.

The quantities length, distance, and overhang need to be described in a *rule* context. The quantities width and current can be described in a *layer* context, if no other objects than the layer are involved. Otherwise, they also need to be described in a rule context.

TABLE 7. Quantities for design rule descriptions

Keyword	usage	measurement definition	See IEEE Std 1603-2003
CURRENT	electrical current traversing an object	MEASUREMENT annotation (average, absolute average, rms, peak) reference to a PATTERN, if in RULE context	10.15.2 10.13.7
WIDTH	width of a routing segment	none, if in LAYER context reference to a PATTERN, if in RULE context	10.19.7
LENGTH	length of a routing segment	reference to a PATTERN	10.19.8
	common run length between two routing segments	BETWEEN construct involving two objects of type PATTERN	10.20.4

TABLE 7. Quantities for design rule descriptions

Keyword	usage	measurement definition	See IEEE Std 1603-2003
DISTANCE	distance between two objects	BETWEEN construct involving two objects of type PATTERN, REGION, or via instance	10.19.9 10.20.4 10.20.5 10.20.6
		MEASURE annotation (euclidian, manhattan, horizontal, vertical)	
		REFERENCE annotation container	
OVERHANG	overhang between two objects	BETWEEN construct involving two objects of type PATTERN	10.19.10 10.20.4

4.0 Other items

4.1 Other terminology

TABLE 8. Other terminology

Term	Explanation	Comment
unit	description of measurement units for geometric and electrical quantities	
layer visualization		
grid representation		
non-rectilinear geometry		
mask options		

4.2 Other description in ALF

FIGURE 5. Other template in ALF

```
LIBRARY <libraryname> {
   /* put global information (e.g. units) here */
   /* put layer declarations here */
   /* put declaration of other objects (e.g. vias) here */
}
```