Overview

This document presents library characterization and modeling items related to timing, power, signal integrity, reliability, yield and others. The items are presented in tables, associated with a rank. The rank indicates the subjective importance of the item (1=high, 1.5=high/middle, 2=middle, 2.5=middle/low, 3=low). An explanation for each table item is provided (not yet complete).

Timing

Table 1: Library items for timing

item	rank
delay, slewrate, setup, hold	1
data = f(voltage, temperature)	1
IR drop and ground bounce (static and transient)	1.5
distributed load (instead of lumped cap)	2
simultaneous switching (timing)	2
non-linear pin capacitance c=f(voltage) etc	2
different methods for setup/hold (independent or in conjunction with each other)	2
on-chip variations	2
Component-specific characterizations of complex blocks (abstraction eg. ILM, black box etc)	2.5
Temperature inversion	2.5
multiple clock domains (?)	3
data-dependency of timing for self-timed devices	3

Delay, slewrate, setup, hold

Delay, slewrate, setup and hold are the basic timing characterization data.
For setup and hold there exist methods of independent as well as interdependent characterization.
Definition of thresholds for timing measurement should be represented and used consistently in the library.

Data = f(voltage, temperature)

Timing data (and to a slightly lesser extend) power, signal integrity and reliability data should be characterized as a function of supply voltage(s) and/or environmental temperature. This leads typically to 4 or more characterization dimensions (input slew and output load cap being the two basic characterization dimensions).
Another "characterization dimension", albeit without interpolation or curve fitting, is the process corner.
Selection of significant characterization points and appropriate fitting into polynomials or accurate interpolation are important aspects in this context.

IR drop and ground bounce (static and transient)

This item has implications on timing, power and signal integrity. Timing, power and noise calculations should consider IR drop (by virtue of voltage-dependent characterization).
Static IR drop can use power characterization data from the library. Transient IR drop can also use timing characterization data. Possibly, additional data (e.g. current waveforms) could be characterized, especially for complex blocks.

Distributed load (instead of lumped cap)

Cells are characterized with lumped cap as load. For interconnect analysis, a discrete set of RC elements is transformed into an "effective capacitance" (Ceff). Need to study whether this approach can be maintained for typical interconnect topologies for 90nm. Maybe new parameters have to be introduced in the characterization space.

Power

Table 2: Library items for power

item	rank
electrical power	1

Table 2: Library items for power

item	rank
multiple power supplies	1
data = f(voltage, temperature)	1.5
switching activity (needs more definition)	1.5
IR drop and ground bounce (static and transient)	1.5
simultaneous switching (power)	1.5
data-dependency of power consumption	2
Component-specific characterizations of complex blocks	2.5

Electrical power

Power can be divided into subcategories: leakage, switching, internal.
Switching power is associated ith charge/discharge of external load capacitance.
Internal power is associated with short-circuit current and charge/discharge of internal capacitances.
Leakage power is dependent on transistor threshold voltages.
Switching and internal power, and to a lesser degree leakage power, are state-dependent.

Multiple power supplies

Multiple power supplies for a cell (e.g. level shifter, back-biasing) require each power supply voltage to become a characterization variable.
Association of rails with pins and with modes of power consumption is required in the library.

Simultaneous switching (power)

Simultaneous switching inputs, or inputs switching close in time may lead to spuriousoutput or internal switching activity, also called glitch. The power consumption due to a glitch needs to be accounted for.

Switching activity (needs more definition)

Statistical or heuristic modeling of cell output and internal switching activity and its associated power consumption as a function of input switching activity.

Signal integrity

Table 3: Library items for signal integrity

item	rank
xtalk noise	1
Noise-related modeling: need better model for driver and receiver (Miller-effect?)	1
data = f(voltage, temperature)	1.5
IR drop and ground bounce (static and transient)	1.5
on-chip variations	2
distributed load (instead of lumped cap)	2
charge sharing (dynamic logic, transmission gates)	2
Inductance	2
Component-specific characterizations of complex blocks	2.5

Xtalk noise

Sub-items: Noise generation, noise detection, noise propagation.
Cell characterization for noise generation requires hold resistance or I/V curve, possibly state-dependent.
Cell characterization for noise detection involves noise-margin or noise-rejection.

Cell characterization for noise propagation: output noise peak, output noise width, input-to-output delay of noise waveform dependent on input noise peak, input noise width, output load capacitance. Possibly, time-to-peak can be characterized as well.
Additional characterization variables: voltage, temperature.

Noise-related modeling: need better model for driver and receiver (Miller-effect?)

This is related to noise generation. The electrical model of a aggressor/victim scenario (possibly involving multiple aggressors) has a significant impact on accuracy.
Eventually, we want to characterize also I/O cells which drive off-chip load, e.g. transmission lines with mis-matched impedance.

Reliability

Table 4: Library items for reliability

item	rank
electromigration (signal, power, cell)	1
data = f(voltage, temperature)	1.5
Radiation	2
Hot electron (NMOS)	2
Component-specific characterizations of complex blocks	2.5
Thermal instability (PMOS)	3

Yield

Table 5: Library items for yield

item	rank
on-chip variations	2
Characterization margins	3

Other items

The following items have not yet beeen discussed and ranked.

- Description of functionality
- DFT (since not enough data in .lib)
- Types, attributes, basic structure of a library model
- Design rules, electrical constraints (max cap etc).