Library Harmonization project

Design Objective Document

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1.0 Introduction

1.1 Scope

The scope of this project is to establish a requirement specification for the contents of an EDA library for structured and cell-based IC design.This EDA library contains characterization models for timing, power, signal integrity, reliability etc., as needed by IC implementation tools such as physical synthesis, timing and electrical analysis, layout optimization etc.

Furthermore, this project shall establish a cross-reference between the library formats liberty [] and ALF [] within the scope of the targeted library contents. This is accomplished by breaking dow the required library contents into items that can be described by atomic contructs in liberty and ALF, creating these constructs and relating them to the required library contents.

By describing the EDA library contents

a) as a requirement specification in english language

b) as a construct in the aforementioned library formats

the reader can easily distinguish between format and contents. Implicit semantics associated with the usage model of a particular library format are exposed and documented.

1.2 Purpose

The purpose of this project is library harmonization, i.e., achieve consensus on EDA library requirements in the industry and facilitate the implementation of high-quality EDA libraries according to these requirements.

Without libary harmonization, fragmented library solutions would continue to emerge and too-specific library formats and versions would be perpetuated. Symptoms of such a situation are the following:

- Library format versions change frequently.
- Tool-specific library generation tools are offered together with a tool.
- Different tools interpret the same or seemingly equivalent data in a different way.

Many formats and description vehicles have been proposed for EDA library contents in the industry. The formats liberty and ALF have been chosen within this project for the following reason:

- Liberty is the most widely used EDA library format in the industry. It has evolved from a proprietary format into an open source format. In recent years, liberty has evolved from a synthesis-centric format to a format that strives to accomodate all EDA applications in the RTL to physical IC implementation space.
- ALF is the most comprehensive library format and a formal IEEE standard. It has in many ways anticipated and exceeded the library contents requirements for modern EDA tools, and it is proven by industry applications.

Therefore Liberty and ALF are the natural candidates for providing a reference to the industry in terms of EDA library contents.

2.0 Technical approach

2.1 Itemization of library contents

The following domains for library contents have been identified:

- Timing
- Power
- Signal integrity
- Electromigration
- Yield
- Other

For each domain a table of items is created, and these items are subjectively ranked as follows (1=high, 1.5=high/middle, 2=middle, 2.5=middle/low, 3=low)

The purpose of the ranking is to establish a priority in terms of developing the project deliverables associated with the item.

For each item, the deliverable shall consist of the following:

1. a requirement specification
2. a breakdown into sub-items
3. atomic Liberty and ALF constructs for each subitem
4. formal explanation of each sub-item

The idea is to deliver on the items with priority 1, 1.5 and 2 first.

During the work, it is possible to discover insufficiencies of the currently available Liberty and/or ALF specifications to adequately describe particular items. For such items, deliverable 3 shall be replaced by a requirement specification for a Liberty and/or ALF construct.

2.2 Timing

item	rank
delay, slewrate, setup, hold	1
interoperability with SDF, i.e., IEEE std 1495-2002	1
data = f(voltage, temperature)	1
IR drop and ground bounce (static and transient)	1.5
distributed load (instead of lumped cap)	2
simultaneous switching (timing)	2
non-linear pin capacitance c=f(voltage) etc	2
different methods for setup/hold (independent or in conjunction with each other)	2
on-chip variations	2
Component-specific characterizations of complex blocks (abstraction eg. ILM, black box etc)	2.5
Temperature inversion	2.5
multiple clock domains (?)	3
data-dependency of timing for self-timed devices	3

2.2.1 Delay, slewrate, setup, hold

Delay, slewrate, setup and hold are the basic timing characterization data.

For setup and hold there exist methods of independent as well as interdependent characterization.

Definition of thresholds for timing measurement should be represented and used consistently in the library.

Conditional timing arcs.

2.2.2 Interoperability with SDF

Should include all SDF 3.0 measurements: recovery, removal, pulsewidth, skew, period, retain. Interdependent measurement data are represented in SDF as setuphold (interdependent setup and hold), recrem (interdependent recovery and removal).

2.2.3 Data = f(voltage, temperature)

Timing data (and to a slightly lesser extend) power, signal integrity and reliability data should be characterized as a function of supply voltage(s) and/or environmental temperature. This leads typically to 4 or more characterization dimensions (input slew and output load cap being the two basic characterization dimensions).

Another "characterization dimension", albeit without interpolation or curve fitting, is the process corner.

Selection of significant characterization points and appropriate fitting into polynomials or accurate interpolation are important aspects in this context.

Other parameters: related to vt, back bias ...

On-chip process variation parameters: geometry ...

2.2.4 IR drop and ground bounce (static and transient)

This item has implications on timing, power and signal integrity. Timing, power and noise calculations should consider IR drop (by virtue of voltage-dependent characterization).

Static IR drop can use power characterization data from the library. Transient IR drop can also use timing characterization data. Possibly, additional data (e.g. current waveforms) could be characterized, especially for complex blocks.

2.2.5 Distributed load (instead of lumped cap)

Cells are characterized with lumped cap as load. For interconnect analysis, a discrete set of RC elements is transformed into an "effective capacitance" (Ceff). Need to study whether this approach can be maintained for typical interconnect topologies for 90nm. Maybe new parameters have to be introduced in the characterization space.

2.3 Power

item	rank
electrical power	1
multiple power supplies	1
data = f(voltage, temperature)	1.5
switching activity (needs more definition)	1.5
IR drop and ground bounce (static and transient)	1.5
simultaneous switching (power)	1.5
data-dependency of power consumption	2
Component-specific characterizations of complex blocks	2.5

2.3.1 Electrical power

Power can be divided into subcategories: leakage, switching, internal.

Switching power is associated ith charge/discharge of external load capacitance.

Internal power is associated with short-circuit current and charge/discharge of internal capacitances.

Leakage power is dependent on transistor threshold voltages.

Switching and internal power, and to a lesser degree leakage power, are state-dependent.

2.3.2 Multiple power supplies

Multiple power supplies for a cell (e.g. level shifter, back-biasing) require each power supply voltage to become a characterization variable.

Association of rails with pins and with modes of power consumption is required in the library.

2.3.3 Simultaneous switching (power)

Simultaneous switching inputs, or inputs switching close in time may lead to spuriousoutput or internal switching activity, also called glitch. The power consumption due to a glitch needs to be accounted for.

2.3.4 Switching activity (needs more definition)

Statistical or heuristic modeling of cell output and internal switching activity and its associated power consumption as a function of input switching activity.

2.4 Signal integrity

item	rank
xtalk noise	1
Noise-related modeling: need better model for driver and receiver (Miller-effect?)	1
data = f(voltage, temperature)	1.5
IR drop and ground bounce (static and transient)	1.5
on-chip variations	2
distributed load (instead of lumped cap)	2
charge sharing (dynamic logic, transmission gates)	2
Inductance	2
Component-specific characterizations of complex blocks	2.5

2.4.1 Xtalk noise

Sub-items: Noise generation, noise detection, noise propagation.

Cell characterization for noise generation requires hold resistance or I/V curve, possibly state-dependent.

Cell characterization for noise detection involves noise-margin or noise-rejection.

Cell characterization for noise propagation: output noise peak, output noise width, input-to-output delay of noise waveform dependent on input noise peak, input noise width, output load capacitance. Possibly, time-to-peak can be characterized as well.

Additional characterization variables: voltage, temperature.

2.4.2 Noise-related modeling: better model for driver and receiver (Miller-effect?)

This is related to noise generation. The electrical model of a aggressor/victim scenario (possibly involving multiple aggressors) has a significant impact on accuracy.

Eventually, we want to characterize also I/O cells which drive off-chip load, e.g. transmission lines with mis-matched impedance.

2.5 Reliability

item	rank
electromigration (signal, power, cell)	1
data = f(voltage, temperature)	1.5
Radiation	2
Hot electron (NMOS)	2
Component-specific characterizations of complex blocks	2.5
Thermal instability (PMOS)	3

2.6 Yield

item	rank
on-chip variations	2
Characterization margins	3

2.7 Other items

The following items have not yet beeen discussed and ranked.

item	rank
Description of functionality	TBD
DFT	TBD
Types, attributes, basic structure of a library model	TBD
Design rules, electrical constraints (max cap etc).	TBD
Format extensibility	TBD
Calculation methods (table, equation etc.)	TBD