Design Constraint Conceptual Model

Outline: July 6, 1998

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I About This Document

/* A overview description of the document */

- I.1 **Purpose** /* purpose of the model */ The attempt of this document is to provide a Design Constraint Conceptual Model that:
- visualize the essentials that capture the designer's intent
- analyze the ways constraints are prescribed
- explore an information model to categorize constraints
- consolidate a common framework of working concepts

The model does not mean to:

- suggest the specific mechanisms to capture or transform design constraints
- purpose schema for a repository database

I.2 Scope

/* The scope of the model */

- I.3 Reference
 [1] Any reference
 [2]
- I.4 Revision History
- Rev.0.1 July 6, 1998draft outline

II Overview

/* Provide an analysis on the nature of design intents and their relationship with design constraints $\ast/$

II.1 Design Intents

- Why is it important to capture and preserve design intents?
- The nature of design intents
- How the design constraints can be structured to reflect design intents?
- Programmatic aspects

II.2 Constraint Domains

II.3 Constraint Abstract Models

- How the constraints are prescribed **Prescription Model**
- How are the constraints transformed along with transition in level of design abstraction **Transformation Model** incorporating Enrico's material
- How are the constraints applied to design hierarchy **Hierarchy Model**
- How are the constraint data organized Information Model
 - Syntactical rules
 - Semantic rules
 - File organization

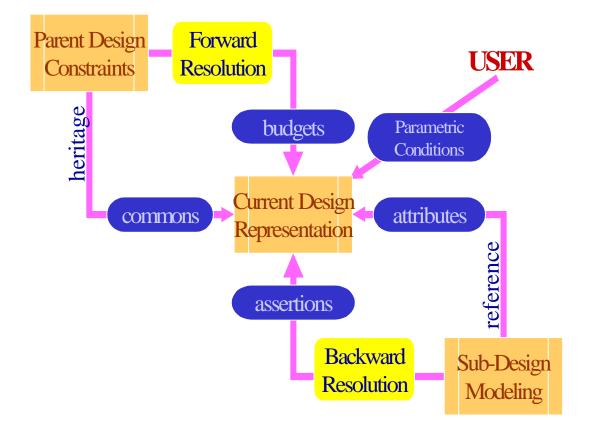
II.4 Methodology Implications

/* How these models fit in with Taxonomy, Language, Tools, EDA environments, etc. */

III Prescription Model

- Commons: Rules, Constants and Variable Assignments inherited from parent design
 - Technology Constants and Rules
 - Operating Conditions
 - Global Signals definition
- **Budgets**: forward constraint resolution -- propagated downward from parent design
 - Timing, Area, and Power Budgets
 - Floorplan and Wiring Models
- Assertions: backward constraint resolution -- surfaced upward from child designs
 - Clocking: skew, setup, hold, etc.
 - Local partial clocktree and power rings
 - Input arrival times, output required times, etc.
 - Signal Integrity Criteria
- Attributes: port level conditions extracted from or assumed for sub-module design implementation
 - Physical: location, orientation, shape and blockage
 - Estimated Wire Load Model
 - Design for Test
 - Port level Parasitic Conditioning
- Parametric Conditions (Constriction?):
 - ♦ Architecture/Logic Variables
 - Boundary Conditions

- ♦ Special Conditions
- Don't care conditions



- Mutually exclusive conditions
- Infeasible states (false paths, feedback loops)
- Detailed Implementation Controls
- File Pointers: parasitics, scripts, detailed wiring, etc.

Toshiba proprietary format for cell library characterization data

IV Transformation Model

- IV.1 Transition in design level of abstraction
- V Hierarchy Model

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VI Information Model

VII Future Works