Operating Conditions

Background

Traditionally the semiconductor industry considers process, voltage & temperature as operating conditions.
A given technology is characterized at desirable operating condition values and customers accept that their product will work if analysis verifies that it operates at these operating conditions.

Voltage was usually targeted at 5V systems with supplies regulated to +/- 10%.

From the application side temperatures were picked to match military or commercially specified extremes for ambient conditions. Or from the technology side transistors are characterized at a junction temperature (Tj) and working inside-out a package is selected considering the application power and desired ambient environment. In most cases fabricators regarded these design points as pessimistic enough to guardband against failures due to noise coupling in the voltage supply or localized thermal ‘hot spots’ on the die.

Operating Conditions

Background Cont'd -

In IBM's case, process variation for ASIC customers is typically expressed as statistical factors plugged into timing analysis. Customers can negotiate process variations but the cost model moves from ASIC business to another semi-custom model.

Based on conversations with colleagues at IBM I've learned of the following customer requirements that cause us to change how we traditionally view operating conditions. We see a growth in battery-powered applications and the use of core (including analog) building blocks as driving changes to design system requirements.

Operating Conditions

VOLTAGE -

Basically with only one voltage to worry about die makers could dedicate more of the chip resources to power distribution. But that is changing.

Voltage Islands -
Customer want to specify that portions of their design run at a different voltage than other portions. These voltages have separate power inputs and possibly grounds and deviate independantly of each other.

Voltage islands specified in the RTL design at arbitrary hierarchical level and in the netlist it's inherited downward.

Same library cells within a design bound to different voltages by instance.

Those cells are interfacing to cells at different voltages (e.g. different switching levels)

Operating Conditions

Voltage Cont'd -

Rails
In a proposed solution actual operating voltage is no longer built into the cell delay representation, instead it's deferred.

We separate actual voltage value from power distribution (the term is rail) and that value is specified on a per instance basis. It is an additional complication in that not all possible

Operating voltages may not be uniformly distributed across the die so operating voltage contstraints may impart placement constraints

Derating Voltage vs Performance
In some cases the same macro design runs at different performance levels but operating condition constraints tighten for higher performance levels.

Operating Conditions

Voltage Cont'd -

Noise
As operating voltages decrease and operating frequency increases the noise margin is no longer negligable and decoupling of the voltage supply becomes more of an art form, **noise** will probably be a component of the overall specification.

The same may be assumed for IR (current x resistance) drop.

On chip regulation

Differential logic operation
Two voltages are introduced (let's call the V1 & V2).
- Some logic operates between V1 - GND
- Some logic operates between V2 - GND
- Some logic operates between V1 - V2

Analog/Mixed signal core applications
Require separate voltage and grounds with additional constraints on resistance (or length) of nets leading in/out.

Operating Conditions

Temperature

Temperature deviations on chip have always existed but have been traditionally ignored. But that is changing..

In advanced technologies temperatures may not distribute evenly across the die as easily. Localized hot spots are no longer negligable.

Temperature gradients as a function of switching activity may be required for accurate delay calculation.
Seeing potential for much more accuracy in NDR's if localized temperature gradients are understood.

Some increase in non-military space applications. Extreme temperature conditions.

Operating Conditions

Power

Widely viewed as a operating condition design constraint closely related to temperature.

Process Variations

K-factors

One colleague pointed out the difference between ‘observable’ and ‘non-observable’ constraints and suggested that process is non-observable.