

ОВИ

Design Constraint Working Group

— Group Charter, Scope and Deliverables —

May 11, 1998: revised initial draft

Charter

The **Design Constraints Working Group** is chartered with developing a **Design Constraint Specification Standard**. The Standard, which encompasses a constraint description language, a constraint semantic dictionary, and a constraint conceptual model, is intended for the prescription, representation, and preservation of the “**design intent**” throughout the **implementation cycle** of an electronic system or subsystem design. (Note: we have a bit of a conflict here because the SLDL folks want us to cover system level constraints but the RAIL folks won’t. I’d say it’s ok to leave it as is, but we’ll have to be careful to look at the relationship with RAIL.)

The design intent, typically expressed in a collection of constraints, assertions, and environment conditions, is the manifestation of system level design requirements other than the logical functionality. Logical functionality is expressed in design languages such as Verilog and VHDL that are covered by other standards. As the implementation of the design progresses, the design intent may expand to cover more detailed aspects of the desired implementation, and the original system level design requirements may be modified and transformed in various ways.

This Working Group envisions the need to establish a common framework across the industry for capturing and transferring design intent, independent of application tools or design processes. The key objectives of the Standard are to:

- ❑ Identify semantics and forms for expressing the design intent, which closely match designers’ needs and facilitate exchanging information between different designers as well as between designers and tools.
- ❑ Contribute to interoperability between tools.

- ❑ Apply uniformly across multiple tasks and constraint domains.
- ❑ Be compatible with existing standards (e.g. PDEF) and technologies (e.g. extension language).
- ❑ Provide for automatic consistency checking between related constraints where possible.

Related works currently deferred or excluded from the group charter are:

- ❑ Board level design constraints
- ❑ Methodology and tools for the transcription and translation of constraints when the design is mapped over to a lower level of abstraction (e.g. RTL to gate level).
- ❑ A persistent data base for the centralized repository of constraints
- ❑ Tool level constraint data exchange format (such as GCF)

Scope

The standard should be language-independent, initially supporting chip and module level designs done in a mixture of Verilog, VHDL languages. Later work should add support for mixed-signal designs and corresponding design languages.

The standard should address required performance characteristics, implementation details, and descriptions of (as well as restrictions on) the environment in which the design is to be used.

The standard should be in consistent with exiting accredited public-domain standards, such as PDEF in physical design. In addition, there are on going standardization efforts, such as RAIL in board level design and SLDL in system level design. Their works may coincide with ours in some areas. The working group will attempt to avoid overlapping efforts with other standard organizations, while achieve semantic consistency in the areas of overlap.

Constraint Domains

Constraint domain refers to different aspects of design objectives that need to be evaluated in tandem to observe the design tradeoffs best for the design over-all.

Constraint domains considered as within the scope of this standard are:

Timing

Area

Clocking

Logic Architecture

Power
Physical Design
Signal Integrity
Test

Initial Focus

The initial focus of this working group is set as follows:

System Logic: Digital
Constraint Domain: Timing & Clocking
Design Interface: Design Reuse

Overlapping Standards

Some physical design constraints are addressed by the Physical Design Exchange Format (PDEF) standard. There is also overlap with the IEEE P1500 standard for testing embedded cores, the System Level Design Language effort, and the RAIL standard for board level constraints. DC-WG should work with these groups to define the relationships between the DC-WG standard and the other efforts.

Deliverables

Constraints Conceptual Model

A presentation that outlines the conceptual model adapted by the working group provides an architectural framework the standard is to base upon. The intent of the model is to:

- visualize the essentials that capture the **designer's intent**
- analyze the ways constraints are prescribed
- explore an information model to categorize constraints
- consolidate a common framework of working concepts

Constraint Semantics Dictionary

The dictionary is to provide standard terminology, structural relationship, and semantic definition of the generic constructs and their associated parameters used for the concise definition of design constraints.

Initially, a tabulated constraint summary will be generated to provide a concise catalog of the different types of constraints, assertions, and environment conditions. Included in the summary table will be a name for each constraint, a list of the possible parameters, and a brief description of the semantics.

Constraint Description Language

It is envisioned that any existing tool can adopt the semantics dictionary in various language implementations. A specific version of constraint description language suitable for user entry will be designed. A specification document for the language design will be provided, which should include a complete description of the syntax and semantic specific to each constraint and its parameters.

Golden Parser

A golden parser and syntax checking program for the above constraint description language will be provided. The syntax checker should read a constraint command file and report all syntax errors but will not check for semantic errors. The program will be placed in the public domain.