Constraint Taxonomy

Version 0.2

Design Constraints Working Group

Open Verilog International

Virtual Socket Interface Alliance

Revision History

Revision	Date	Name	Comments
0.2	7/6/98	Mark Hahn	Added a table of contents, clock constraints, and did some reformatting
0.1	6/8/98	Mark Hahn	Initial Creation

Table Of Contents

1. Timing Domain

1.1 Clock Constraints

Clock

Specifies a set of points in the design at which a clock waveform originates

Type Environment condition

Applies To Hierarchical pins or primitive outputs

Depends On Waveform, Derived Waveform

Verified By None

Parameters

Name	Value Type	Restrictions	Semantics
Waveform	String	Waveform can only have two edges	The name of the abstract waveform

Clock Delay

Constraint on the timing characteristics of a clock network or a portion of a hierarchical clock network

Type Constraint

Applies To Hierarchical pins or primitive outputs

Depends On Clock

Verified By Timing analysis

Parameters

Name	Value Type	Restrictions	Semantics
Root	Pin name		Name of hierarchical pin or primitive output which drives the clock network. Either a pin name or a waveform name may be specified as the root, but not both. Values specified using a pin name override those specified using a waveform name.
	Waveform name		When a waveform name is given, it specifies default values which affect all clock networks driven by that waveform, including virtual clock networks referenced in ***Arrival*** and ***Required Time*** constraints.
Analysis mode	ideal or actual		This specifies whether the ideal insertion delay, skew, and transition times within the clock network should be used, or whether the actual values should be computed. Generally the analysis mode is set to ideal prior to inserting the clock network, and actual afterwards. This overrides the default Clock Mode specification.
Explicit leaf pins	List of pin names		These override the default rules, specifying that pins which would otherwise lie within the default clock network should be treated as leaf pins, or grouping a set of default leaf pins in order to override the default constraints.
Excluded leaf pins	List of pin names		These override the default rules, specifying a group of pins which should be ignored for the purpose of computing skew. These pins may be default leaf pins or they may lie within the default clock network. The forward trace stops at these pins. Transition times may

Name	Value Type	Restrictions	Semantics
			still be specified explicitly or by default on these pins.
Default insertion delay	Float for each edge	Non-negative	The nominal cumulative delay from the root to the default leaf pins, as well as the default value for explicit leaf pins.
Explicit insertion delay	Float for each edge	Non-negative	This overrides the default, specifying a different insertion delay for a group of explicit leaf pins
Default skew	Float min, max for each edge	Non-negative	The range of differences in insertion delay allowed between any pair of leaf pins, except for the excluded leaf pins.
Explicit skew	Float min, max for each edge	Non-negative	The range of differences in in insertion delay between any pair of explicit leaf pins in a group.
Default transition time	Float min, max for each edge	Non-negative	The range of transition (ramp) times allowed at each default leaf pin, as well as the default value for explicit leaf pins.
Explicit transition time	Float min, max for each edge	Non-negative	The range of transition (ramp) times allowed at a group of explicit leaf pins.
Default overshoot limit	Float min, max		For board level analysis, the default overshoot allowed at each default leaf pin, as well as the default value for explicit leaf pins
Explicit overshoot limit	Float min, max		For board level analysis, the overshoot allowed at a group of explicit leaf pins
Active	List of rise, fall, high, low or all		This specifies the active portion of the clock for the sequential elements downstream from a group of explicit leaf pins. It is required when the leaf pins are the root of another clock network, or when the leaf pin is an output port. Rise and fall are used for edge-triggered devices, while high and low are used for level-sensitive devices.
Source arrival time	Float min, max for each edge		The nominal cumulative delay from the root of a hierarchical clock network to the root of this partial clock network. The total insertion delay to leaf pins in this partial clock network is the sum of the source arrival time and the insertion delay within this clock network.
Jitter	Float	Non-negative	Potential variation in clock period across different clock cycles.

Clock Mode

Default for whether the ideal characteristics of clock networks should be used for analysis, or whether the actual characteristics should be computed

Type Control

Applies To Design

Depends On None

Verified By None

Parameters

Name	Value Type	Restrictions	Semantics
Analysis mode	ideal or actual		This specifies the default value (for all clock networks) of whether the ideal insertion delay, skew, and transition times within the clock network should be used, or whether the actual values should be computed. Generally the default analysis mode is set to ideal prior to inserting clock networks, and actual afterwards. The default analysis mode can be overridden for particular clock trees by the ***Clock Delay*** constraint.

Derived Waveform

A waveform which is derived from another waveform (by a clock multiplier or divider, for example)

Type Environment condition

Applies To None

Depends On None

Verified By None

Parameters

Name	Value Type	Restrictions	Semantics
Parent	String		The name of the waveform from which this waveform is derived
Inverted	Boolean		Whether the derived waveform is inverted or not
Phase shift	Float		Offset from the parent waveform
Frequency multiplier	Float		Multiplier relative to parent waveform frequency. 0.5 corresponds to divide-by-two
Skew adjustment	List of floats		Additional skew. Each value is both added to and subtracted from corresponding edges in the parent waveform
	List of min/max ranges (float)		Each value is both added to and subtracted from corresponding edges in the parent waveform

Waveform

A description of an abstract waveform

Type Environment condition

Applies To None

Depends On None

Verified By None

Parameters

Name	Value Type	Restrictions	Semantics
Edges	List of floats		Offsets from an implicit reference point in time
	List of min/max ranges (float)		Offsets from an implicit reference point in time. Min/max range describes uncertainty region in which edge can occur
Domain	String		Name of a clock domain. All clocks in the same domain are synchronous with respect to each other.