IBIS Accuracy Specification

DRAFT

Revision 1.2
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1. Introduction

1.1 Accuracy Defined

In his book, "Data Reduction and Error Analysis for the Physical Sciences," author Philip Bevington offers the following definition of accuracy. "The accuracy of an experiment is a measure of how close the result of the experiment comes to the true value." An engineer might amend his definition as follows: "The accuracy of a simulation is a measure of how close the result of the simulation comes to the true value." In the case of behavioral modeling of high-speed digital circuits, the *true value* is what one accurately measures in the lab, and the behavioral simulation is a theoretical prediction. A highly accurate behavioral simulation is one in which the difference between simulation and lab data is small.

1.2 Overview

The IBIS Accuracy Specification defines a quantitative method for correlating test hardware with behavioral simulation predictions and documenting the results of the correlation. It is a document of understanding between a semiconductor vendor (the IBIS datasheet originator) and a semiconductor customer (the IBIS datasheet user). The primary application is as a reference document for specifying the purchase of semiconductor components that meet the signal integrity requirements for a given system design. Using the IBIS Accuracy Specification, the vendor can quantify how closely test hardware matches a set of "golden waveforms," and the customer can decide whether or not a given IBIS datasheet meets his or her accuracy needs. This working definition of the document necessitates the quality of built-in flexibility. The IBIS Accuracy Specification does not make requirements of an IBIS datasheet to meet a given level of accuracy; it merely provides a method for quantifying and documenting accuracy.

The method defined in this document has several components. First, the Measurement section describes which electrical parameters the originator of an IBIS datasheet should measure to validate the accuracy of the datasheet. The basic categories of parameters are IV curves, test load waveforms, and capacitance. The Measurement section also specifies techniques necessary to minimize measurement uncertainty. For example, oscilloscope and probe bandwidths must be consistent with signal rise times. Second, the Correlation section defines methods for correlating data from test hardware with golden waveforms and assigning a figure of merit to the results. Third, the Documentation section provides a template for communicating the correlation results to the user in a clear and concise manner.

Specifying a correlation procedure presents a conflict. On the one hand, the user only cares that behavioral simulations accurately correlate with device performance. On the other hand, the semiconductor vendor does not want the burden of having to correlate lab data with all available simulators, which may use different behavioral models and different circuit solution algorithms. The IBIS Accuracy Specification resolves this conflict using a two-step approach. In the first step, the semiconductor vendor correlates lab data against SPICE-based golden waveforms that are embedded in the IBIS datasheet in the form of voltage-time tables. In the second step, the user correlates behavioral simulation results against the same golden waveforms using his or her simulator of choice. This approach effectively decouples the behavioral simulator from the hardware and splits the correlation problem into independent components.

In addition to providing a reference for the purchase of semiconductor components, the IBIS Accuracy Specification has other potential applications. When a possible signal integrity problem arises, the IBIS Accuracy Specification can serve as a basis for comparison between measurements made during system debug and measurements made by the semiconductor vendor. Another possible application of the IBIS Accuracy Specification is as a quality standard for IBIS datasheets that originate from a third-party vendor (i.e., not the semiconductor vendor).

Please scan through the glossary to become familiar with the terms used in this document.

1.3 Background

The idea for an IBIS Accuracy Specification was hatched at the December 1997 meeting of the IBIS Users Group in Chelmsford, Massachusetts. Many of the attendees expressed strong concerns regarding the accuracy of presently available IBIS datasheets, and a subcommittee quickly formed with the mission of producing an IBIS Accuracy Specification in one year's time. The members of the IBIS Accuracy Subcommittee are Fawn Engelmann (CAE Engineer, EMC), Robert Haller (Hardware Principle Engineer, Compaq Computer), Bruce Heilbrunn (Customtech), Peter LaFlamme (Applications Engineer, Fairchild Semiconductor), Harvey Stiegler (Senior Member Technical Staff, Texas Instruments), and Greg Edlund (Advisory Engineer, IBM Corporation and subcommittee chairman).

1.4 Technical Challenges

The challenge of writing any specification is to clearly state only what is necessary in such a way as to minimize the opportunity for misinterpretation (which will happen occasionally in even the best-written specifications). Writing the IBIS Accuracy Specification presented some unique challenges, such as bringing IBIS accuracy from the conceptual realm into the quantitative realm. The word accuracy conjures up a vague concept of agreement between simulations and data from test hardware; what exactly does this mean, and how can one quantify accuracy?

In the process of defining IBIS accuracy quantitatively, one of the first questions the IBIS Accuracy Subcommittee had to address was scope. The effectiveness of the IBIS Accuracy Specification lies in its ability to cover the relevant electrical behavior of a given driver family. Each unique driver family requires a certain set of IBIS keywords for accurate behavioral modeling, and each unique driver family might require a unique set of test loads to elucidate the electrical behavior of that driver family. For example, modeling the circuit behavior of a simple push-pull CMOS driver requires the basic IBIS keywords: Pulldown, Pullup, GND_clamp, POWER_clamp, C_comp, C_pkg, Ramp, Rising Waveform, and Falling Waveform. Modeling the circuit behavior of a multi-stage driver requires additional keywords. What set of test loads will sufficiently cover the relevant electrical behavior of each of these types of drivers?

Another question that presented itself was how much detail to include regarding measurements. For example, when a modeling engineer is measuring dV/dt for a 0.5 ns edge, oscilloscope and probe bandwidth play a critical role in determining the accuracy of the measurement. However, the subcommittee did not wish to write a specification that was only relevant to a narrow set of test equipment. Which features of the test environment are necessary elements of the specification?

One topic that arose repeatedly during discussions of the IBIS Accuracy Subcommittee was the effects on IBIS accuracy of the simulator. Even if a modeling engineer goes to great lengths to verify the accuracy of a given IBIS datasheet on a given simulator, it is possible that the lab data may not agree with results obtained using another simulator. Each simulator must translate the IBIS datasheet into its own native model format before a simulation can begin, and this translation process is one potential source of discrepancies among simulators. Furthermore, each simulator uses its own unique numerical algorithms to arrive at the circuit solution. How could the IBIS Accuracy Subcommittee craft a specification that was independent of simulator platform?

1.5 IBIS Accuracy Test Board

The IBIS Accuracy Test Board is a companion to this specification. Its purpose is to demonstrate one possible set of test structures that facilitate measurement of the ac and dc parameters specified in this document. The schematics, Gerber files, parts list, and application note are available on the web sites listed in the "Reference" section. The board design is free. The IBIS Accuracy Subcommittee encourages any interested party to study, improve, and freely share the design to further the understanding of the IBIS Accuracy Specification.

1.6 References

I/O Buffer Information Specification 1.1, 2.1, 3.2
IBIS Cookbook 2.0
IBIS Accuracy Test Board Application Note (forthcoming)

The above documents are available on the IBIS web site: www.eia.org/eig/ibis/ibis.htm

"Measuring Parasitic Capacitance and Inductance Using TDR," David J. Dascher, Hewlett-Packard Journal, April 1996, www.hp.com/hpj/apr96/ap96a11.htm.

"Impedance Measurement Handbook," M. Honda, copyright 1986 by Yokogawa Hewlett-Packard Ltd., HP part number 5950-3000.

2. Scope

The scope of the IBIS Accuracy Specification is based on IBIS keywords and subparameters, which in turn are based on circuit behavior. Driven by the need to simulate more advanced I/O circuit designs, the list of features has grown considerably since the inception of IBIS. Although the scope of the IBIS Accuracy Specification is not yet up-to-date with the current version of IBIS, we expect the scope to grow as development continues.

Two disclaimers are in order. First, package resistance and inductance are not easily measured on a sample component. While resistance and inductance measurements are not a direct part of this specification, the other measurements will introduce discrepancies when resistance or inductance is grossly amiss. Second, the methods defined by this version of the specification *may* be used with unspecified I/O buffers families, but the IBIS Accuracy Specification makes no attempt to insure coverage of their electrical behavior by the measurements and metrics defined within. For example, the tests specified for a simple open-drain driver may be used to correlate a GTL open-drain driver, but there may be other tests necessary to cover the additional circuit behavior of the GTL driver. GTL is not yet covered by the IBIS Accuracy Specification.

2.1 IBIS Keywords and Subparameters

Table 1: IBIS Keyword and Subparameter Coverage

Keyword	Subparameter	Description
[Package]	C_pkg	Default package capacitance.
	L_pkg	Default package inductance.
	R_pkg	Default package resistance.
[Pin]	C_pin	Pin-specific package capacitance.
	L_pin	Pin-specific package inductance.
	R_pin	Pin-specific package resistance.
[Model]	C_comp	Capacitance associated with silicon.
	Model_type	Input, Output, I/O, 3-state, Open_drain.

[Pulldown]		Pull down IV curve.
[Pullup]		Pull up IV curve.
[GND clamp]		Ground clamp IV curve.
[POWER clamp]		Power clamp IV curve.
[Ramp]	dV/dt_f	Falling output edge rate measured at 20-80%.
	dV/dt_r	Rising output edge rate measured at 20-80%.
[Falling Waveform]	R_fixture	Voltage vs. time waveform for falling edge.
	V_fixture	
[Rising Waveform]	R_fixture	Voltage vs. time waveform for rising edge.
	V_fixture	

2.2 Circuit Behavior

2.2.1 Simple Push-Pull Driver

The IBIS Accuracy specification covers driver designs employing a transistor that pulls up to the positive rail and a transistor that pulls down to the negative rail. The simple push-pull driver does not employ any impedance control, edge-rate control, or feedback circuitry.

2.2.2 Simple Open-Drain Driver

The IBIS Accuracy specification covers driver designs employing a transistor that pulls down to the negative rail. The simple open-drain driver does not employ any impedance control, edge-rate control, or feedback circuitry.

3. Measurements

Section Three defines a set of measurements that the modeling engineer may use to extract the data defined by the keywords and subparameters in the Scope section of this document. The three subsections are IV curves (dc), test load waveforms (transient), and capacitance (transient and ac). In addition to the 50 Ω loads specified by IBIS, there are three extra test loads that serve to crosscheck the data from each of the three categories of measurements. These extra test loads are the open-ended transmission line, the transmission line/receiver, and the standard load.

3.1 Look-up Table

The following look-up table specifies a correspondence between circuit behavior from section 2.2 and measurements from section 3. An "X" in a cell designates that the measurement indicated by the row header is necessary to insure the accuracy of the circuit behavior indicated by the column header. For example, a simple push-pull driver (2.2.1) requires a full set of IV curves, five test loads, and a capacitance measurement. A simple open-drain driver (2.2.2) requires a smaller subset of these

measurements and some unique test loads because it only has a pull-down device and needs an off-chip pull-up resistor to function.

Table 2: Measurement Look-Up Table

Measurement	Description	Push-Pull 2.2.1	Open-Drain 2.2.2
3.3.1	Input IV curve	X	X
3.3.2	Tri-state IV curve	X	X
3.3.3	Pull-down IV curve	X	
3.3.4	Pull-up IV curve	X	X
3.4.1	50 Ω to ground	X	
3.4.2	50 Ω to VDD	X	X
3.4.3	Open-ended t-line	X	
3.4.4	T-line and receiver	X	
3.4.5	Standard load	X	X
3.4.6	Open-ended t-line		X
3.4.7	T-line and receiver		X
3.5.1(2)	Capacitance	X	X

3.2 Measurement Techniques

3.2.1 IV Curve Measurement Techniques

There are three important considerations related to accurately measuring IV curves: range, resolution, and line drop.

It is important to sweep the current (or voltage) far enough to turn on any clamp diodes that are connected to the power or ground rails. The IBIS Accuracy Subcommittee recommends sweeping out to the vendor's absolute minimum and maximum current specifications. It is not necessary to sweep the voltage from -Vdd to +2 Vdd as specified by IBIS if doing so would push the component beyond its absolute minimum or maximum current specification.

Using adequate current and voltage resolution will ensure that significant features of the IV curve do not fall between data points. The IBIS Accuracy Subcommittee recommends a minimum delta-current of 1 mA and a minimum delta-voltage of 50 mV for IV curve measurements, regardless of whether the sweep variable is current or voltage. These values need not be consistent with the corresponding delta-current and delta-voltage in the IBIS datasheet. Model vendors often filter the data points and only include those that are deemed significant. If this is the case, the modeling engineer must take care to accurately interpolate between data points.

Depending on the length and cross-sectional area of the wire between the instrument and the DUT, line drop may introduce a significant error into the IV measurement. The modeling engineer must calculate or measure line drop. If it is greater than 5% than any voltage in the IV curve, the modeling engineer must use a four-point probe, as demonstrated in the second schematic in section 3.1.1.

3.2.2 Test Load Measurement Techniques

There are six important considerations related to accurately measuring voltage-time waveforms for a given test load: bandwidth, resolution, probe characteristics, PC board characteristics, period, and simultaneous switching.

Assuming a Gaussian edge, there is a simple relationship between the 10-90% rise time of a signal and its frequency content ["High-Speed Digital Design," Johnson and Graham, equation 3.2].

$$T_{rise} = \frac{0.338}{F_{3dB}}$$

For example, a 0.5 ns edge requires a scope whose bandwidth is *at least* 676 MHz:

$$F_{3dB} = \frac{0.338}{T_{rise}} = \frac{0.338}{0.5ns} = 676MHz$$

If the aggregate bandwidth of the oscilloscope and the probe is not high enough for the rise time in question, high frequency components of the waveform will be attenuated, and the measurement will be in error. The following equation expresses the measured rise time as a function of the "true" rise time, the oscilloscope bandwidth, and the probe bandwidth ["High-Speed Digital Design," Johnson and Graham, equation 3.7].

$$T_{measured} = \sqrt{{T_{rise}}^2 + \left(\frac{0.338}{F_{3dBscope}}\right)^2 + \left(\frac{0.338}{F_{3dBprobe}}\right)^2}$$

Even if the bandwidth of the oscilloscope and probe are high enough to accurately measure a clean edge, it is possible they may not be high enough to accurately capture inflections in the waveform that have a frequency content even higher than that of the edge itself. An accurate SPICE model of the I/O buffer and its package can indicate when a high-frequency inflection may be present. Simulating the network with an equivalent RLC circuit model for the probe can elucidate the effects of its bandwidth on the signal passed to the oscilloscope.

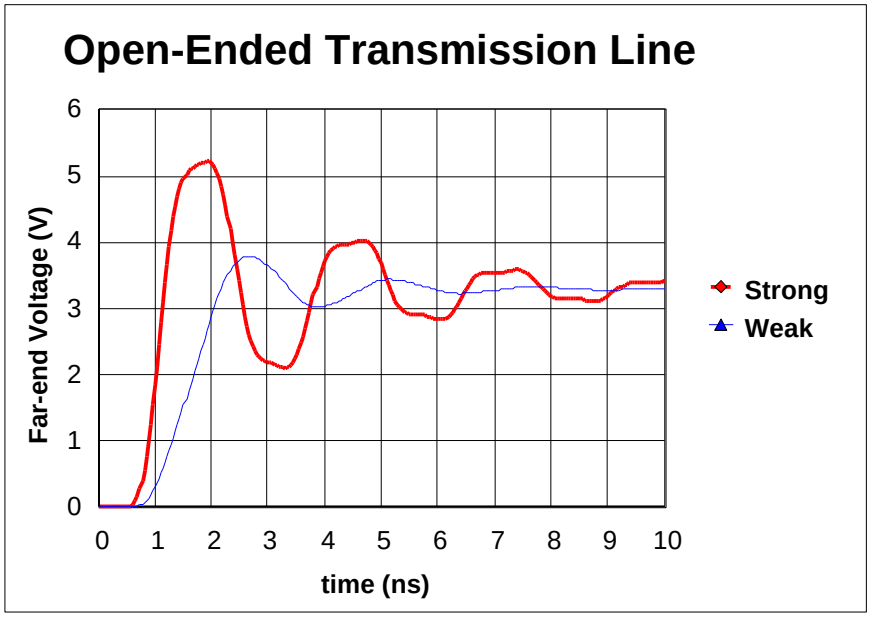
Like the IV curve measurements, the voltage-time waveform measurements require adequate voltage and time resolution. The IBIS Accuracy Subcommittee recommends setting the voltage and time per division on the oscilloscope so as to facilitate at least ten data points per edge. More data points are required if the waveform contains high-frequency inflections.

It is important to know the probe capacitance and include it in the correlation simulations. This may mean constructing a special test structure to measure the probe capacitance if a vendor specification is not available or reliable. Probe inductance is *absolutely critical*. The modeling engineer should use a probe and probe jack that minimize the length of the inductive loop formed by the signal conductor and its ground return conductor (represented by L1 and L2 in the test load schematics above). Such probes usually integrate the signal and ground conductors into one unit.

Unknown PC board impedance and propagation delay can also introduce errors into the correlation process. Therefore, it is important to measure the impedance and propagation delay of the transmission

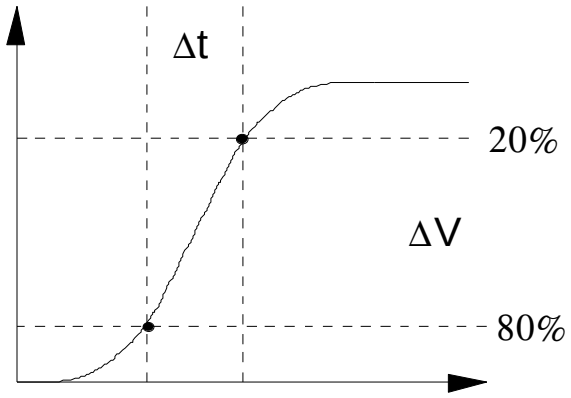
lines using a TDR and include the measured values in the correlation simulations. In cases of extreme rise times, it may also be important to measure the capacitance of vias and surface-mount pads.

In the open-ended transmission line load, it is important to design the transmission line impedance high enough relative to the driver's output impedance so as to create multiple reflections on the transmission line. This will facilitate crosschecking of the driver's complex reflection coefficient. The waveform should look similar to the one shown below.



In the Transmission Line and Receiver load, the transmission line impedance should be high enough to allow the clamps to turn on, if they exist. Set the period of the input signal slow enough to allow the waveform to settle out to its dc state before it begins switching again. Finally, only switch one output at a time. This will minimize any errors introduced by power and ground rail collapse when multiple outputs switch at the same time.

The figure below demonstrates how to measure dV/dt_r using the 50 Ω to Vdd test load. The 20% and 80% lines are relative to the *loaded* dc high level rather than the *unloaded* dc high level.



3.2.3 Time Domain Capacitance Measurement Techniques

The time domain technique involves sending a TDR pulse down two transmission lines that are identical with the exception of the presence or absence of the DUT at the end of the line. (See "Measuring Parasitic Capacitance and Inductance Using TDR," listed in the references.) The waveforms from these two measurements are then overlaid on the same x-y plot. The area between the two curves equals the product of the load capacitance, the transmission line impedance, and the voltage step size. This relationship holds even in the presence of package inductance. Note that it is not possible to distinguish between die and package capacitance. One can only measure the sum of C_comp and C_pin (or C_pkg).

$$C_{lab} = \frac{1}{Z_o V_{step}} \int V_{unloaded}(t) - V_{loaded}(t) \cdot dt$$

[Insert plot: TDR waveforms]

There are three important considerations related to accurately measuring capacitance in the time domain. First, both traces on the printed circuit board must be identical to each other. This means they must lie on the same layer and have identical geometrical dimensions. Second, each trace should be sufficiently far away from neighboring traces as to make crosstalk insignificant. A simple crosstalk computation is in order here. Third, the traces should be long enough relative to the TDR rise time so as to allow the operator to distinguish between the discontinuity of the test jack and the reflection from the end of the line.

It is imperative the capacitance measurements be made while the DUT is powered up as semiconductor junction capacitances are bias-dependent.

3.2.4 Frequency Domain Capacitance Measurement Techniques

The frequency domain capacitance measurement is considerably more complicated than the TDR capacitance measurement. It employs an auto-balancing bridge instrument, which compares the amplitude and phase response of the unknown impedance with a known sinusoidal signal. (See "Impedance Measurement Handbook," listed in the references.) Because the auto-balancing bridge creates a virtual ac ground, the measurement is sensitive to grounding. The ac isolation box provides a high impedance at the test frequency between the DUT and the power supply; this keeps the ac signal local to the DUT.

Besides ac grounding, there are two other important considerations related to accurately measuring capacitance in the frequency domain: calibration and ac signal. The frequency-domain measurement requires both open-circuit and short-circuit calibration structures in addition to the loaded structure. Like the time-domain technique, all three traces on the printed circuit board must be identical to each other and sufficiently far away from neighboring traces as to make crosstalk insignificant. The short-circuit calibration structure should have a ground via at the connector center pin. The amplitude of ac signal should be low enough so as not to turn any clamp diode junctions. It may also be important to apply a dc bias that is consistent with logic high and low voltages if the capacitance is sensitive to dc bias.

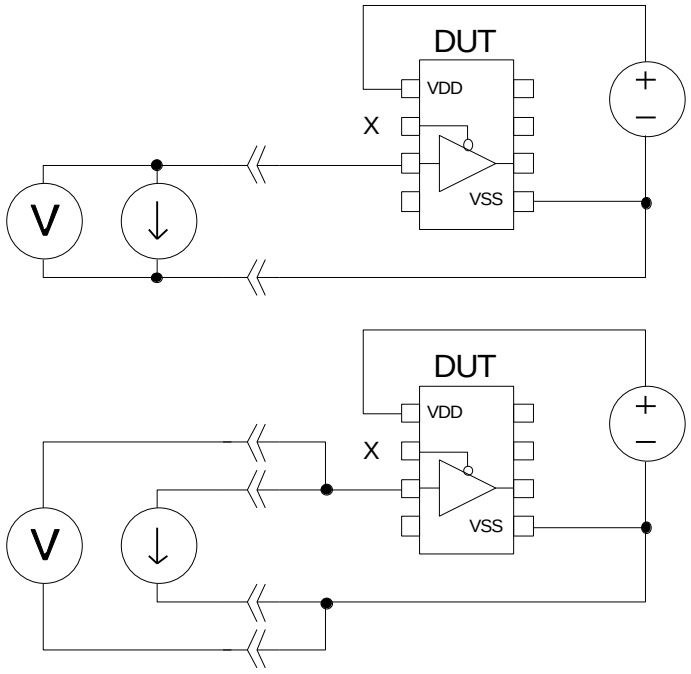
3.3 IV Curves

IV curves form the foundation of any behavioral model. They describe the dc characteristics of the I/O structures seen looking into the pin of a component. The IV curves define the impedance characteristics of the I/O buffer in a dc sense. In the case of the simple push-pull output buffer, the IV curves are the drain current vs. drain-source voltage characteristics of the pull-up and pull-down FETs with a fixed gate voltage. In the case of a simple input buffer with clamp diodes, the IV curves are the diode terminal current vs. junction voltage characteristics, equivalent to the classical diode equation. IV curves are the

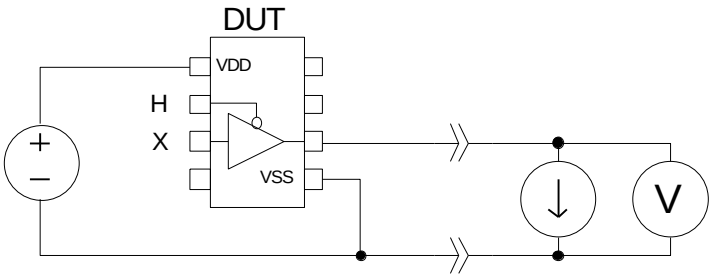
simplest of the three categories of measurements, and they are essential for successful correlation of the other measurements.

The IV curve measurements cover the IBIS keywords Pulldown, Pullup, GND lamp, and POWER clamp.

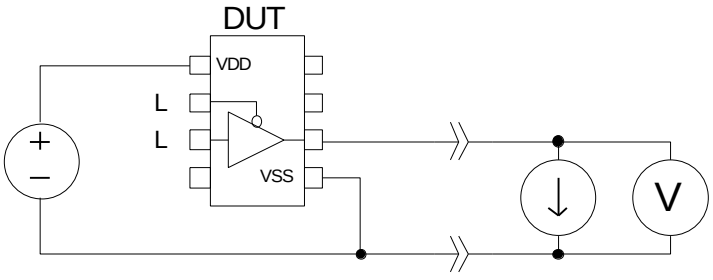
3.3.1 Input



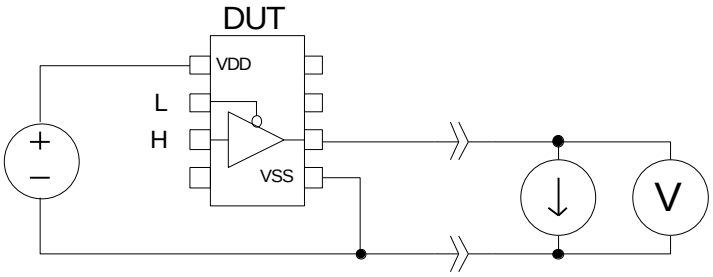
3.3.2 Tri-State



3.3.3 Pull-Down



3.3.4 Pull-Up



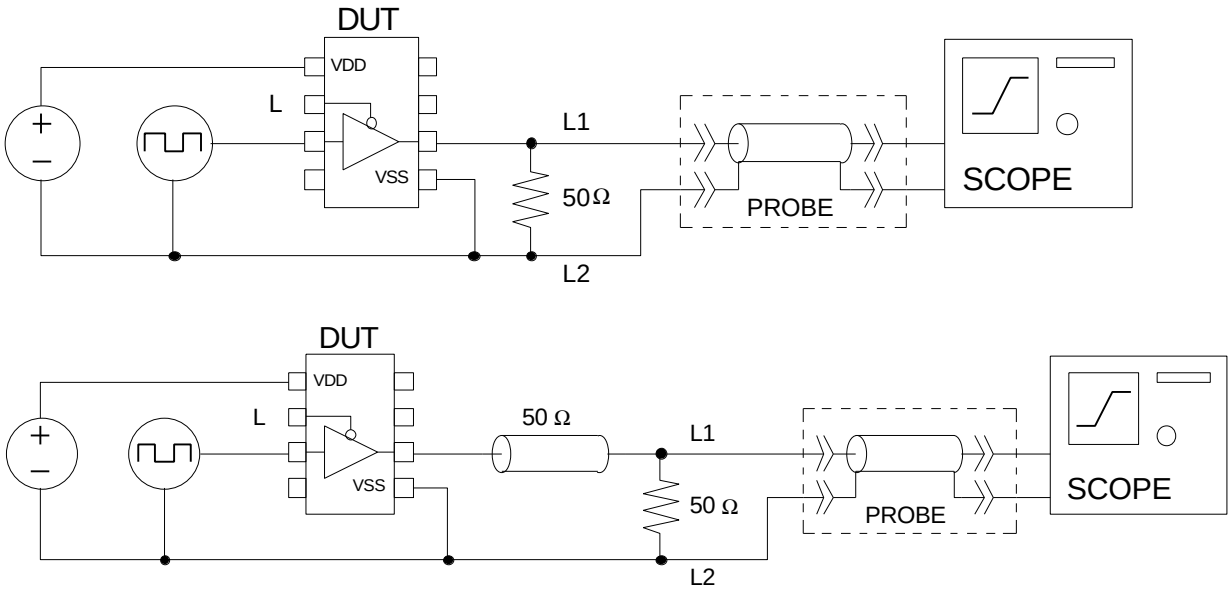
3.4 Test Load Waveforms

Voltage-time waveforms into a specified test load are the next most complicated measurements following IV curves. The first two waveforms of interest are the test loads IBIS uses to specify edge rates and voltage-time (VT) tables, namely 50 Ω to ground and 50 Ω to Vdd. Edge rates are the second essential piece of information in a behavioral model. Note that schematics for measurement 3.4.1 demonstrate two electrically equivalent loads that may be used interchangeably depending on board placement constraints.

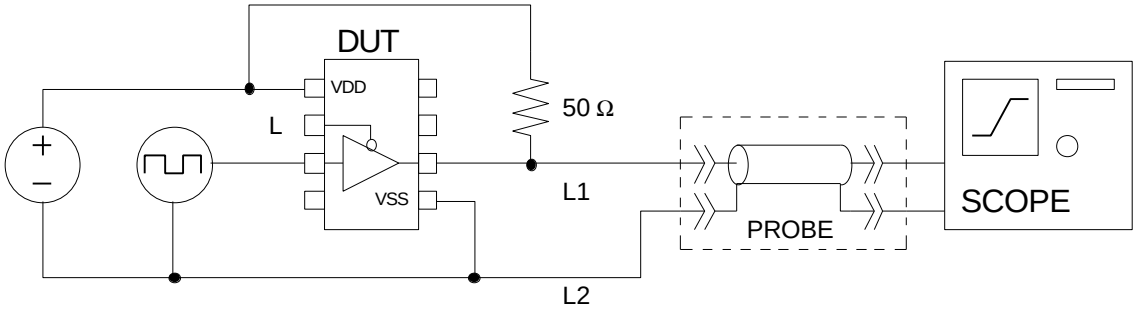
The remaining three test loads are not yet found in IBIS but are essential to insuring the accuracy of an IBIS datasheet. The open-ended transmission line tests the complex reflection coefficient of the driver, which is a combination of non-reactive components (represented by IV curves) and reactive components (die capacitance and package elements). The driver reflection coefficient is important when there are multiple reflections on a net and in cases where reflected reverse crosstalk is significant. The transmission line and receiver load tests the complex reflection coefficient of the receiver as well as the transient response of the clamp devices. Finally, the standard load represents the conditions the manufacturer deems to be most common. This load is less critical than the other four, but it is important in defining the timing parameters of the component.

The test load measurements cover the IBIS Package and Ramp keywords, as well as their underlying subparameters, and the IBIS subparameters C_comp, C_pin, L_pin, and R_pin.

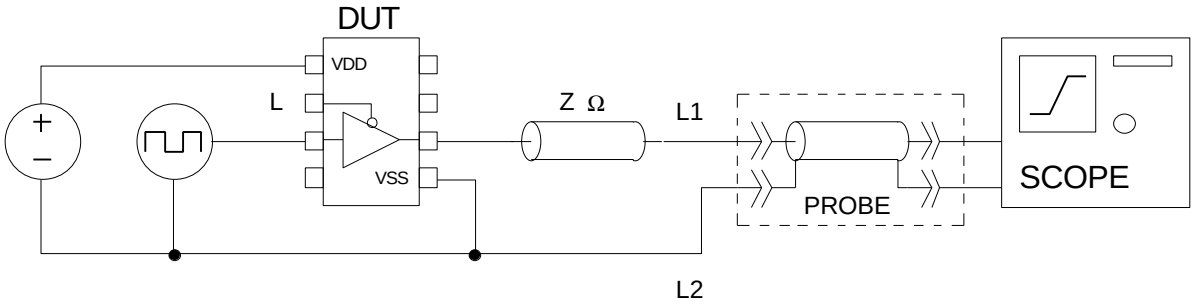
3.4.1 50 Ω to Ground



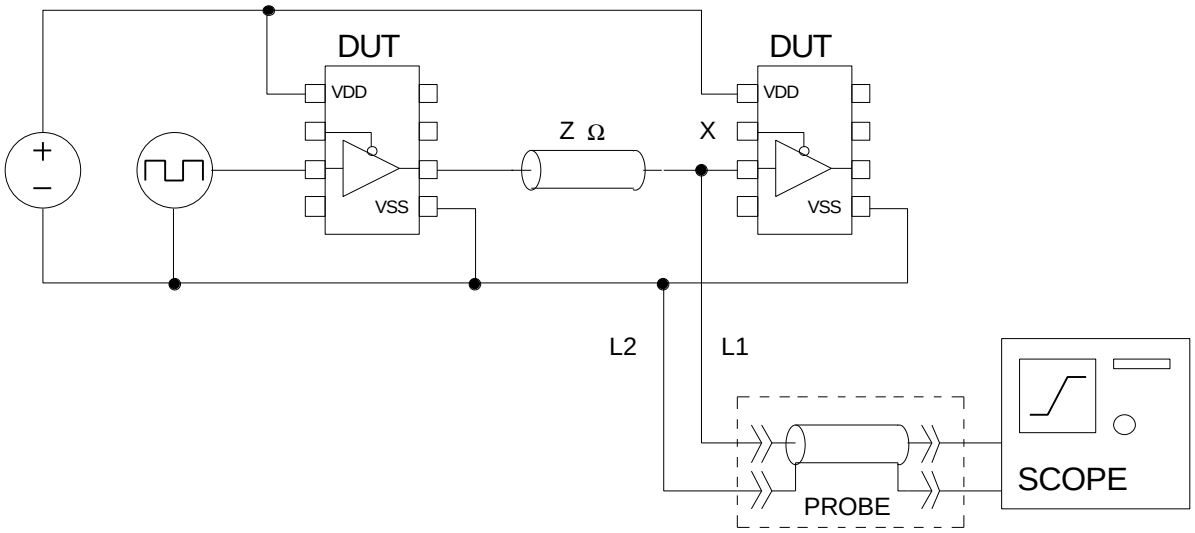
3.4.2 50 W to Vdd



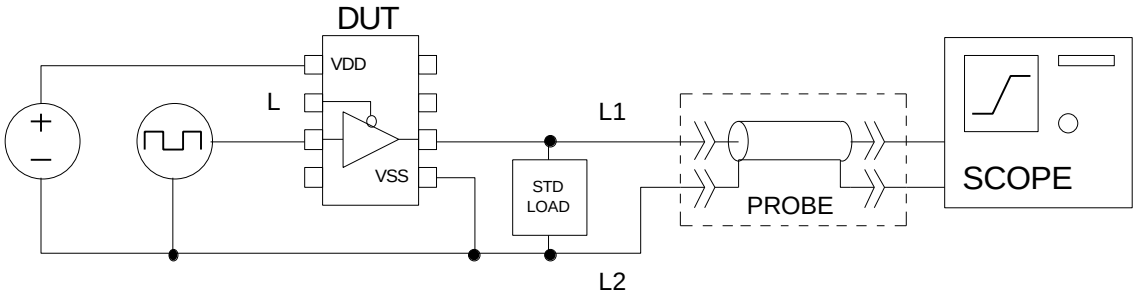
3.4.3 Open-Ended Transmission Line



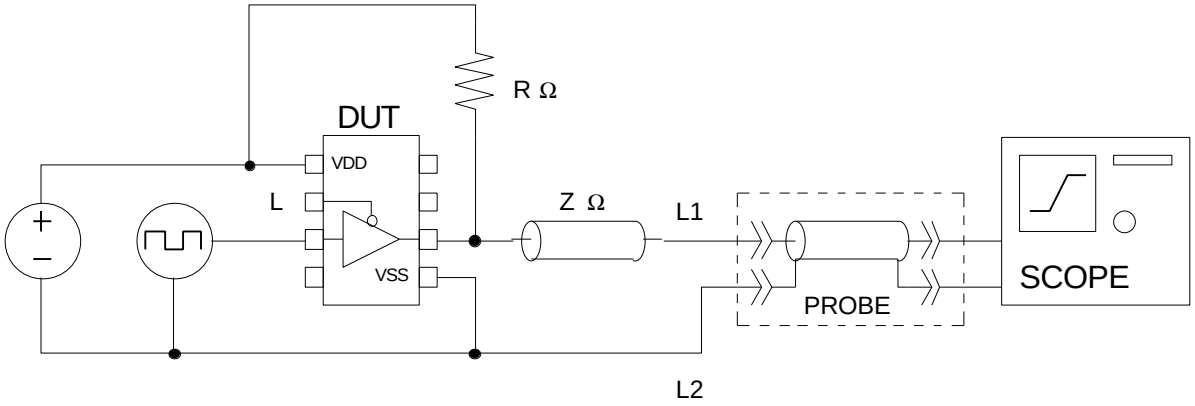
3.4.4 Transmission Line and Receiver



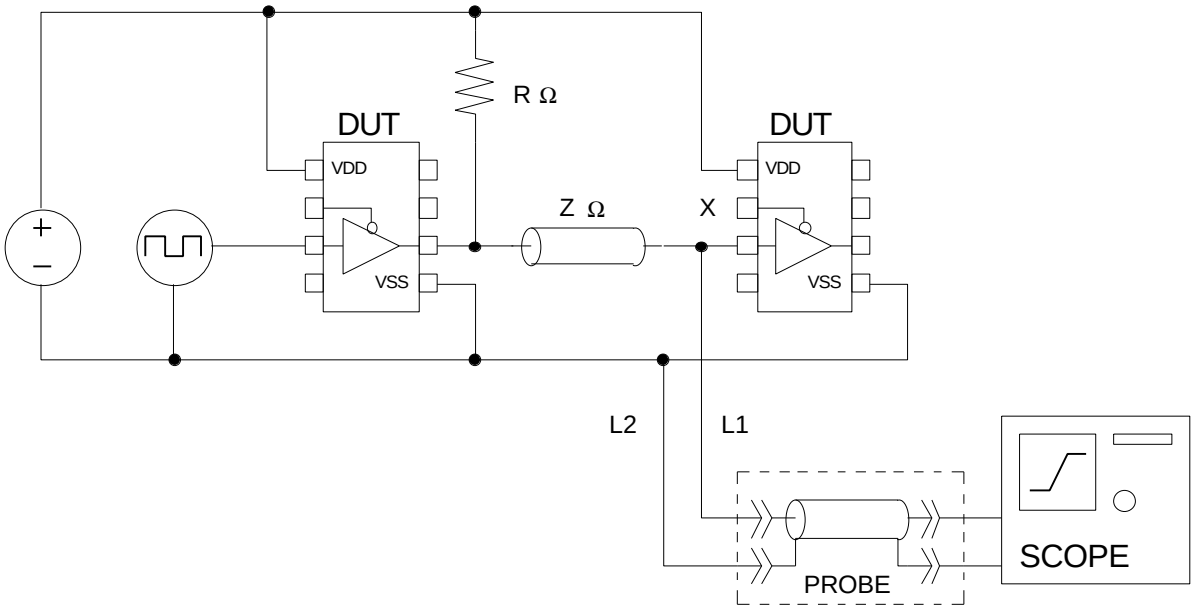
3.4.5 Standard Load



3.4.6 Open-Drain Open-Ended Transmission Line



3.4.7 Open-Drain Transmission Line and Receiver



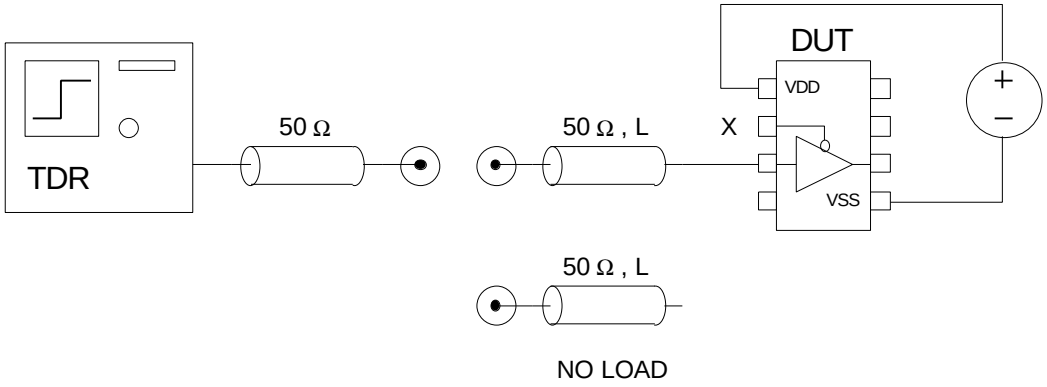
3.5 Capacitance

Capacitance is the third fundamental piece of information in a behavioral model and probably the most difficult to measure. This section includes two different measurement techniques: one in the time domain

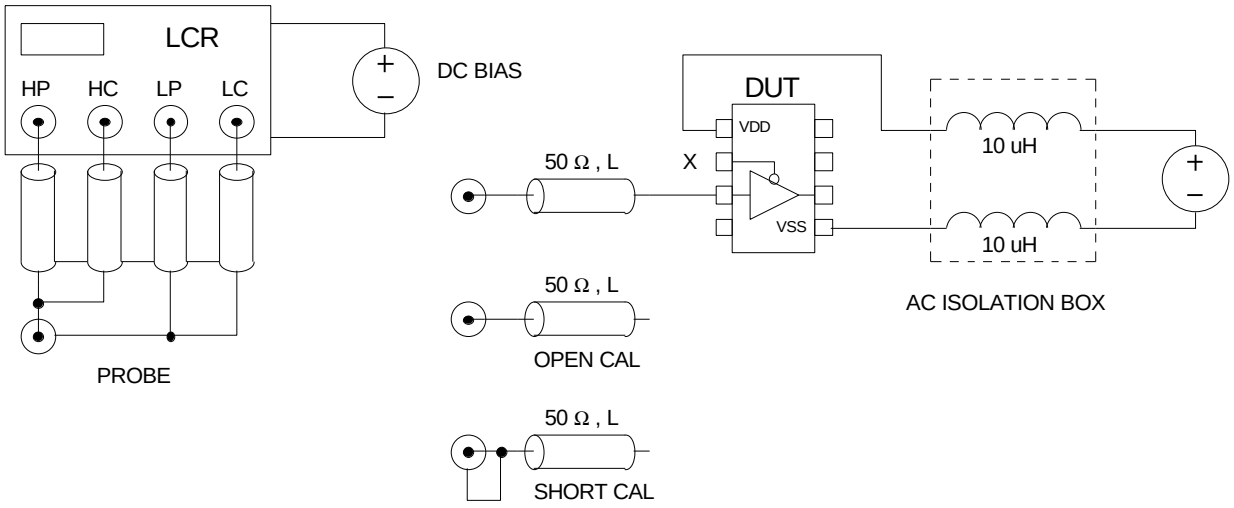
and one in the frequency domain. There are certainly other valid techniques; the important thing is to document the measurements. The time domain method is the simpler of the two and requires a time-domain reflectometer (TDR). The frequency domain method may be useful to labs that already have an auto-balancing bridge, the instrument labeled "LCR" in the figure below.

The capacitance measurements cover the IBIS subparameters C_comp, C_pin, and C_pkg.

3.5.1 Time-Domain Reflectometer Capacitance Measurement



3.5.2 Auto-Balancing Bridge Capacitance Measurement



4. Correlation

Correlation is the process of making a quantitative comparison between behavioral simulation results and lab data. Section 4 defines the correlation process for IV curves and transient waveforms. It also describes how to compare data from capacitance and edge rate measurements.

The IBIS Accuracy Specification employs a two-step approach to correlation. In the first step, the semiconductor vendor correlates lab data against SPICE-based golden waveforms that are embedded in the IBIS datasheet in the form of voltage-time tables. In the second step, the user correlates behavioral simulation results against the same golden waveforms using his or her simulator of choice. This approach effectively decouples the behavioral simulator from the hardware and splits the correlation problem into independent components.

4.1 Correlation Levels

IBIS users have accuracy needs that vary with the demands imposed by their designs. For this reason, the IBIS Accuracy Specification defines several "correlation levels," allowing the IBIS user and the modeling engineer to decide how much effort is required in comparing simulations with data from test hardware for a given application. A correlation level is a means for categorizing IBIS datasheets by the amount of effort the datasheet originator invests in verifying their accuracy. Each individual correlation level is defined on the basis of how much the modeling engineer knows about the semiconductor processing conditions of the sample component(s). For the purposes of this specification, a metric is simply a numerical method for quantifying how well two sets of data points agree with each other.

Table 3: Correlation Levels

Level	Component Sample	Envelope Metric	Overlay Metric
1	Random	YES	NO
2	Known typical	YES	YES
3	Known typical, fast, slow	YES	YES

4.1.1 Correlation Level 1

Correlation Level 1 applies in the case that the modeling engineer knows nothing about the processing conditions of the DUT. In other words, the DUT is a random sample. The Curve Overlay Metric only applies in cases where the two curves should theoretically lie on top of one another. Therefore, the Curve Envelope Metric is the only valid metric in this case. The Envelope Metric is not useful in all waveforms or IV curves (see section 4.4). Correlation Level 1 provides the least accuracy information. It is relevant to correlation of golden waveforms to lab measurements only.

4.1.2 Correlation Level 2

Correlation Level 2 applies in the case that the modeling engineer has a sample component that is known to come from a lot with typical semiconductor device parameters. The Envelope Metric applies in all Correlation Levels, but the Overlay Metric provides more accuracy information. Correlation Level 2 is relevant to correlation of golden waveforms to lab measurements and behavioral simulations.

4.1.3 Correlation Level 3

Correlation Level 3 applies in the case that the modeling engineer has three sample components: one from a lot with known typical semiconductor device parameters, one from a fast lot, and one from a slow lot. As in the previous two Correlation Levels, the Envelope Metric applies. Correlation Level 3 insures the highest degree of accuracy as well as confidence that the semiconductor vendor can indeed control the process in a manner consistent with the IBIS datasheet. This allows the IBIS user to have confidence in the timing and noise margins of the system he or she is designing. Correlation Level 3 is relevant to correlation of golden waveforms to lab measurements and behavioral simulations.

4.2 Correlation Considerations

4.2.1 I/O Cell Coverage

It is up to the discretion of the modeling engineer to decide which I/O cell designs warrant correlation. For example, a gate array I/O cell library may contain hundreds of cell designs, many of which are similar to one another. In this case, the modeling engineer may choose a sample that represents a family of I/O cells. It is important that the modeling engineer document which I/O cells he or she correlated in the IBIS Accuracy Trailer.

4.2.2 SPICE Model Requirements

The SPICE model must be a subcircuit that is consistent with the same I/O cell layout that was used to build the sample component, i.e. each semiconductor device (transistor, resistor, diode, etc.) in the layout must be represented in the SPICE subcircuit. The engineer responsible for the SPICE subcircuit must insure consistency with the layout using either a tool that extracts SPICE subcircuits from the layout or a layout vs. Schematic checking tool. The modeling engineer must run the IV curve and test load SPICE simulations using the verified subcircuit and transistor model parameters that represent the silicon at fast, slow, and typical delay process corners.

4.2.3 Voltage and Temperature Conditions

The three correlation levels defined above address the semiconductor processing conditions of the sample component, but they do not address operating voltage and temperature. Voltage is easy to measure; temperature is not. It is possible for the modeling engineer to measure junction temperature by observing the characteristics of a semiconductor device (such as a diode) or by measuring the power the device draws for a known junction-to-ambient thermal resistance (θ_{ja}).

When correlating lab data and simulation results using the Curve Overlay Metric, it is important that the voltage and temperature conditions in simulation match those in the lab as closely as possible. When using the Curve Envelope Metric, it is important that the voltage and temperature conditions are within the boundaries used to create the IBIS datasheet. In either case, the voltage and temperature should be documented in the IBIS Accuracy Trailer.

4.2.4 Process Indicator

One can define an indicator that measures how close the sample component is to a typical curve. While this number does not measure the accuracy of the IBIS datasheet, it does provide a rough indication of the processing conditions of the sample component. Such information may be useful in debugging activities.

$$PROC = \frac{\sum_{i=1}^{N} Y_i(lab) - Y_i(typical)}{\Delta Y \cdot N}$$

A positive value for this number indicates that the sample component is toward the strong end of the semiconductor process variable space. A negative value indicates that the sample component is toward the weak end of the process variable space.

4.3 Curve Overlay Metric

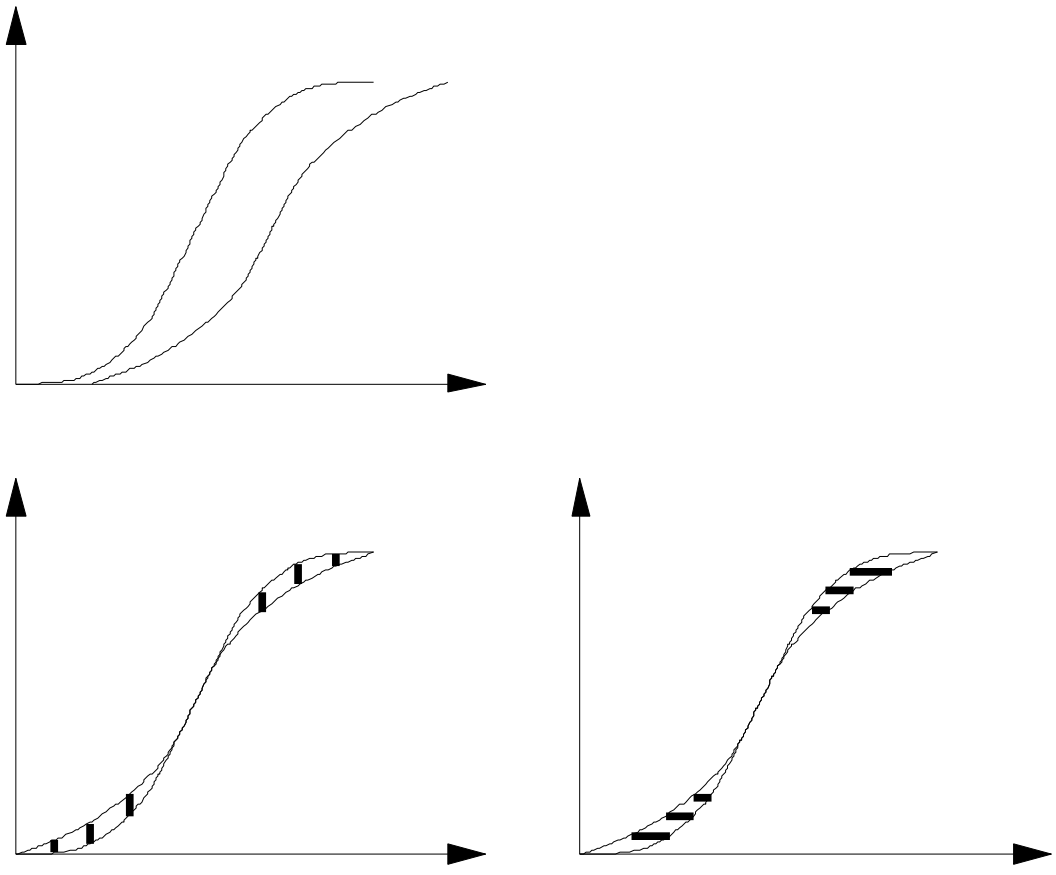
The Curve Overlay Metric applies to cases in which the measured and simulated data should theoretically lie directly on top of each other. For example, a SPICE simulation of a 50 Ω load and a behavioral simulation of the same load should theoretically yield identical results. Another example is the measurement of a known-typical sample component and a SPICE simulation of the same network under identical process-voltage-temperature conditions. The Curve Overlay Metric gauges how well the two

curves or waveforms match each other by summing the absolute value of the x-axis (or y-axis) differences between the two data points, weighing the sum against the range of data points along that axis, and dividing by the number of data points.

$$FOM = 100 \cdot \left[1 - \frac{\sum_{i=1}^{N} \left| X_i(sim) - X_i(lab) \right|}{\Delta X \cdot N} \right]$$

A small C program or script could compute the "Figure of Merit" defined in the above equation. The first numerical task that the algorithm must carry out is to map each set of data points to a common x-y grid by interpolation. The second task is to slide one curve against the other along the x-axis. In the case of the IV curve, this is a trivial step because the two curves are already aligned, but the x-axis origin is an arbitrary point in the case of voltage-time waveforms. Once this is accomplished, the algorithm can then perform the third and final step: comparing the data points and calculating the figure of merit.

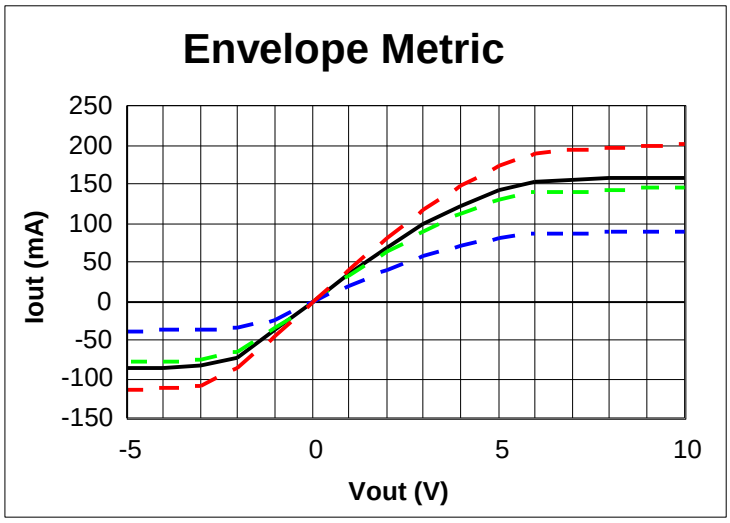
The example below demonstrates two voltage-time waveforms that have identical edge rates but slightly different corners. The first plot shows the original raw data. The second plot shows the same two waveforms after x-axis adjustment. The bold lines are y-axis "error bars," i.e. the difference between the two curves in the y direction. The third plot shows the x-axis error bars.



4.4 Curve Envelope Metric

The Curve Overlay Metric applies to cases in which the measured data are, in theory, bounded by two curves (or waveforms) that represent process-voltage-temperature extremes. In general, this metric is

useful when the processing conditions of the sample component are unknown. The Curve Overlay Metric returns a yes/no value depending on whether or not every one of the data points falls within the envelope boundaries defined by the min and max curves. The plot below demonstrates a lab pull-down curve (solid line) that is slightly stronger than the typical curve (middle dashed line) and lies well within the (outer dashed lines).



The Curve Envelope Metric presents a difficulty in the case of unterminated transmission line loads. Because these waveforms overshoot normal logic levels and ring back, the min and max waveforms intersect each other and do not define an envelope. Therefore, the Curve Envelope Metric may not be applied to the Open-Ended Transmission Line load or the Transmission Line and Receiver load.

4.5 Capacitance

If the C_pin subparameter is present in the IBIS data sheet, the measured capacitance must satisfy the following inequality:

$$[C\_comp(min) + C\_pin] \leq C_{lab} \leq [C\_comp(max) + C\_pin]$$

If the C_pin subparameter is *not* present in the IBIS data sheet, the measured capacitance must satisfy the following inequality:

$$[C\_comp(min) + C\_pkg(min)] \leq C_{lab} \leq [C\_comp(max) + C\_pkg(max)]$$

In other words, the sum of the silicon capacitance (C_comp) and the package capacitance (C_pkg or C_pin) must bound the measured capacitance at their respective minimum and maximum values.

4.6 Edge Rate

IBIS defines edge rate using the Ramp keyword and two subparameters, dV/dt_f and dV/dt_r. These two subparameters each contain two values, a ΔV and a Δt, which are defined by the intersection of the waveform with the 20% and 80% voltage lines when the output buffer is driving a 50 Ω load to ground or Vdd. The measured edge rate should be bounded by the minimum and maximum values of the quotient $\Delta V/\Delta t$ from the IBIS data sheet.

5. Documentation

The final step in the process is documenting the correlation results in a format that the user can quickly digest to decide whether or not an IBIS datasheet is appropriate for a given application. The format for documentation is the IBIS Accuracy Trailer, a comment section appended to the end of an IBIS datasheet. The IBIS Accuracy Trailer contains a disclaimer, information regarding the test environment, and the correlation results in the form of a figure of merit table.

5.1 Disclaimer

The wording of the disclaimer is not fixed; an IBIS datasheet originator may amend it as they see fit. The strength of the suggested wording lies somewhere between that of a component datasheet and "use at your own risk." The IBIS user community realizes that uncorrelated modeling data can severely affect the profitability of the companies whose product reliability depends on that data. The suggested disclaimer is an attempt to find a common ground between the two extremes.

5.2 Test Environment

The test environment section of the IBIS Accuracy Trailer contains two subsections: measurement conditions and test equipment. The measurement conditions subsection records the values of the parameters that are most critical to limiting uncertainty in the correlation process. Some of the parameters represent measured values, such as transmission line impedance and propagation delay. Measured values should be indicated with an asterisk. Other values, such as probe bandwidth, may come from a specification sheet. The test equipment subsection gives the user confidence that the correlation measurements were made in a lab with equipment that is appropriate for the measurements. Using the information in the test environment section, anyone should be able to obtain a sample component and repeat the correlation measurements.

5.3 Figure of Merit Table

The IBIS Accuracy trailer contains one figure of merit table for each model in the IBIS datasheet that was correlated against a sample component(s). The beginning of a FOM table can be identified by the string [Model] followed by the name of the model. The first information that appears is the pin number and signal name of the pin that the modeling engineer used to take the data. This information is important for repeatability.

There are two distinct sections within the FOM table. The first section contains the actual FOM values that are returned by the applicable metric. The measurement column refers to the section of the IBIS Accuracy Specification that defines the measurement; a brief description follows. The population of the next three columns depends on the correlation level. The column labeled "overlay" contains the value returned by the Curve Overlay Metric, in units of percent. The column labeled "envelope" corresponds to the Curve Envelope Metric. It has a yes or no value depending on whether or not the lab data fell within the min/max envelope. The column labeled "process" gauges the fit to the typical curve, in units of percent. A positive value indicates strong silicon; a negative value indicates weak silicon.

The second section within the FOM table contains the values of capacitance and edge rate measurements compared to the corresponding values from the IBIS datasheet. The capacitance values in the "IBIS min" and "IBIS max" columns are the sum of C_comp and C_pin (or C_comp and C_pkg, whichever is appropriate). The edge rate values in the "IBIS min" and "IBIS max" columns are the quotient of the two number separated by a "/" in the IBIS [Ramp] keyword.

Glossary

Accuracy: Agreement between behavioral simulation results and lab measurements.

Behavioral Model: The set of equations that govern the circuit solution for a given I/O buffer. Behavioral models are not necessarily as common among behavioral simulators as the BSIM or Gummel-Poon transistor models are common among SPICE simulators.

Correlation: The process of making a quantitative comparison between behavioral simulation results and lab data.

Correlation Level: A means for categorizing IBIS datasheets based on how much the modeling engineer knows about the processing conditions of a sample component and which correlation metric he or she used.

Correlation Metric: A means for quantifying accuracy. The Curve Overlay Metric associates a figure of merit with a given set of lab and simulation data. The Curve Envelope Metric indicates whether or not the lab data fell within the envelope defined by the simulation data.

DUT: Device-under-test.

Figure of Merit: A percentage that indicates the "goodness of fit" between lab data and simulation results. A figure of merit of 100% indicates ideal correlation.

Golden Waveform: A voltage-time table in the IBIS datasheet that stores SPICE simulation results for a specified load using the IBIS [Rising Waveform] and [Falling Waveform] syntax. Golden Waveforms are not to be confused with the voltage-time tables used by simulators to adjust their internal stimulus. These waveforms require a non-reactive load.

IBIS: I/O Buffer Information Specification. A template for communicating information about the electrical characteristics of an I/O buffer.

IBIS Accuracy Specification: A specification that defines a quantitative method for correlating test hardware with behavioral simulation predictions and documenting the results of the correlation.

IBIS Accuracy Trailer: A comment section appended to the end of an IBIS datasheet that contains the correlation results (figure of merit table) and some information regarding the test environment.

IBIS Datasheet: The ASCII text file that conforms to the I/O Buffer Information Specification and contains the input data for a behavioral simulation. In common conversation, the terms "IBIS datasheet" and "IBIS model" are often used interchangeably, which can lead to confusion about exactly what information an IBIS datasheet contains. See "Behavioral Model."

IBIS Datasheet Originator: The company that is responsible for creating an IBIS datasheet for a component. The semiconductor vendor has all the information necessary to create an IBIS datasheet at its disposal and is therefore the natural IBIS datasheet originator.

IBIS Datasheet User: The engineer responsible for appropriate application of and IBIS datasheet to a network analysis problem. The IBIS datasheet user is often a signal integrity engineer at a PC board or system house.

Known Typical Sample: A sample component that process or device engineers have identified as lying in the center of the device parameter distributions. Such identification is usually accomplished by means of parametric measurements on a test site common to every wafer. Known fast or known slow samples are also possible but less common.

Modeling Engineer: An employee of the IBIS datasheet originator who carries out the analysis necessary to generate an IBIS datasheet from source data and check the IBIS datasheet against measurements of sample components. The modeling engineer must have sufficient circuit analysis background to make decisions about how the relevant electrical characteristics of the I/O buffer are communicated to the behavioral simulator through the IBIS datasheet.

Random Sample: A sample component of unknown process origin.

Sample Component: The DUT that the modeling engineer uses to make lab measurements for correlation with simulation results.