Cook Acrobat 0.7 Brief Comments - Bob Ross 2/10/05

1. Page 5 capitalization consistency in definitions

2. Several references are made implying that Clamp tables are required for certain model types. It is not clear whether they need to be extracted or whether the keyword [GND Clamp] and [Power Clamp] are actually required.

The Clamp keywords are always optional because the data may be zero for that model architecture.

3.
3.1.1.3, 3.1.1.4 The clamp tables may be needed for extractions, but are NOT required in IBIS - if they contain no added data.

For Output only, some model producers extrapolate the I-V data to separate out data expected to be caused by a separate clamp path, as seen by the sudden slope change.

4. 3.1.1.4 There is no exception to the Sweep ranges in IBIS for Open-Drain.

CLAMP tables are NOT required.

5. 3.1.1.5 Clamp tables are not required.

6. 3.2.1 Ramp rate - use voltage consistent with spec - recommend use Vcc because the tool will assume Vcc. Spec is ambiguous. A cookbook recommendation is helpful (set [Voltage Range] equal to actual voltage used for pullup resistor.)

For ECL, use Vcc-2V - this is defined in the Spec. (also applies to PECL)

7. pg. 10 "CAE" to "EDA" vendors - global change in several places.

8. Table 1 - delete TTL 500 ohms and 7 ohm case. This is only a Quad recommendation - for debatable reasons. 8 waveforms is way too many for most tools.

Also, not sure about note (2), if greater than 100 ohms. The intent is to use a resistor to match the TL impedance for most accurate dynamic response. Recommend using load a low resistance load for extraction if the buffer switches fast.

Some very weak buffers are not strong enough to drive 50 ohms. That is the exception, but they will not be factors in high speed design because they will stair-step up to the final voltage anyway.

Also, some tools can process 2R and 2F waveforms for ECL. 1R and 1F are sufficient because ECL operates in an active region where the V-T shape remains fairly constant.

9. 3.3.2 last paragraph regarding extra "validation" waveforms - some tools ignore, but some include. The 50 pF to Gnd may be included and severely distort the algorithms. So be careful with this recommendation!!

10. 3.2.4 multi-stage , now pre-emphasis incomplete

11. 3.2.5.2 CMOSFET vs CMOS technology. terminology consistency

True, half and pseudo differential Interesting, but is half treated as true?

Need to stress that everything is modeled as pseudo-differential
Ver. 4.1 needed for true and half. (defined as true in the spec.)

12. 3.2.5.4 Also T-structure (use pi equivalent) and unsymmetrical??)
IBIS Supports general pi structure in 4.1.

13 3.2.5.9 Curves vs. Tables???

Details of additional topics not really needed at this time -
could mention and refer to Section 7 - uploaded presentations
as a placeholder.

Cautions - simple R is adequate and more widely supported than
[Series MOSFET] which may not be supported the same way, and may
not include non-monotonic capability.

14 4.1.3.2
CMOS, MOSFET CMOSFET terms?? What is the terminology

CMOS buffer used here.

15. 4.1.3.11
First Table is misleading. Clamps are NEVER required.
Disclaimer too weak. Change first table.

Second table ECL waveforms are WRONG, load is always to termination
voltage which is usually the default (for RAMP) of Vcc - 2.

16. Figure 4.16 might have slope extrapolated if known gnd ref resistor.
Then current subtracted from power clamp - as an alternative way
of handing this and more correct if the the internal element is
really a resistor.

17. 4.4.2 V-T table windowing. Tool DEFECT issue. Slow weak may not pass
parser if this is done. We can alert people of the potential
"overclocking" problem and that tools may handle this differently.
However, the model needs to be complete.

18 Section 6 - refer to Accuracy Report and Quality docs.

19. Section 7 - just add a set of links.