I E R S E T
INSTITUT EUROPEEN DE RECHERCHE
SUR LES SYSTEMES ELECTRONIQUES
POUR LES TRANSPORTS

Advances on the ICEM model for Emission of Integrated Circuits

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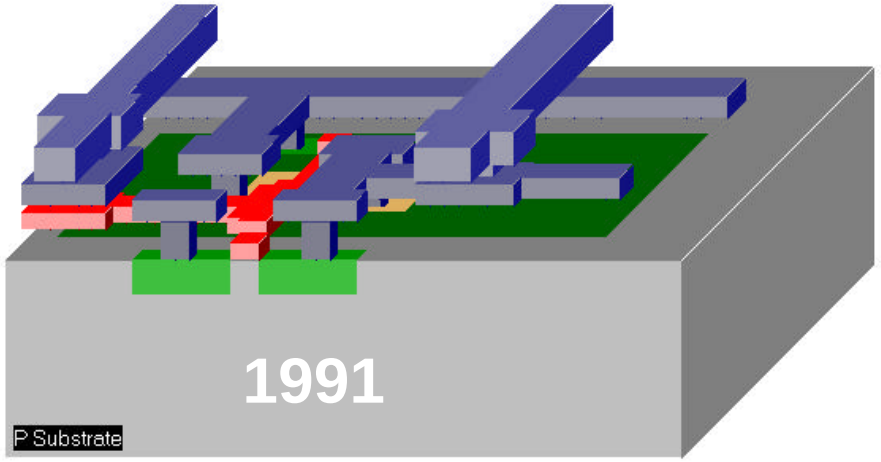
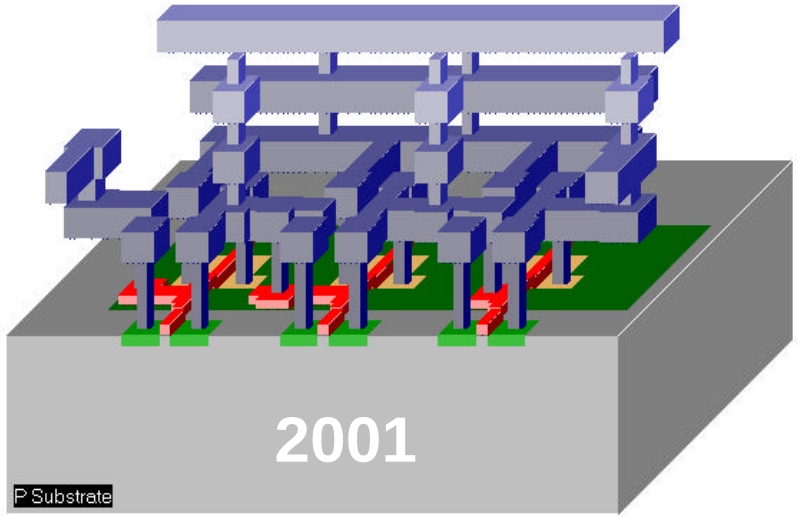
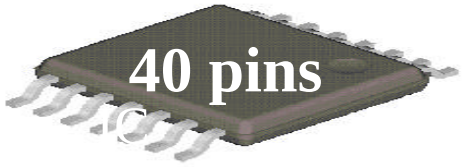
1. Context of the study



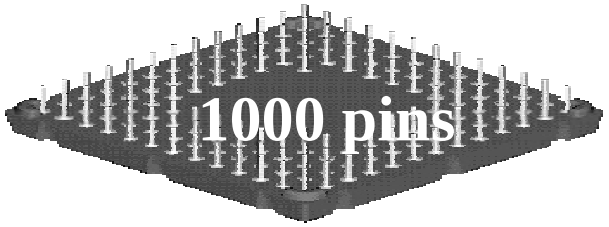


- 0.7µm, 2 metal layers
- Up to 100,000 devices on a chip
- CPU frequency 50MHz

- 0.12µm, 6 metal
- Up to 200,000,000 devices
- CPU frequency 1GHz



10 years of evolution



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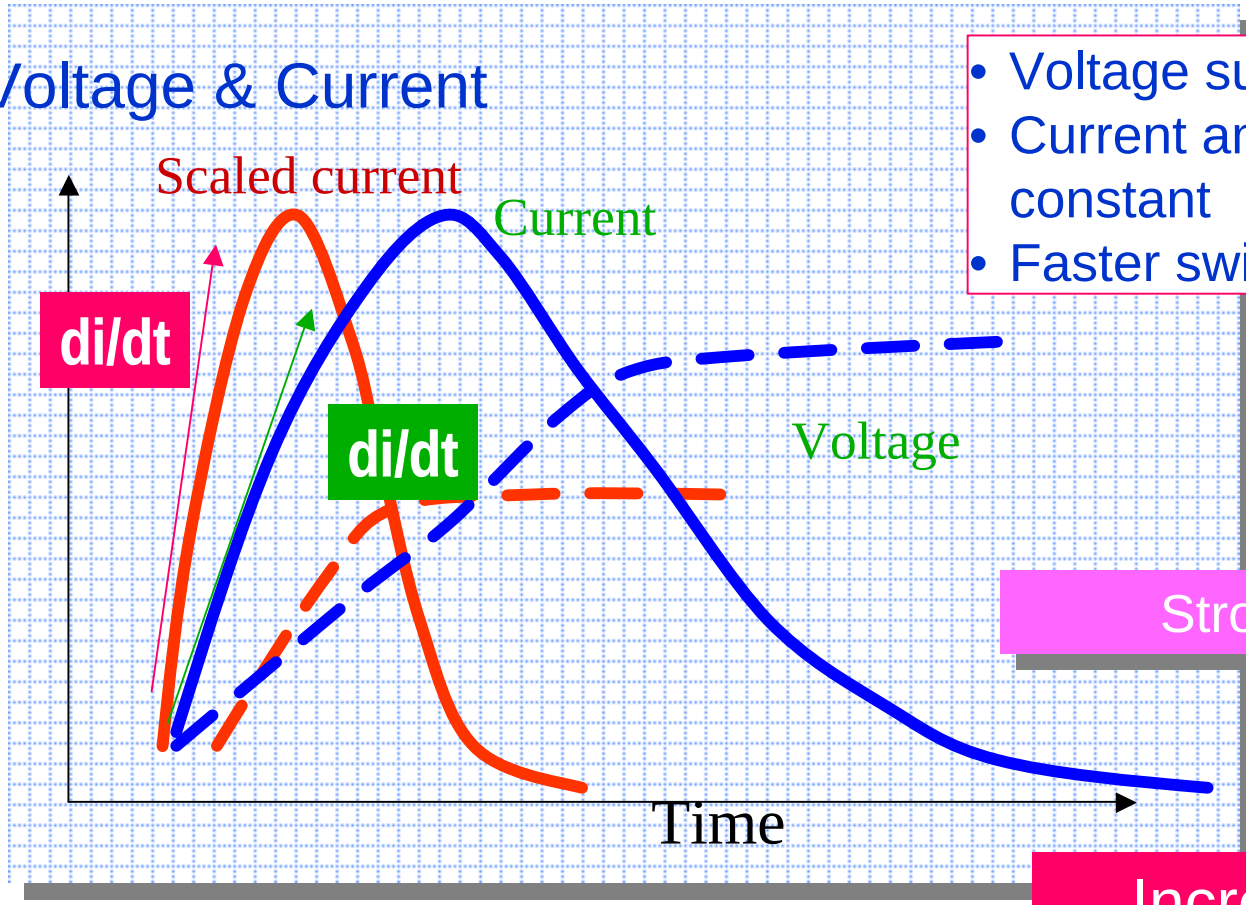


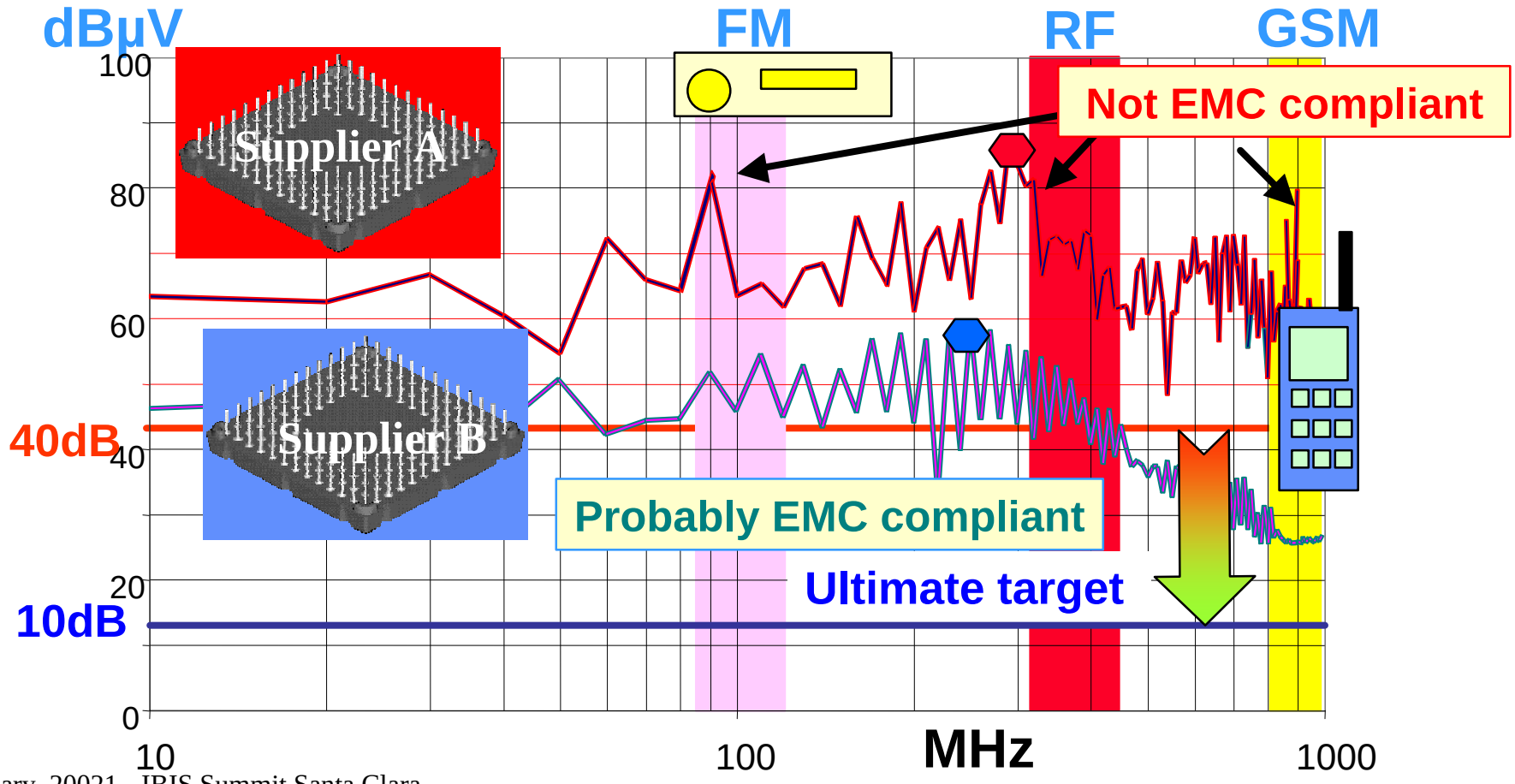
- Voltage supply decreases
- Current amplitude keeps constant
- Faster switching

Stronger di/dt

Increased EMC problems

1. Context of the study

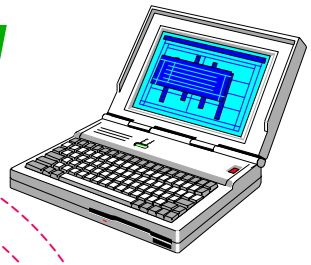
Low parasitic emission is a key argument

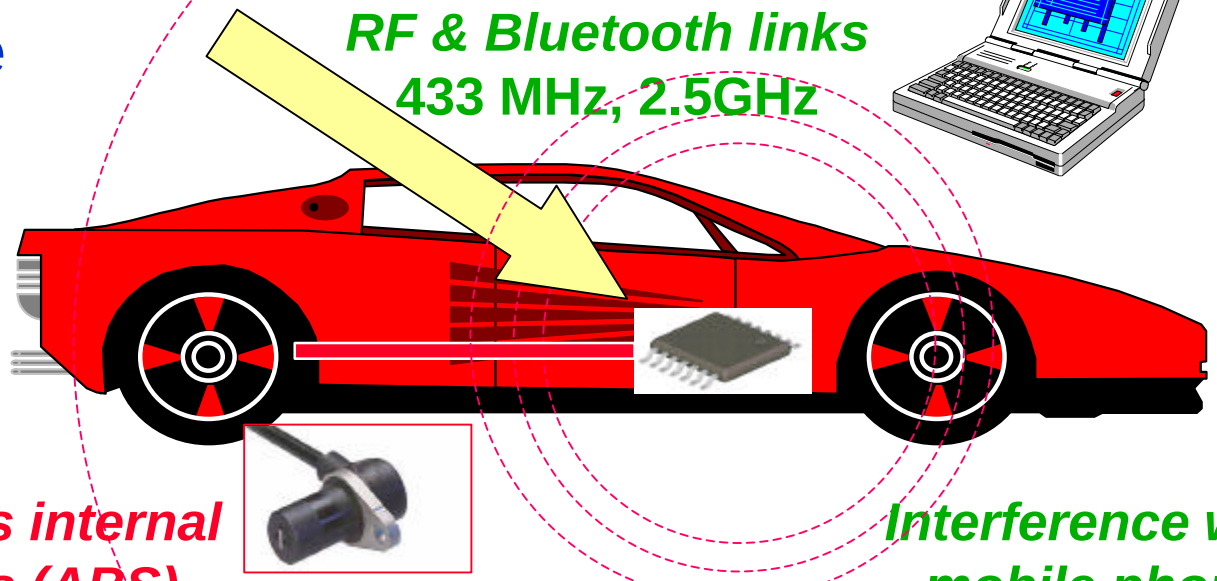


1. Context of the study

Example for automotive

Interference with local RF & Bluetooth links
433 MHz, 2.5GHz





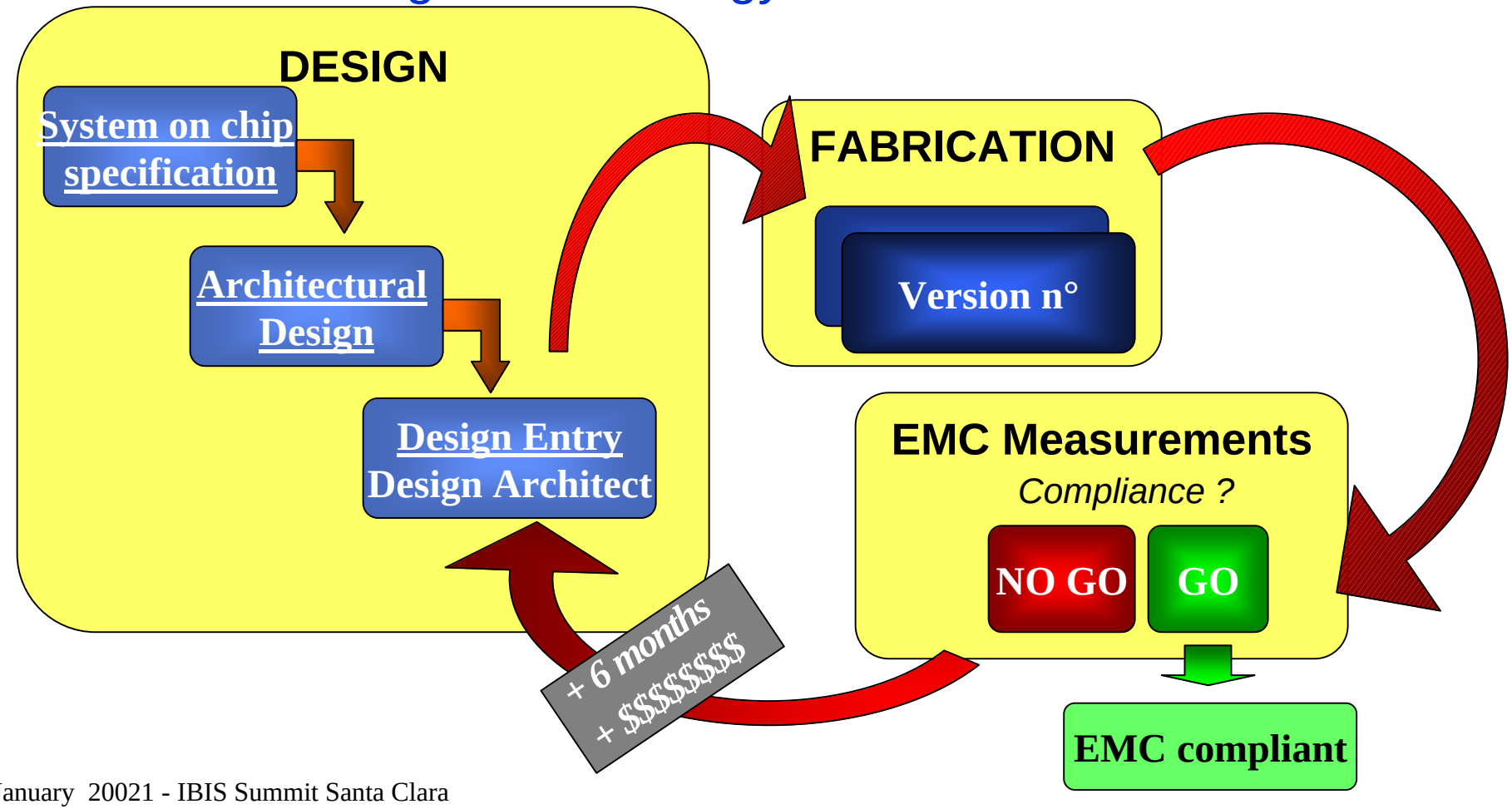
Parasites internal devices (ABS)

Interference with mobile phone
900, 1800,1900MHz

Similar EMC problems in aerospace

2. System Design Methodology for EMC

Obsolete Design Methodology



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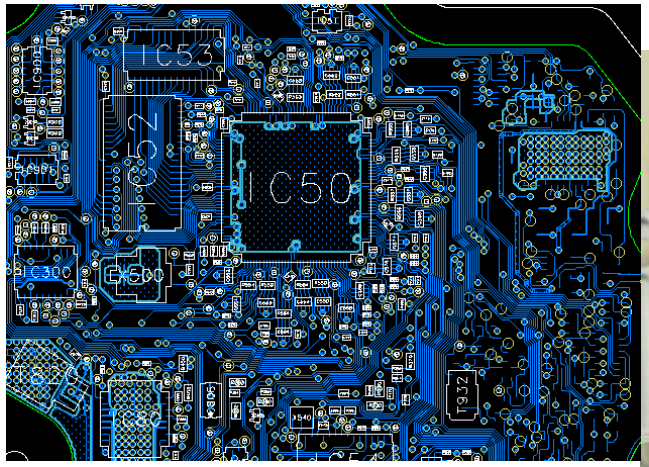
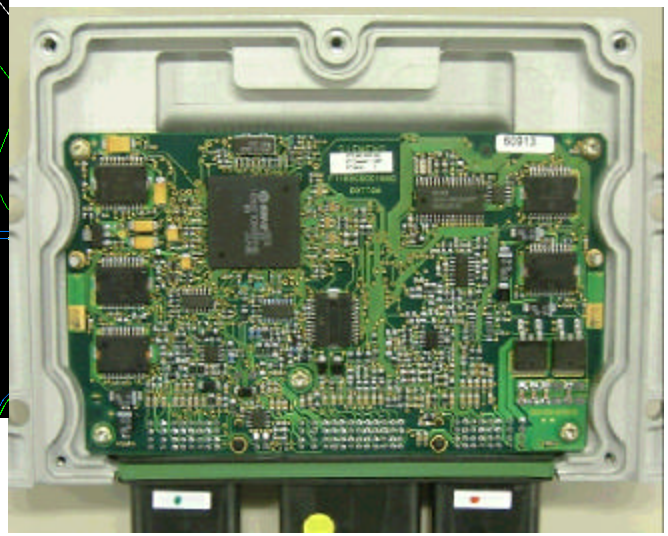
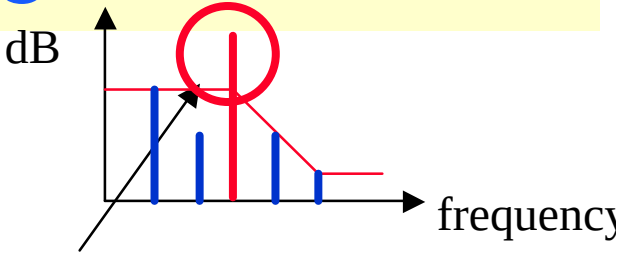
Obsolete Design Methodology

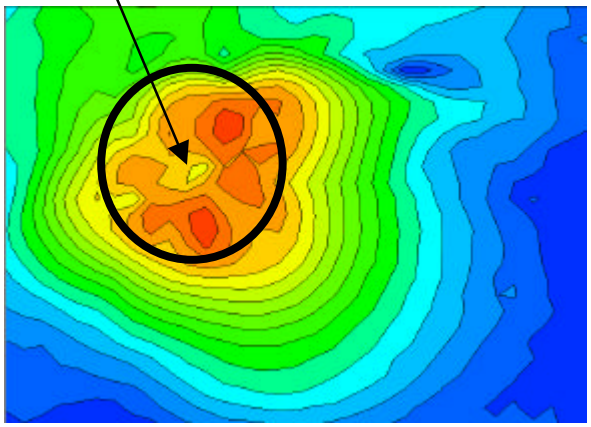


PCB design



Prototype board



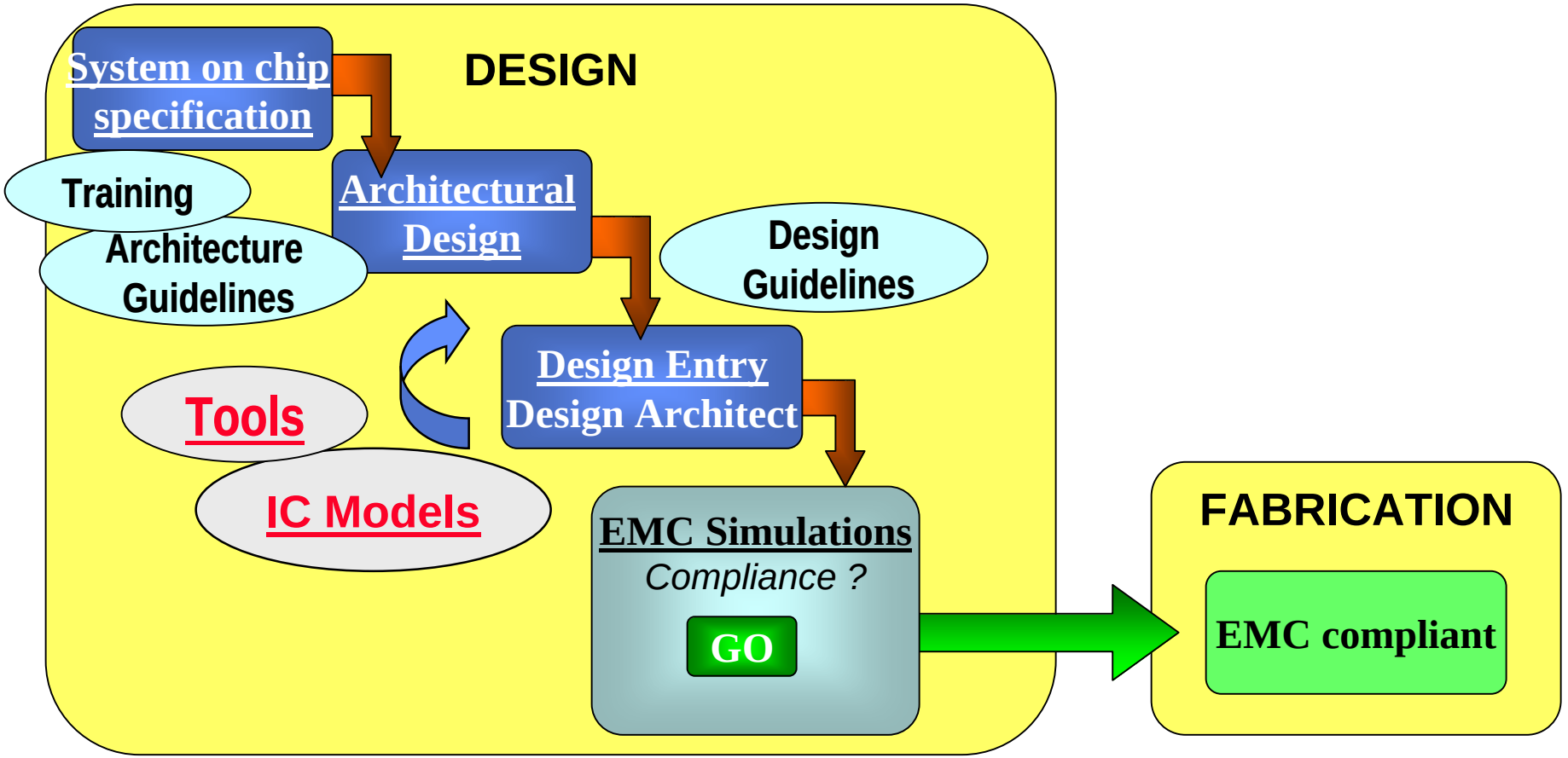


EMC scan

Electromagnetic incompatibility found too late

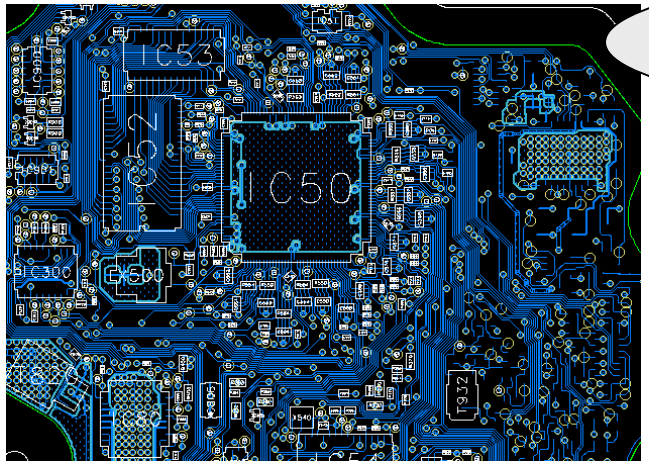
2. System Design Methodology for EMC

Target Design Methodology



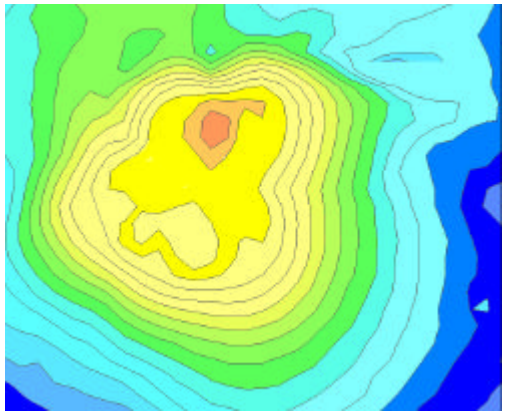
2. System Design Methodology for EMC

Target Design Methodology



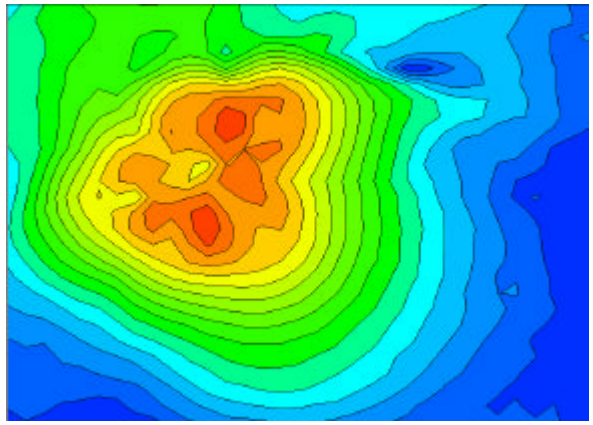
PCB design

With IBIS



Wrong prediction of the radiated emission

With IBIS and core model



Good forecast of radiated emission

A core model is mandatory for accurate emission prediction

3. The IERSET project

European Research Centre on Electronics for Transportation
identifies and co-ordinate co-operative research.

Project EMC for ICs

Objectives

- Definition and validation of a model to be used in PCB CAD tools to guarantee the EMC of electronic systems
- One model from 1MHz to 1GHz, for conducted *and* radiated emission

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3. The IERSET project

ICEM (*Integrated Circuit Electromagnetic Model)*

Technical work at IERSET Toulouse, France

1997-2001

Draft standard UTE France

02/2001

ICEM Cookbook *version 1.c aug. 2001*

08/2001

Commitee Draft for Voting at IEC

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	SOUBEYRAN Amaury	EADS MSI
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	LUBINEAU Marc	IERSET

11/2001

Document on the UTE web www.ute-fr.com

3. The IERSET project

ICEM draft

☞ Now draft technical report 93/146 CDV

IEC

93/146/CDV

DRAFT TECHNICAL REPORT

Project number **62014-3/TR/Ed.1**	
IEC/TC or SC **TC 93**	Secretariat **U.S.A.**
Distributed on **2001-11-30**	Voting terminates on **2002-05-03**
Also of interest to the following committees	Supersedes document

Functions concerned

☐ Safety ☒ EMC ☐ Environment ☐ Quality assurance

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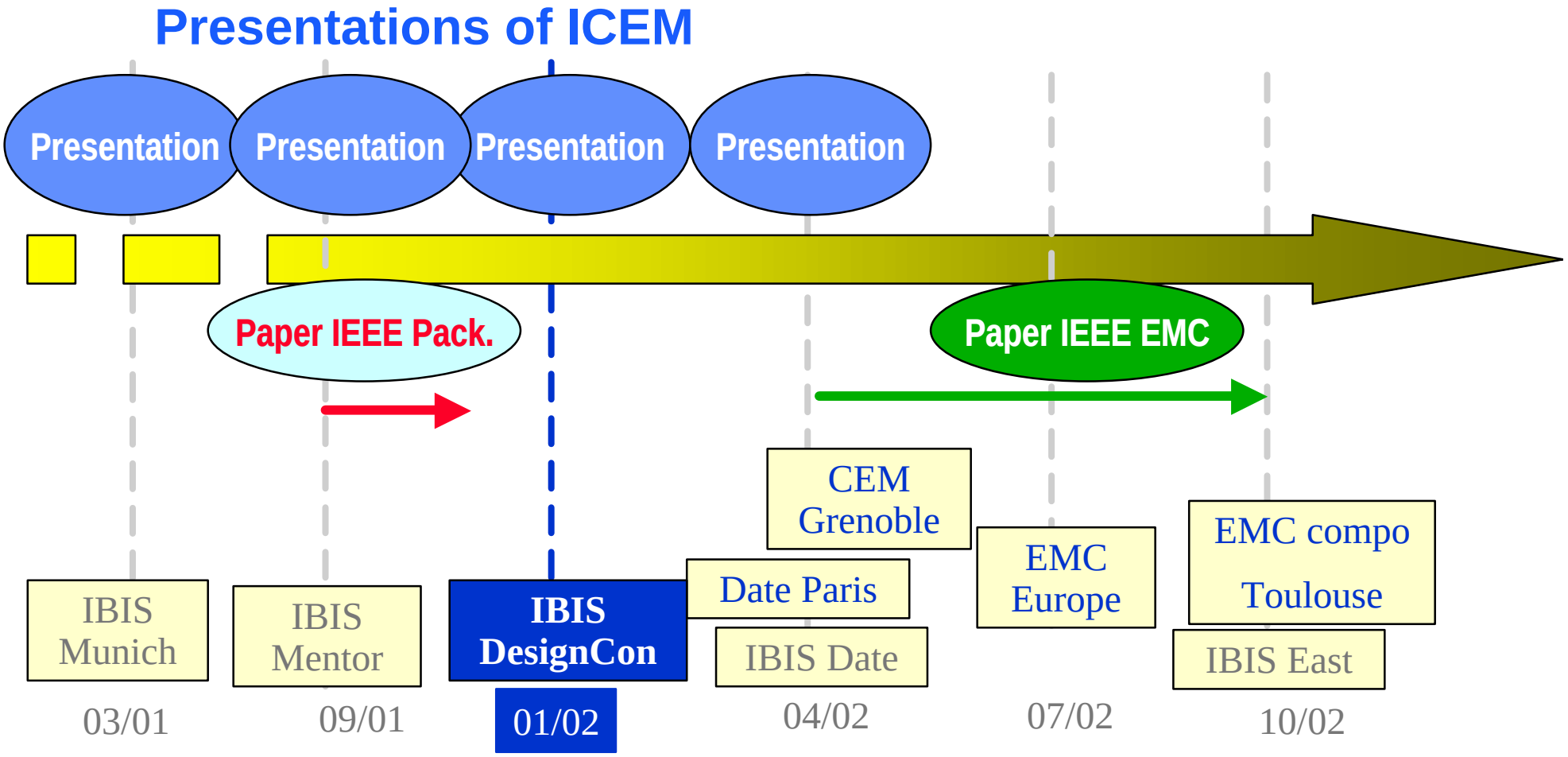
Titre: CEI 62014.3: CEM des composants – Partie 3 : Modèle électrique des circuits intégrés (ICEM)

Title: IEC 62014-3: EMC for Component – Part 3: Integrated circuits Electrical Model (ICEM).

Fou de Bassan © J.C Perrin

3. The IERSET project

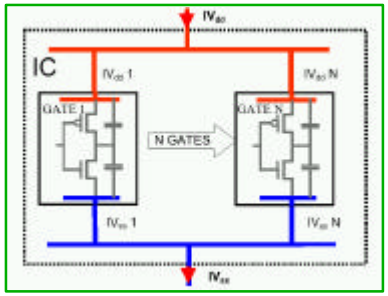


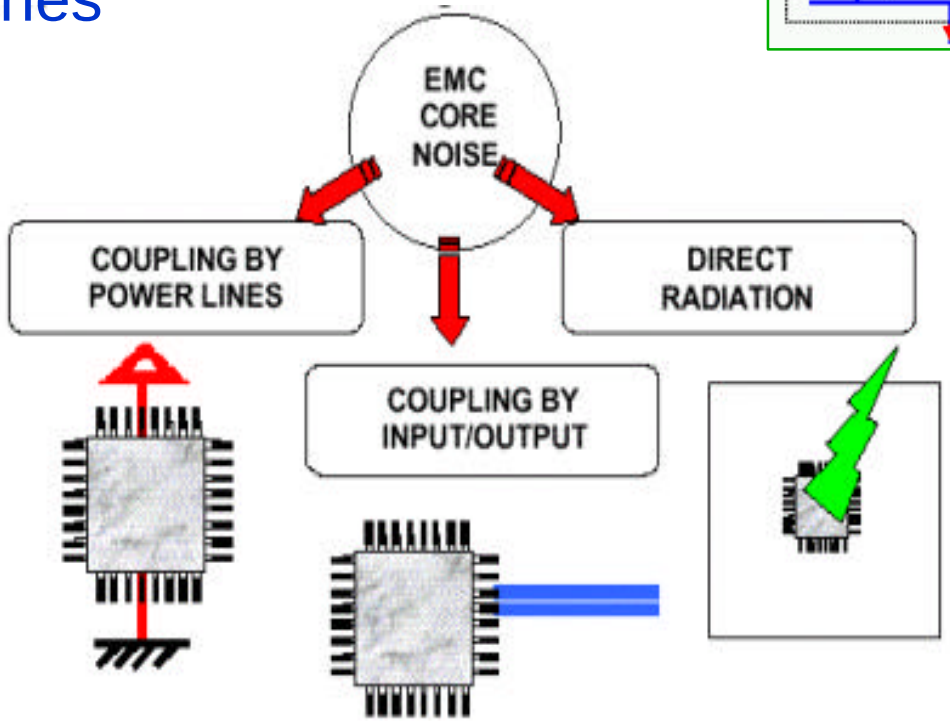
4. Core Emission Model

Core noise of ICs: 3 modes of coupling

- *conducted*: Power lines
  I/Os
- *radiated*: Direct

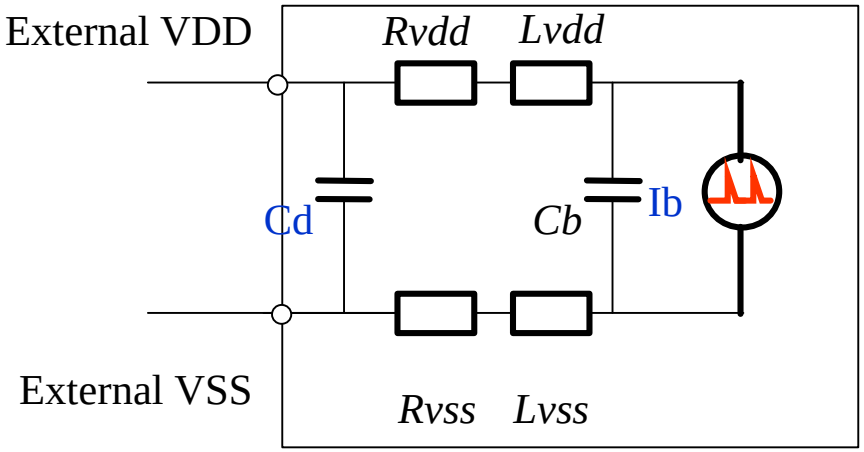
Origin of parasitic emission in CMOS: gate switching



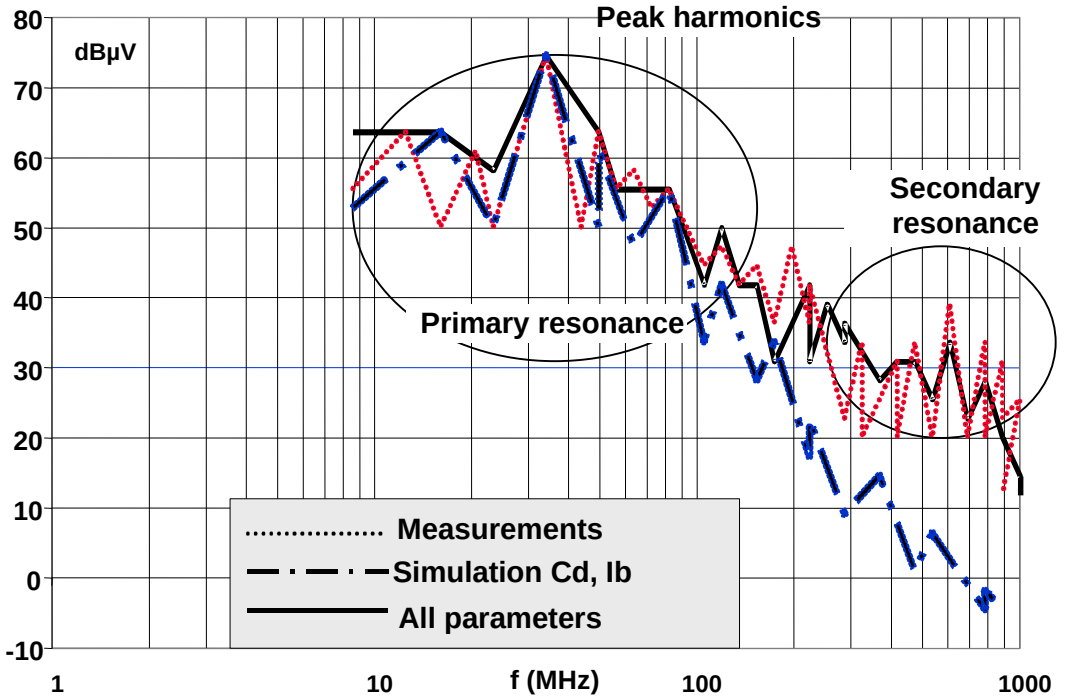


4. Core Emission Model

ICEM includes a simple core model, not handled by IBIS



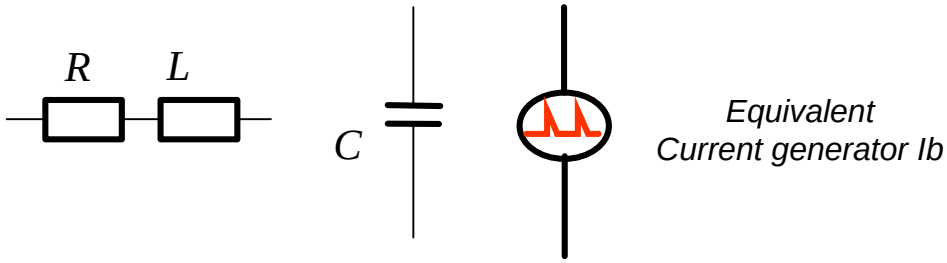
Basic parameters	Cd, Ib
Advanced param.	R,L,Cb



4. Core Emission Model

Parameter determination: several levels

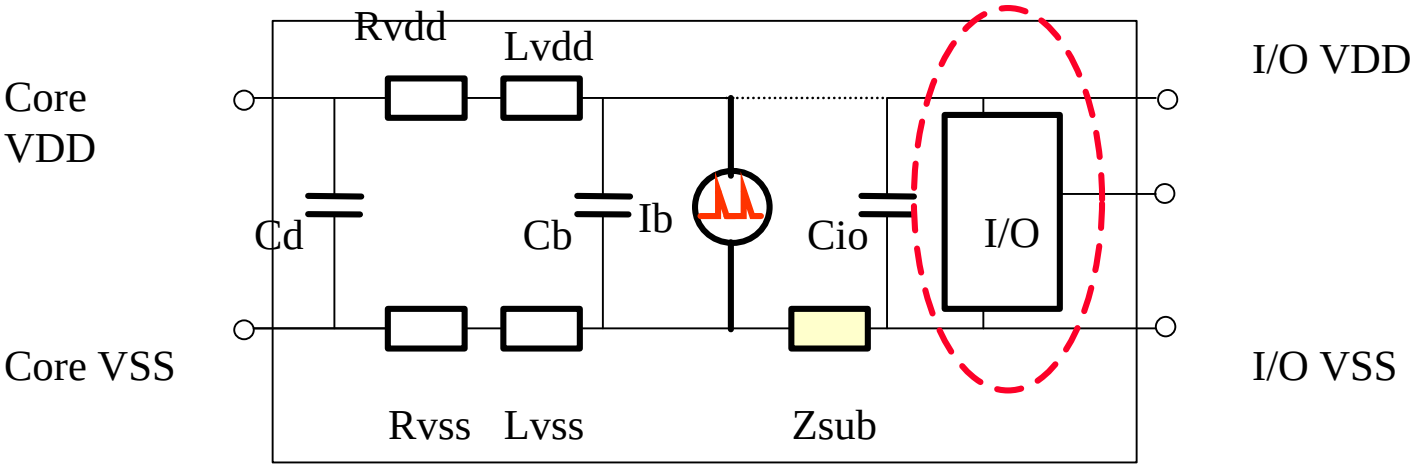
Simulations	Measurements	Estimation
Libraries	*Measurement setup*	*Statistics*
Tools	*After fabrication*	*Standard technologies*
Before fabrication		*Approximation*



Equivalent
Current generator Ib

5. Emission Model with IOs

Add IBIS I/O data



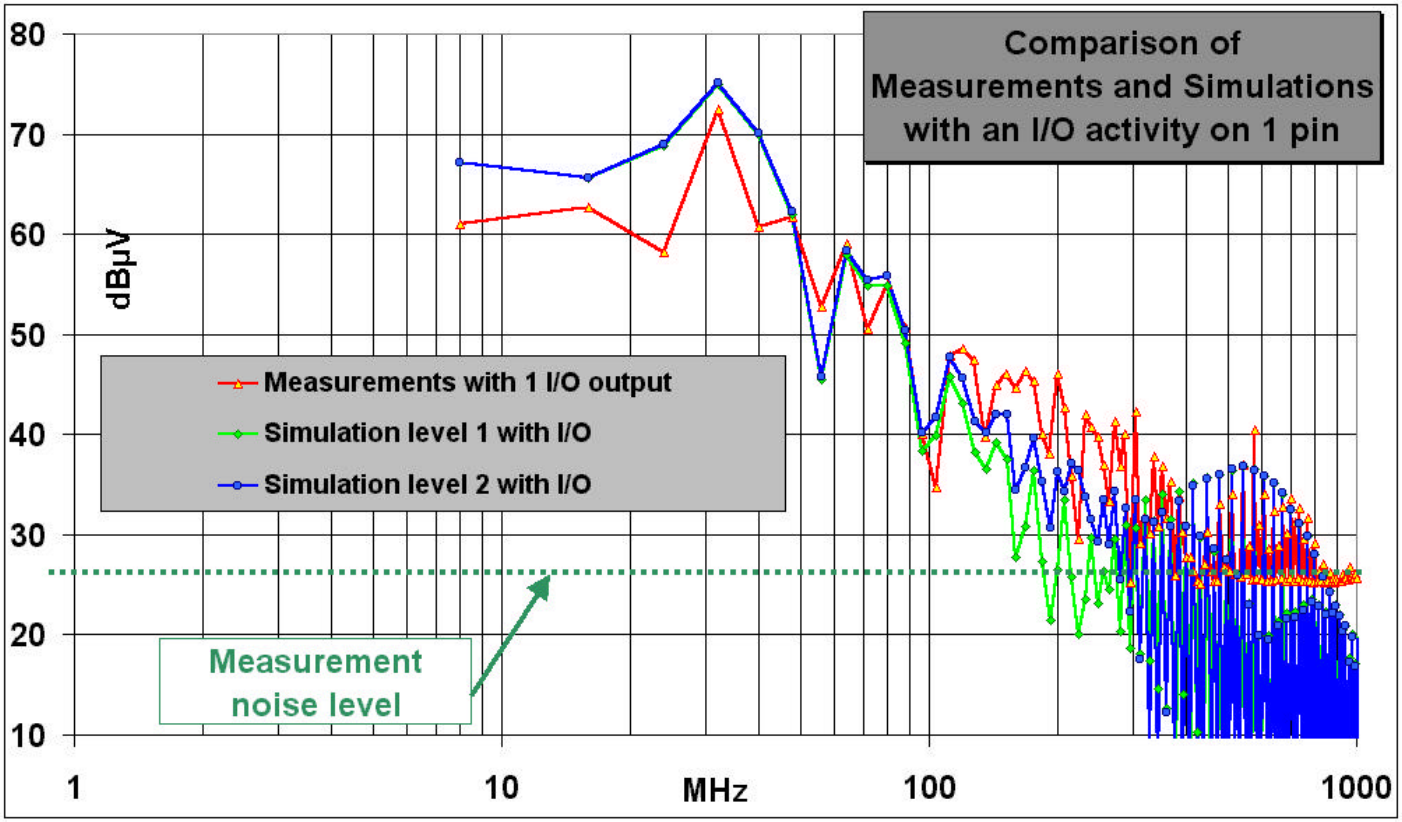
Zsub: basically a 1-10Ω serial resistance

Cio : decoupling capacitance for IO supply

IO block: reuse of IBIS

5. Emission Model with IOs

Validation

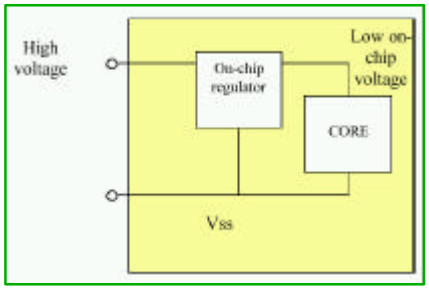


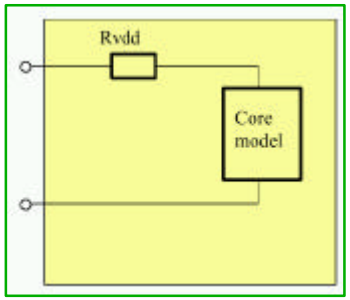
IO modify the spectrum at high frequencies (>300MHz)

6. Adaptation of Emission Model

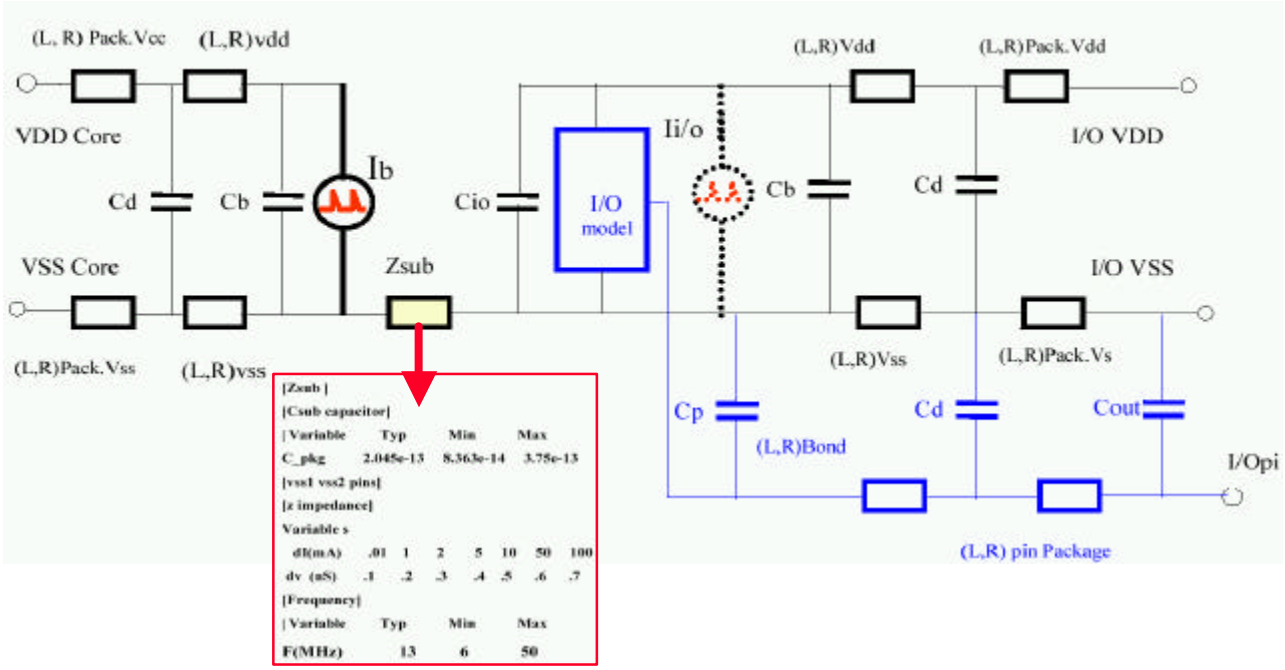
Case of multiple supply structure

Voltage Regulator





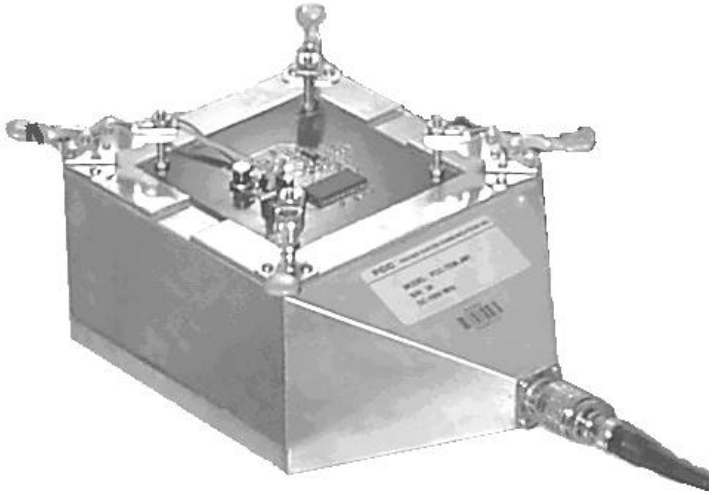
Separate supply for I/Os

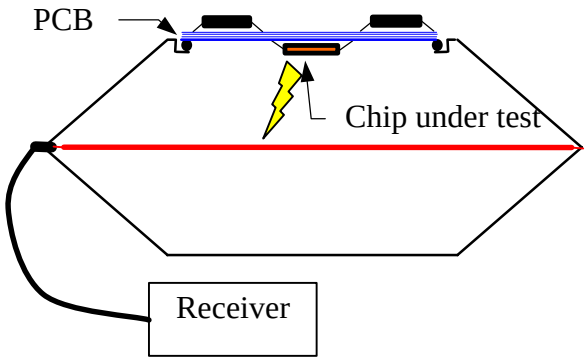


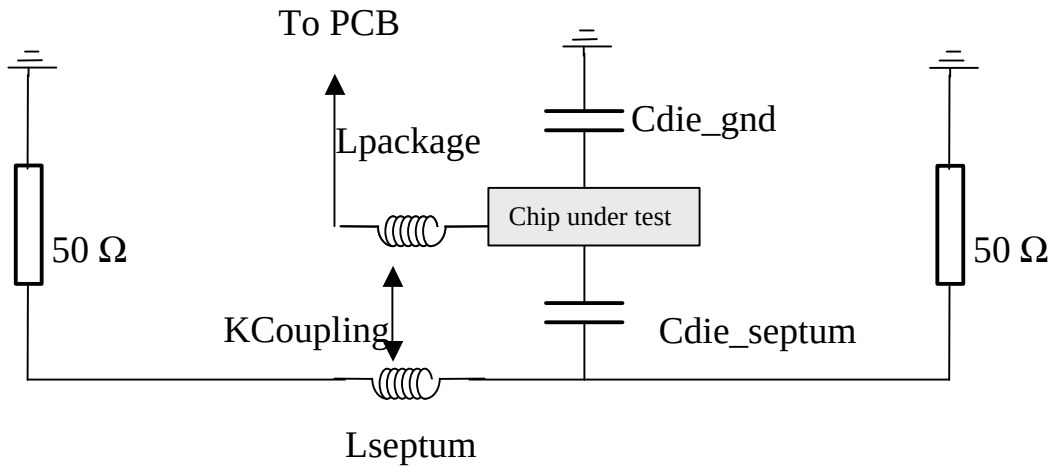
Substrate impedance

7. Emission in TEM cell

Proposed model: capacitance & inductance coupling

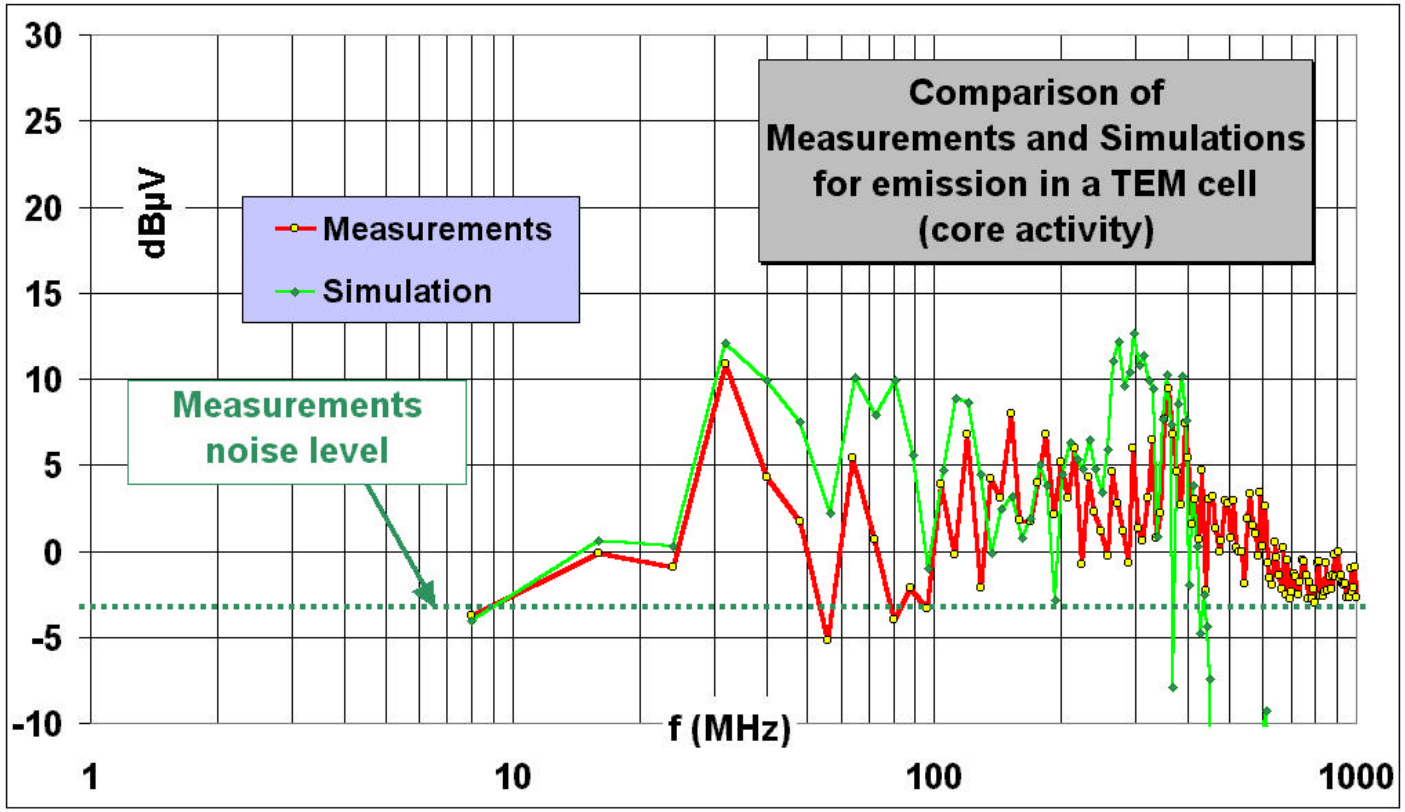






7. Emission in TEM cell

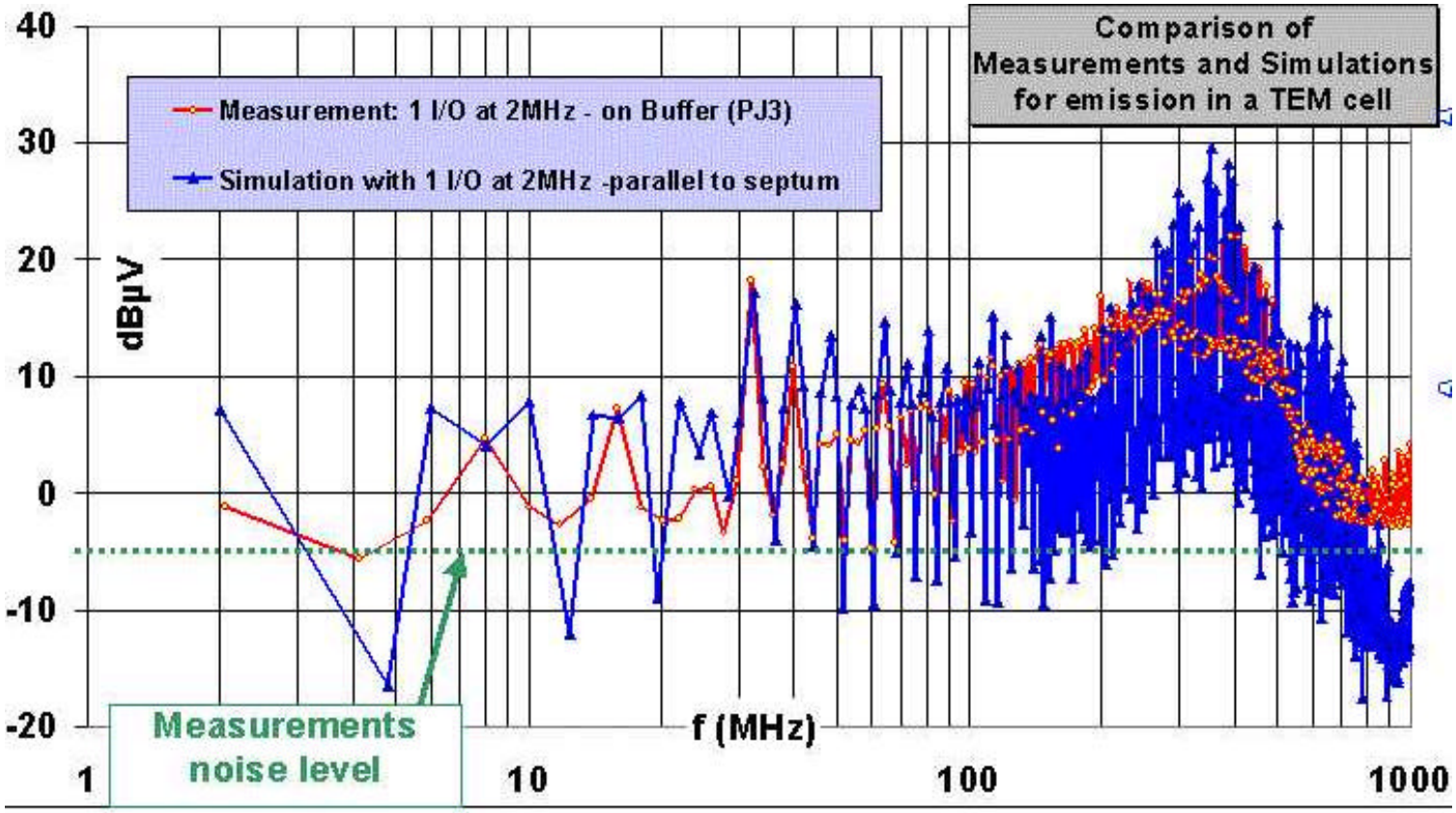
Validation for the core alone



- Model fits correctly up to 400MHz
- At high frequencies, close from noise floor

7. Emission in TEM cell

Validation for the core & IOs



- Model fits correctly up to 800MHz
- At high frequencies, IO effects dominate

8. Implementation of ICEM in IBIS-ML

ICEM in IBIS-ML

- IBIS mark-up language (IBIS-X) makes ICEM implementation very easy
- IBIS-ML draft on the IBIS web site


IBIS-ML Specification 10/31/2001 Rev 0.5

IBIS Macro Language Reference Manual

I/O Buffer Information Specification Macro Language (IBIS-ML)
Language Reference Manual Version 05.

The IBIS Macro Language is a standard language suitable for modeling the analog characteristics of a digital integrated circuit. The IBIS Macro Language is intended for use in conjunction with the ANSI/EIA-656A IBIS standard.

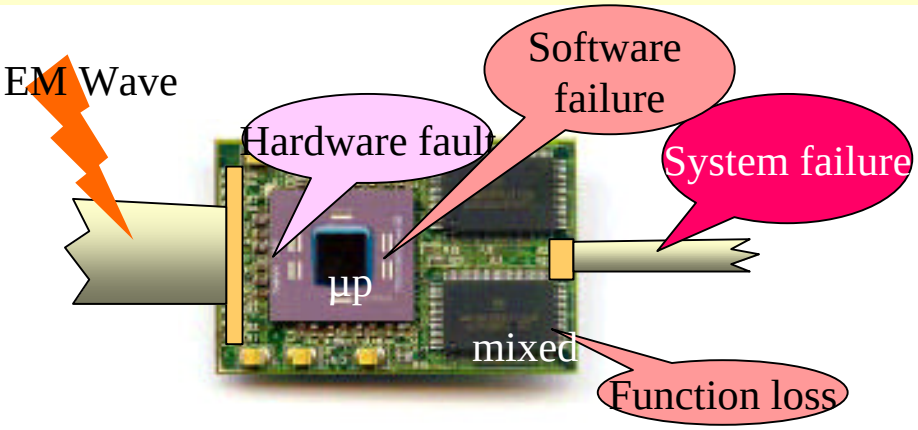
```
[define model] ICEM
| on chip capa
capacitor c_dec (vcc vss) C=5nF
| Serial supply resistor
resistor r_vdd (vcc vcc_int) R=10
resistor r_vss (vss vss_int) R=10
...
| current
Ib (vcc_int vss_int) I=It(TIME)
[It]
time I(typ)
0.0 0.3e-3
0.1e-9 0.3e-3
0.2e-9 0.5e-3
0.3e-9 0.8e-3
…
[end It]
[end define model] ICEM
```

Call of the user-defined model:

```
[begin header]
[ibis-ml version] 0.5
[filename] uC.ibs
[data] Nov 27,2001
...
```

9. Perspectives

- Interest in Susceptibility



- Extend model to higher frequencies (> 1 GHz)

Conclusion

- Technology scale down illustrated
- More complex chips increase parasitic emission
- An EMC model for ICs is mandatory
- A simple model has been proposed
- Satisfactory prediction of conducted emission
- Prediction of the core emission in TEM investigated
- Model proposal standardized by UTE (ICEM)
- Presentation and promotion to CAD & IC providers