# Split C-comp for Quiet Line

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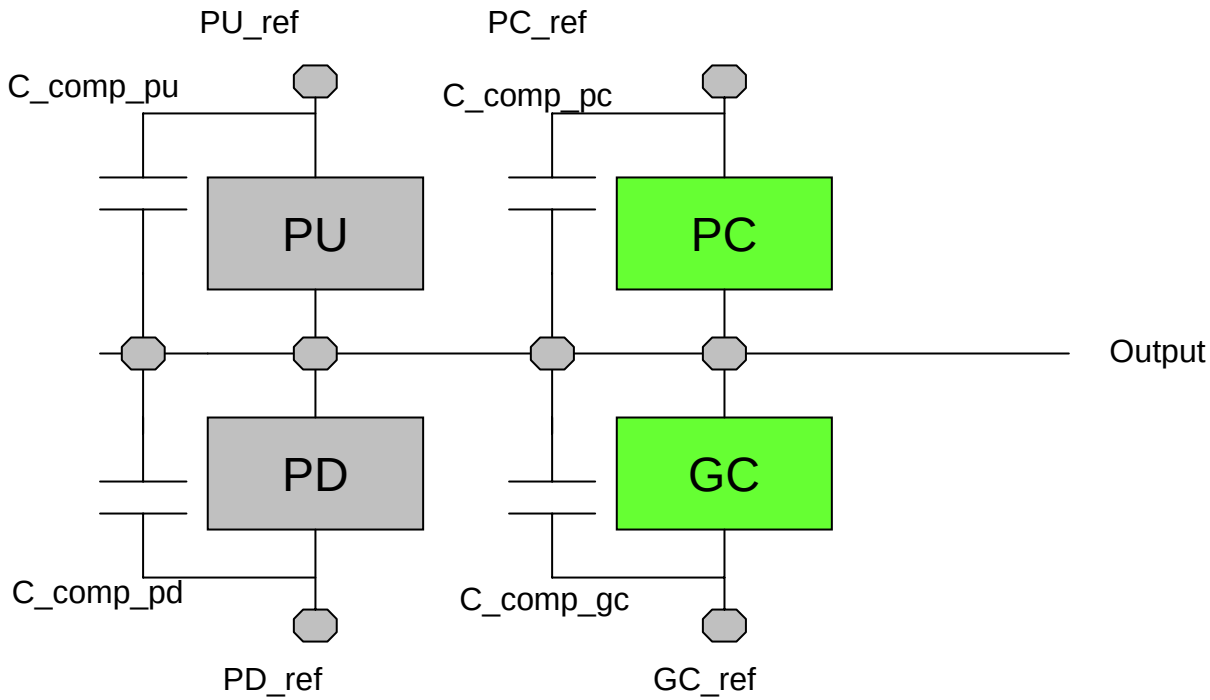
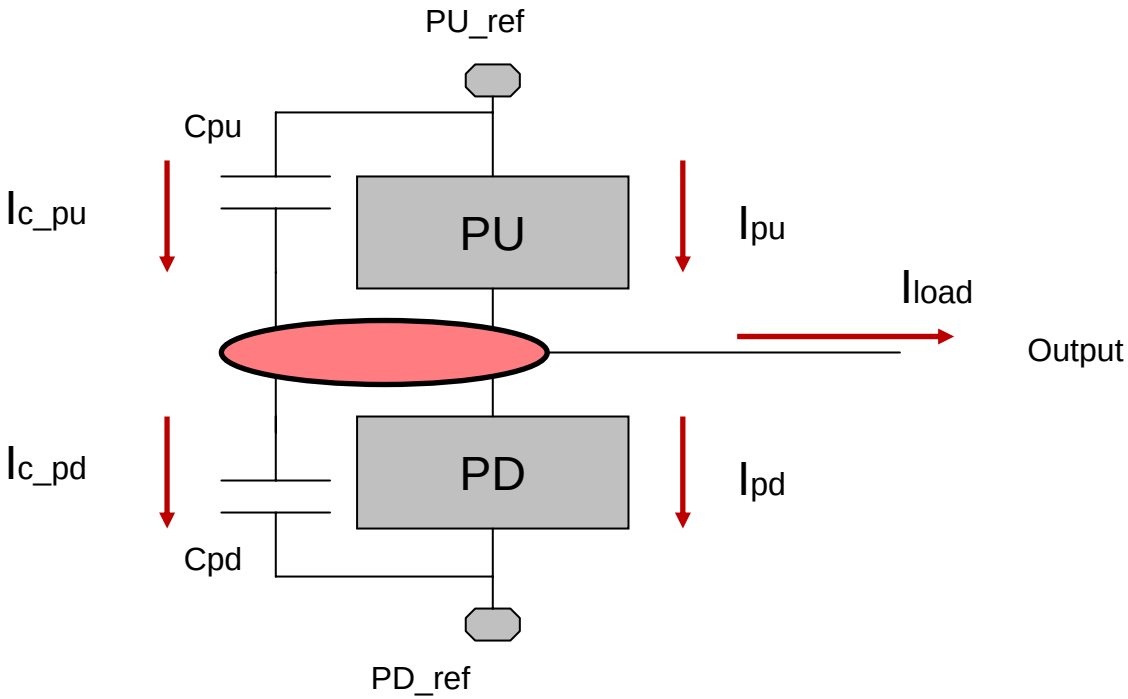
# Outline

- C_comps in IBIS
- How do C_comps affect simulations?
- What does HSpice Transistor-Level model give?
- Conclusions

# C_comps in IBIS



# C_comps in IBIS



# How do C_comps affect simulations?

$I_{pu} + I_{c\_pu} + I_{pd} + I_{c\_pd} - I_{load} = 0$ ---- (1)

$I_{load} = F_{pu} + C_{pu}*(dV_{pu}/dt) + F_{pd} + C_{pd}*(dV_{pd}/dt)$ ---- (2)

Where:

$F_{pu}$ is from V/I Pullup

$F_{pd}$ is from V/I Pulldown

$V_{pu} = V_{pu\_ref} - V_{output}$

$V_{pd} = V_{output} - V_{pd\_ref}$

From (2):

$I_{load} = F_{pu} + F_{pd} + C_{pu}*(dV_{pu\_ref}/dt - dV_{output}/dt) + C_{pd}*(dV_{output}/dt - dV_{pd\_ref}/dt)$

$= F_{pu} + F_{pd}$

$+ (C_{pu}* dV_{pu\_ref}/dt - C_{pd}* dV_{pd\_ref}/dt) + (- C_{pu} + C_{pd})*(dV_{output}/dt)$ ---- (3)

From (3) using fixed PU_ref and PD_ref:

$I_{load} = F_{pu} + F_{pd} + C_{pwr\text{-}gnd} + (- C_{pu} + C_{pd})*(dV_{output}/dt)$ ---- (4)

Where $C_{pwr\text{-}gnd} = C_{pu}* dV_{pu\_ref}/dt - C_{pd}* dV_{pd\_ref}/dt = 0$

# How do C_comps affect simulations?

$I_{load} = F_{pu} + F_{pd} + (- C_{pu} + C_{pd})*(dV_{output}/dt)$ ---- (4')

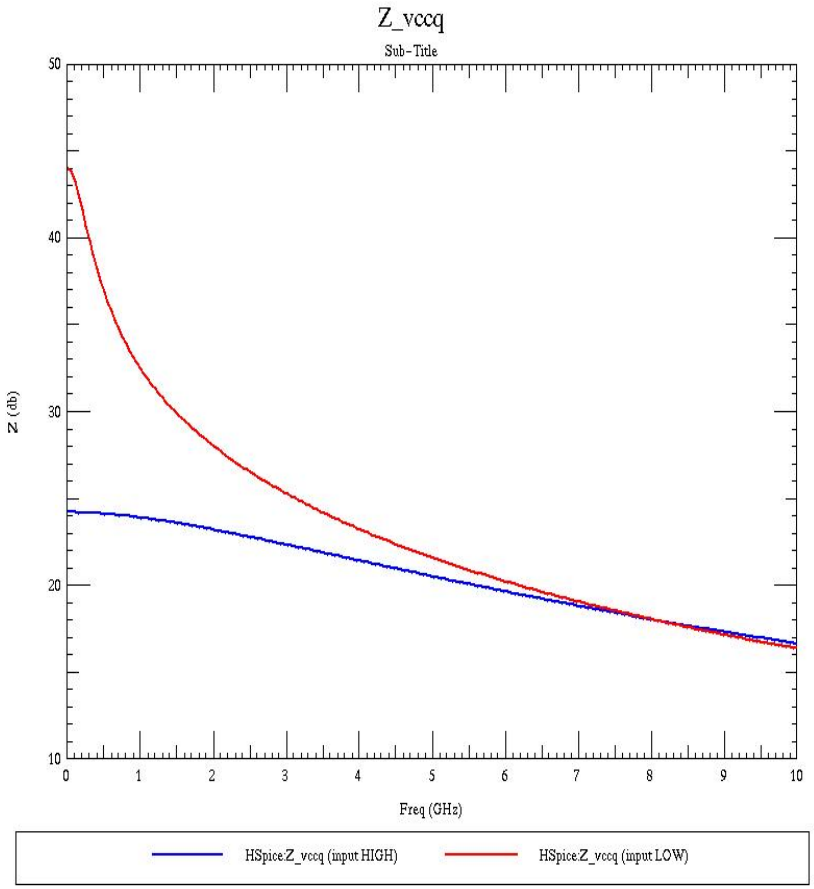
When Input State steady (Quiet Line)

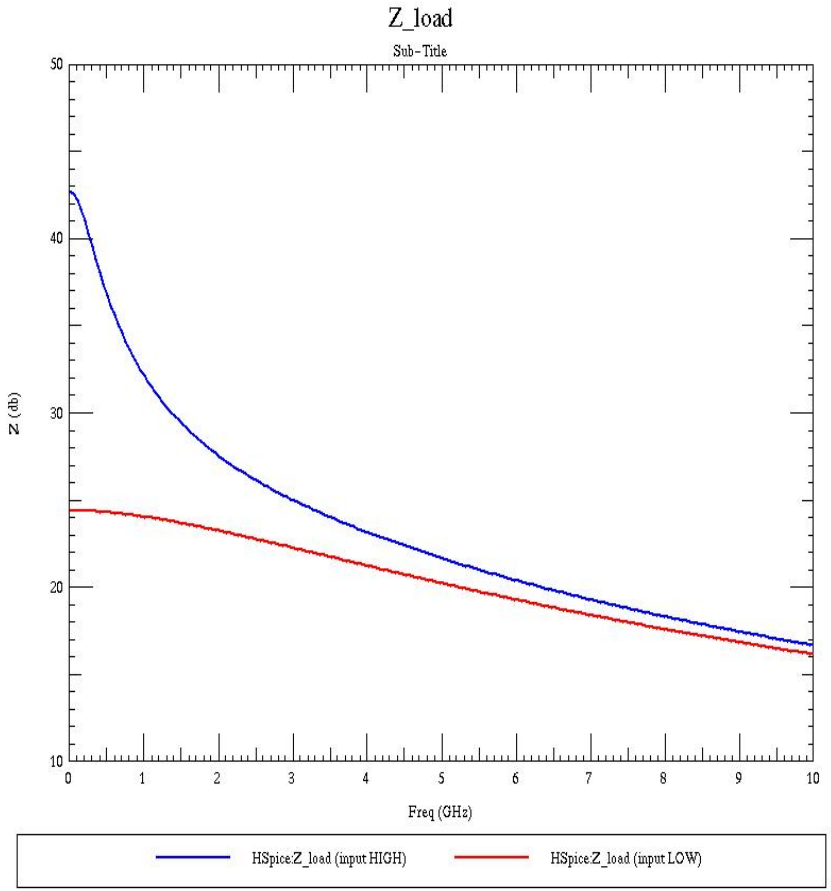
$I_{load}$ changes are depended on $(- C_{pu} + C_{pd})*(dV_{output}/dt)$, So,

$I_{load} = f((C_{pd} - C_{pu})*(dV_{output}/dt))$

**The key is ($C_{pd}$ – $C_{pu}$) !**

# What does HSpice Transistor-Level model give?




- Used the same Micron Model (u27a_dp) that Cisco used in the last result presentation

# Conclusion

- C_comp (PU/PD) ratio is changing when Input-State from Low-High
  - They are almost switched as we showed in last slide
- Simulation should NOT give a correct results for the Quiet lines on both Low and High states if it used a fixed ratio of C-comps!