IBIS Futures Subcommitte Special Meeting

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IBIS Simultaneous Switching Output Simulations Criticality

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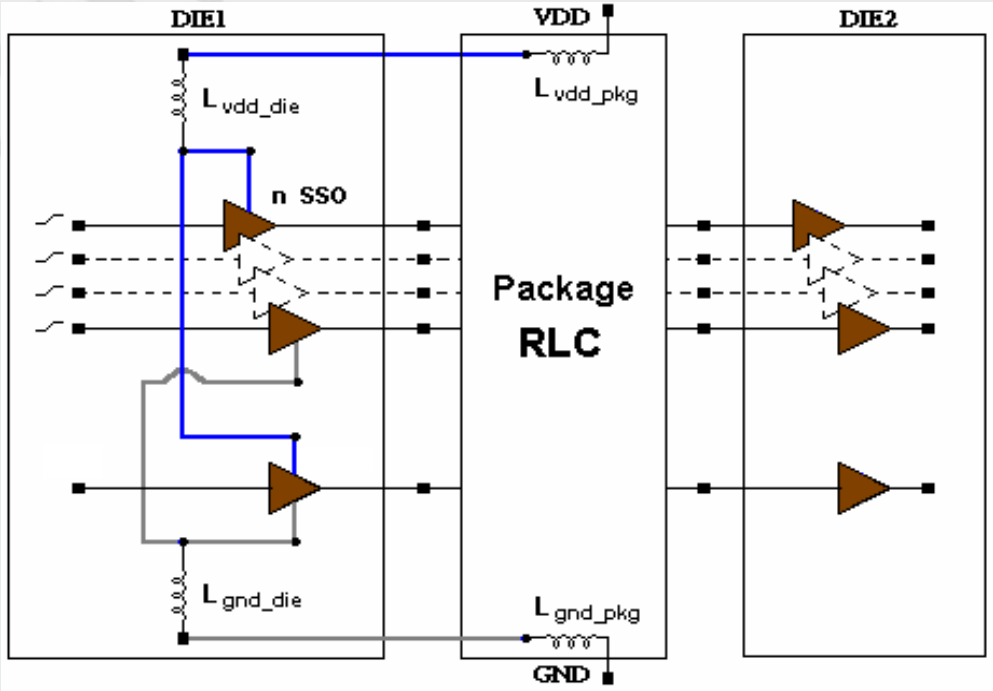
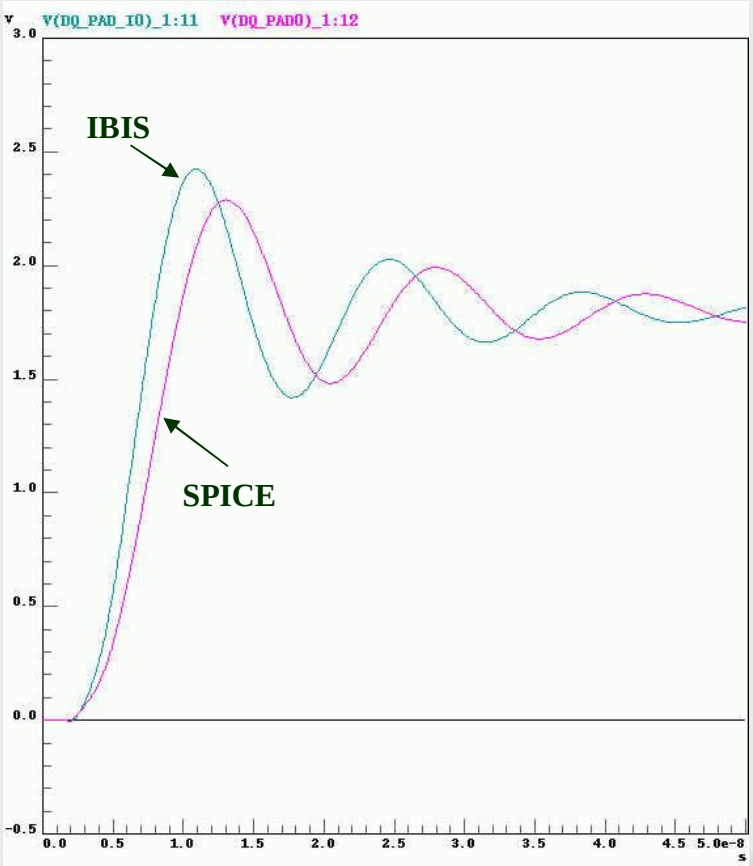
Summary

- IBIS Simultaneous Switching Output Simulations
- Power Network Model Back-annotation
- IBIS “Gate Modulation Effect” Criticality and suggested Solution
- Results of the identified solution obtained by IBIS-VHDL-AMS implementation
- Conclusions

IBIS Simultaneous Switching Output Simulations





The IBIS simultaneous switching outputs simulations are not accurate for two reasons:

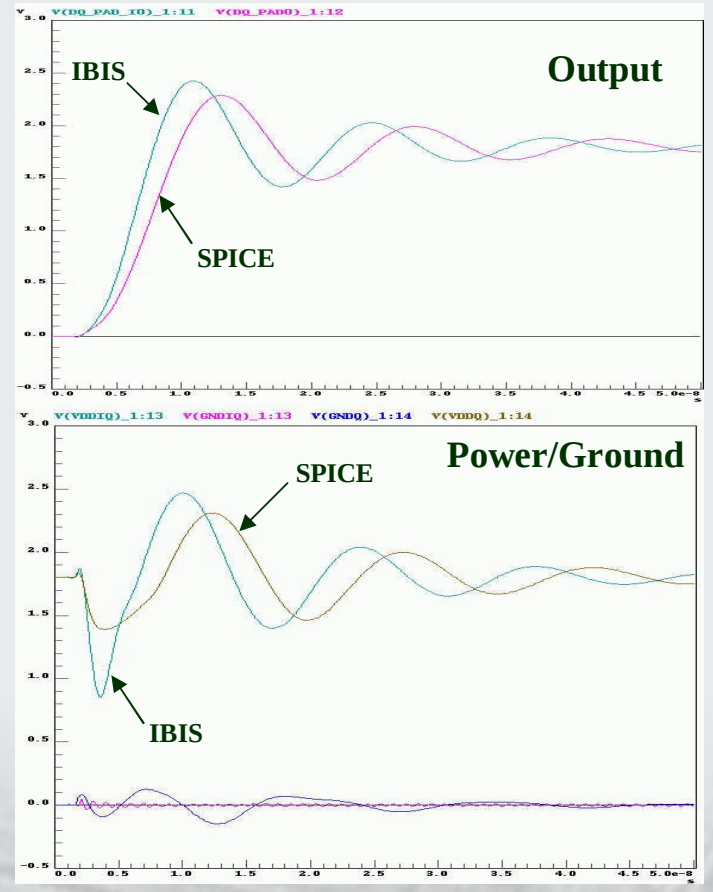
1) The power network is not modelled in the standard IBIS model

2) Lack of the "Gate Modulation Effect"

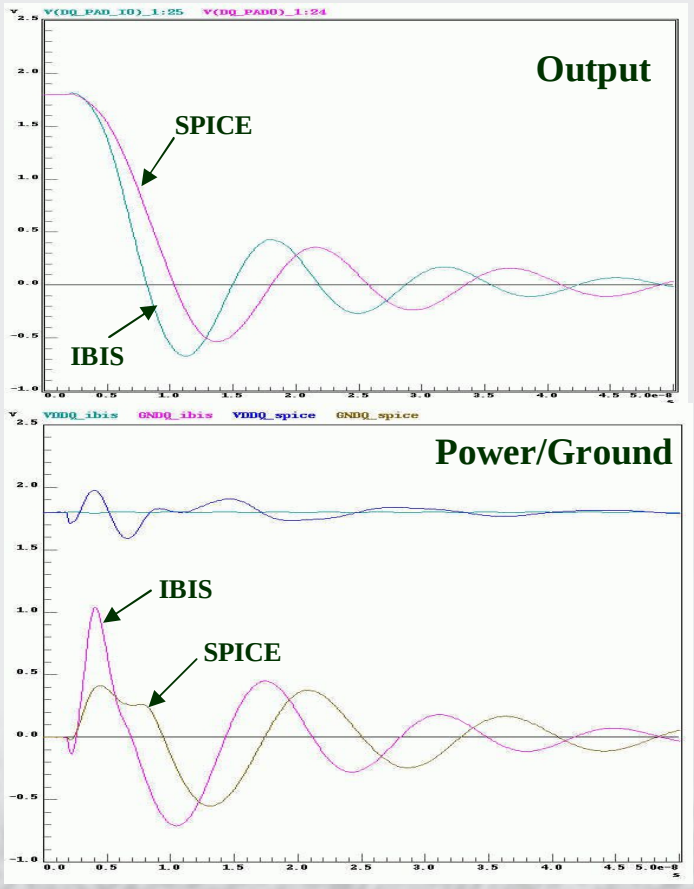
Benchmark SPICE vs IBIS(Standard)

High mismatching of both output and power/ground signals behaviour

SSO – Rise Transition



SSO – Fall Transition



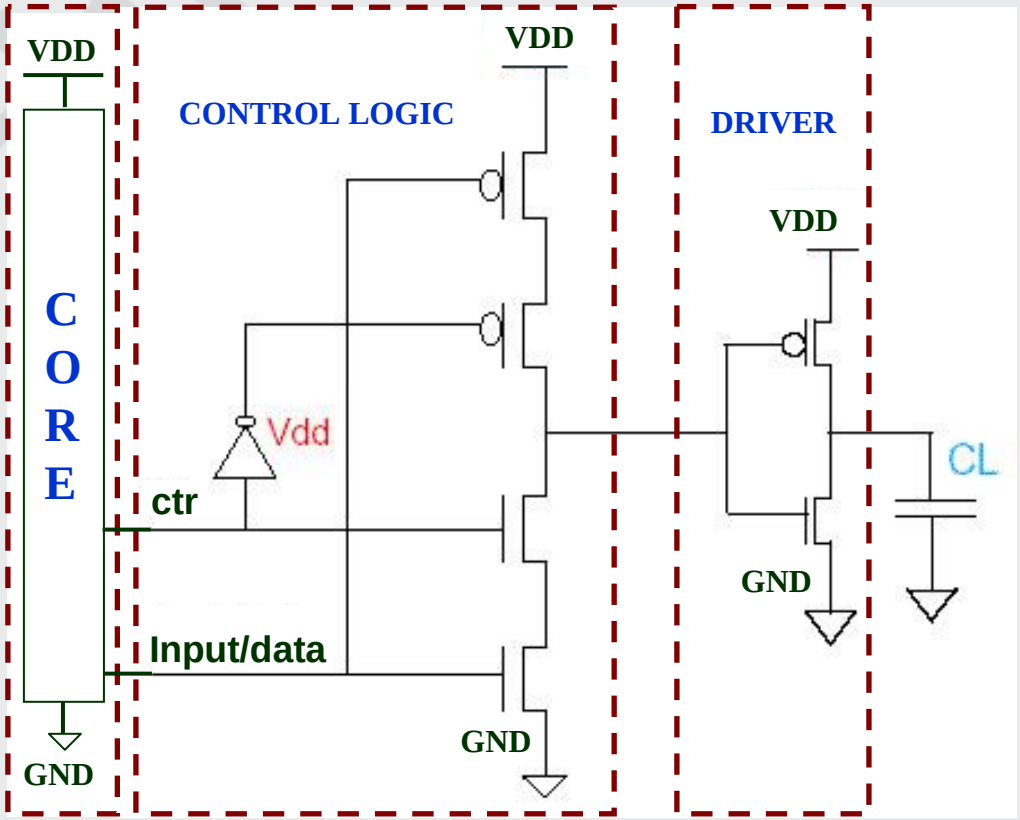
Relative Percentage Error

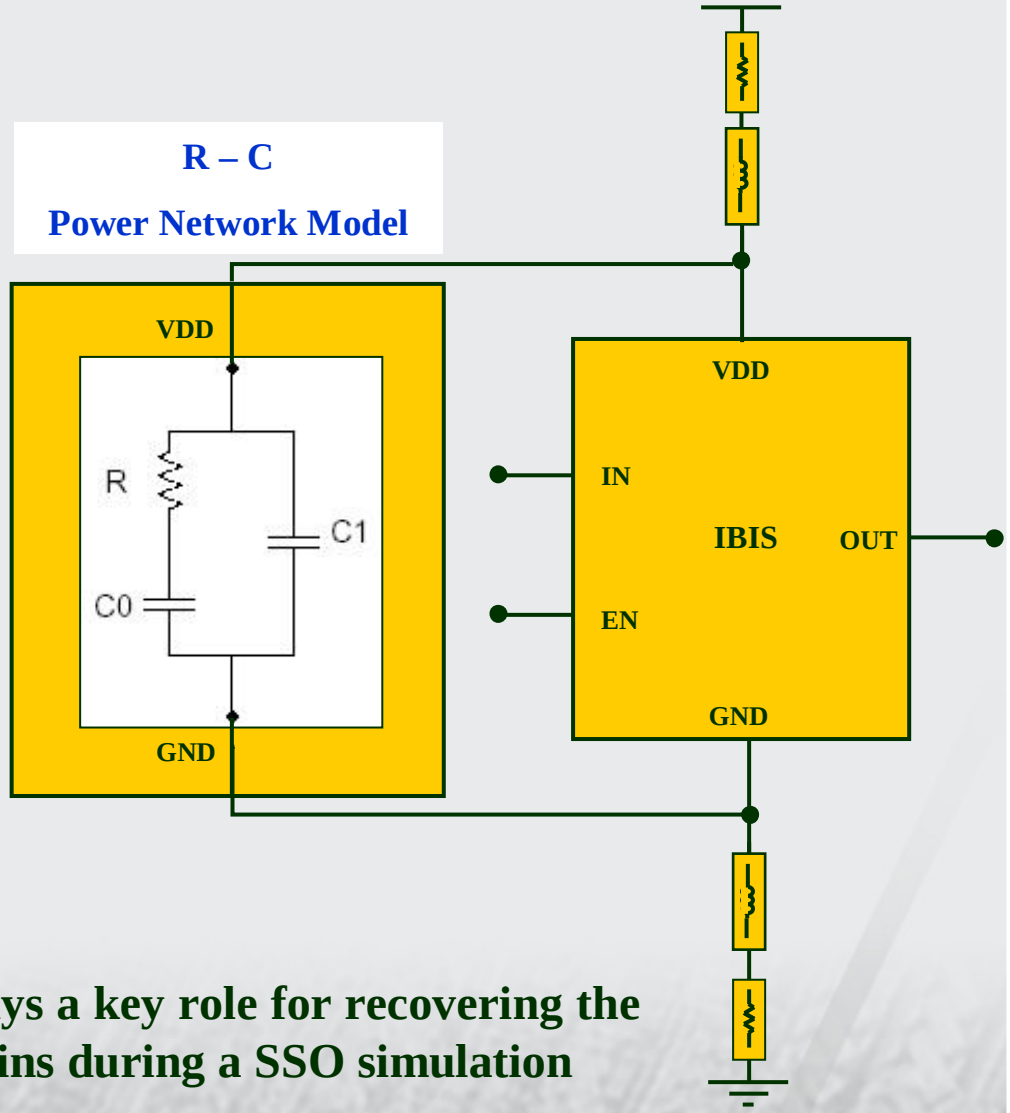
Max delay = 22%

Max ringing = 25%

Diff. Power supply = 32%

Power Network Model

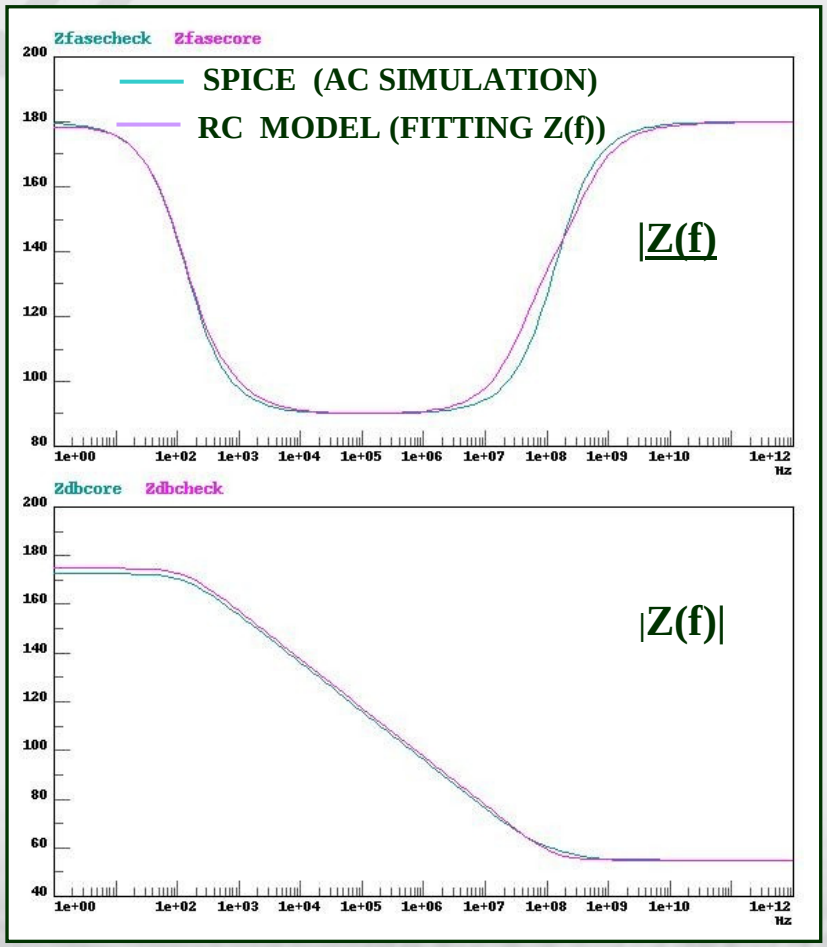




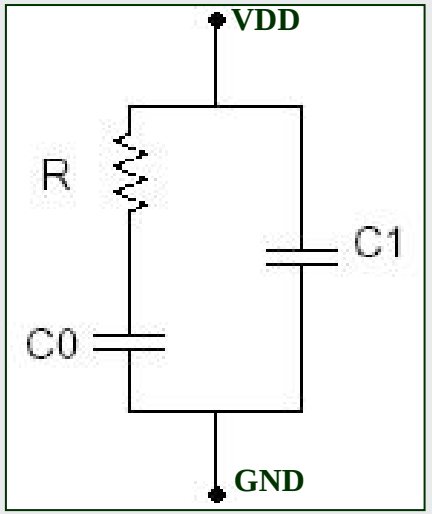
The RC equivalent load of the power network plays a key role for recovering the correct dynamic behaviour of the Vdd and Gnd pins during a SSO simulation

Power Network Model Extraction

Z(f) impedance between Vdd and Gnd nodes

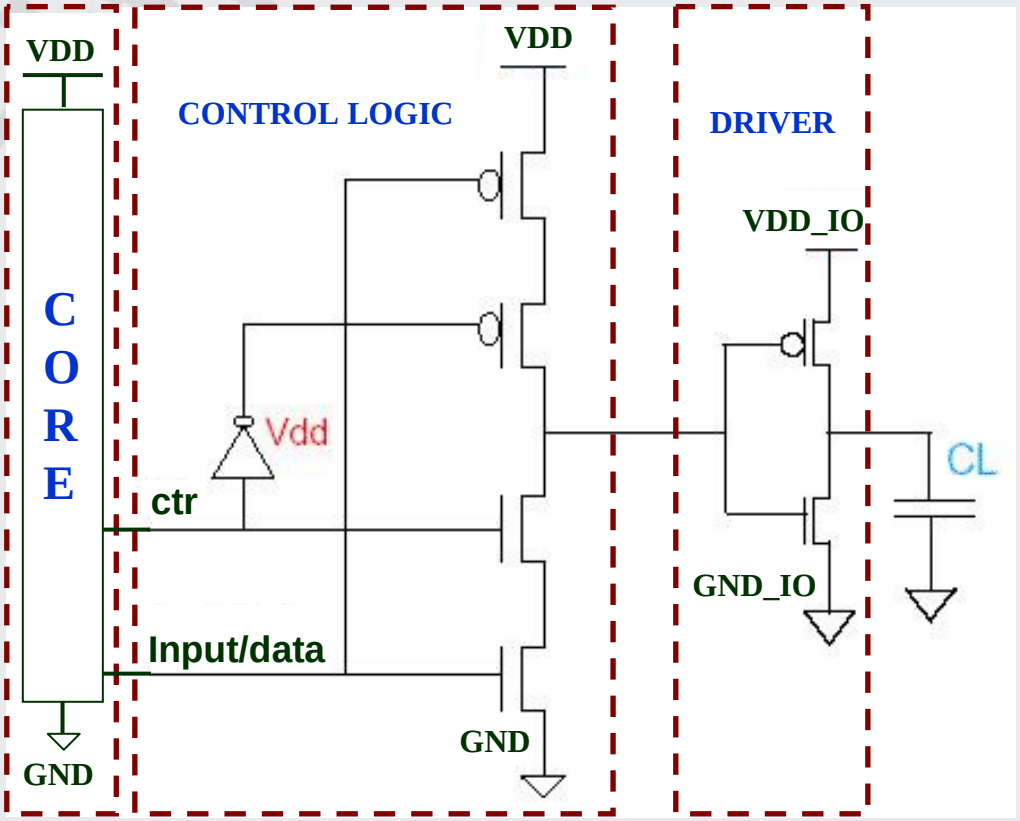


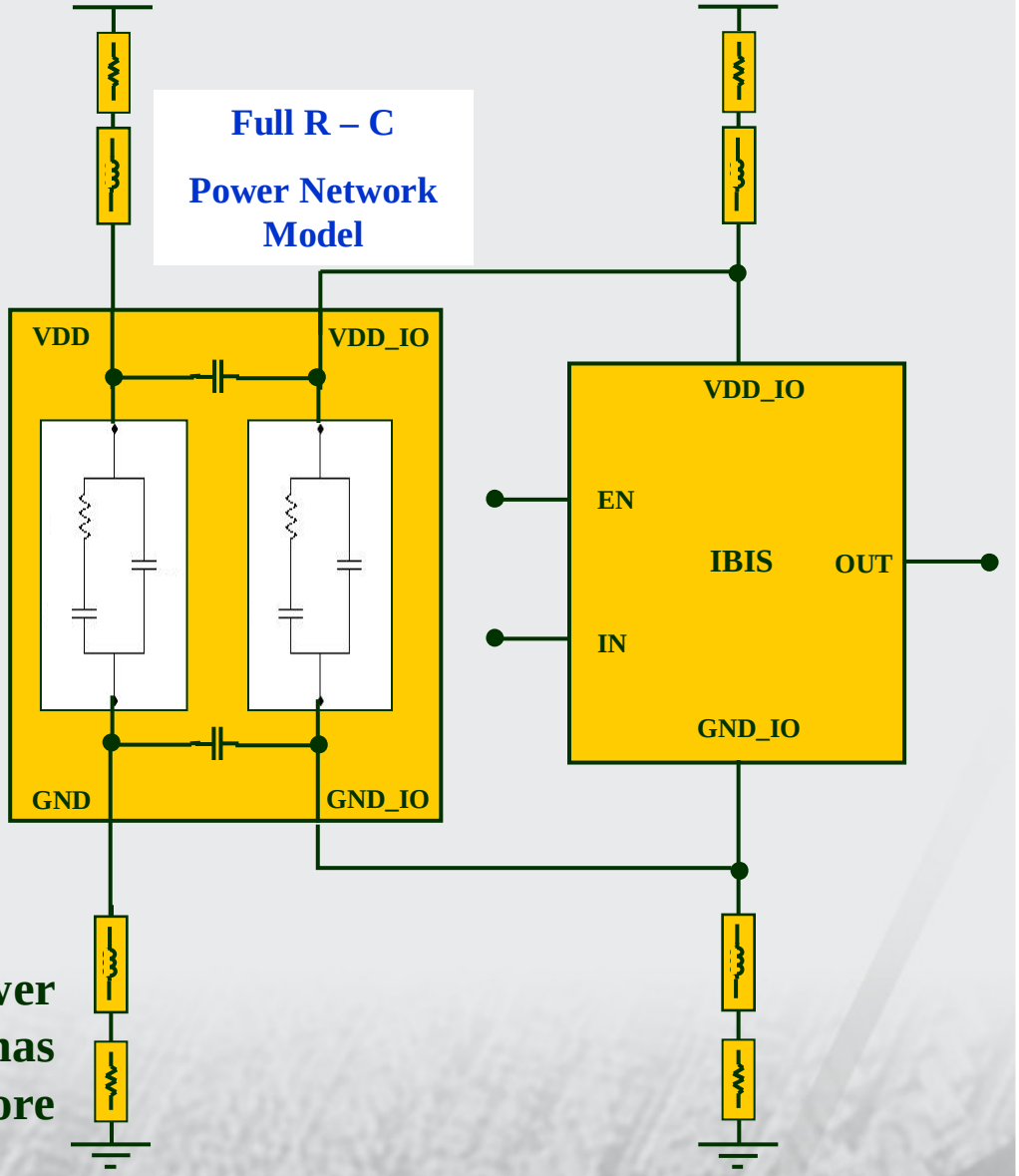
R-C equivalent model extracted



The R-C equivalent model has been extracted by fitting the frequency-dependent impedance Z(f)

Power Network Model: Vdd and Vdd_io



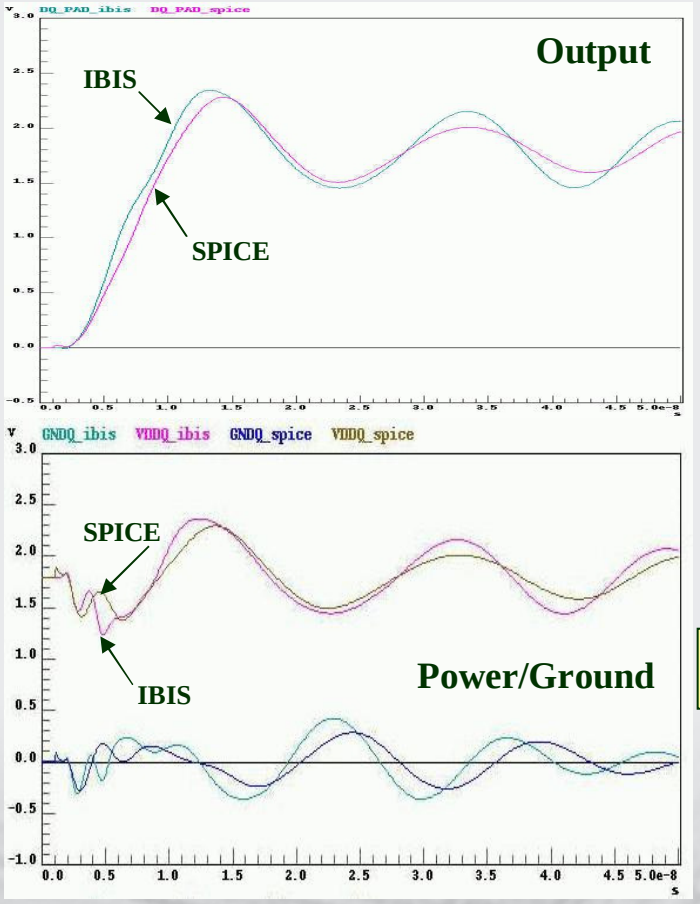


When the drivers are powered by a dedicated power supply voltage, the related R-C equivalent load has to be linked with the one of the control logic+core circuit.

Benchmark SPICE vs IBIS(RC Power Model)

Good IBISvsSpice matching for power/ground signals by RC model back-annotation

SSO – Rise Transition



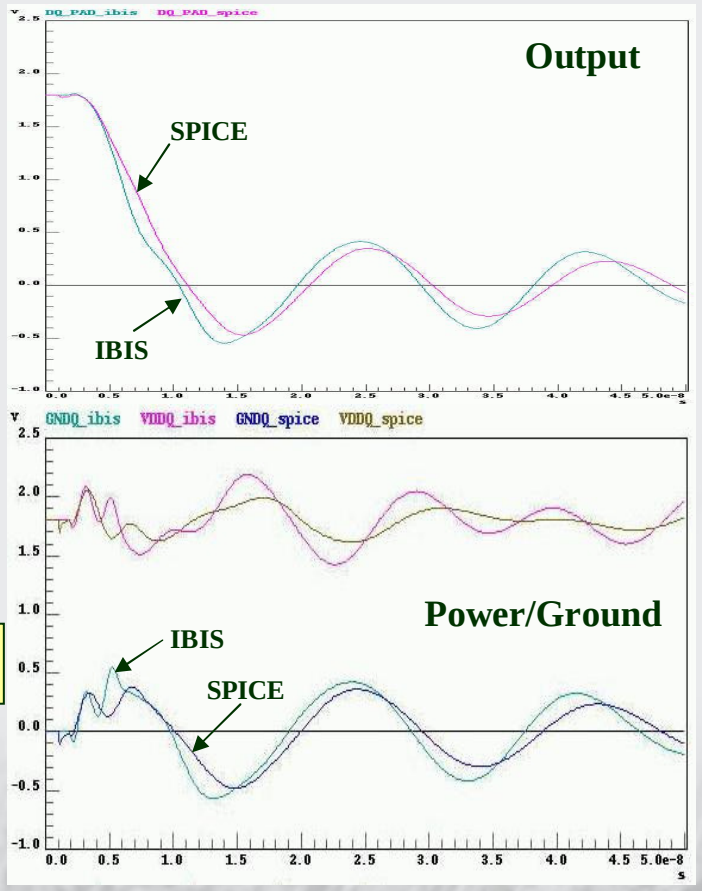
Relative Percentage Error

Max delay = 17% (22% IBIS std)

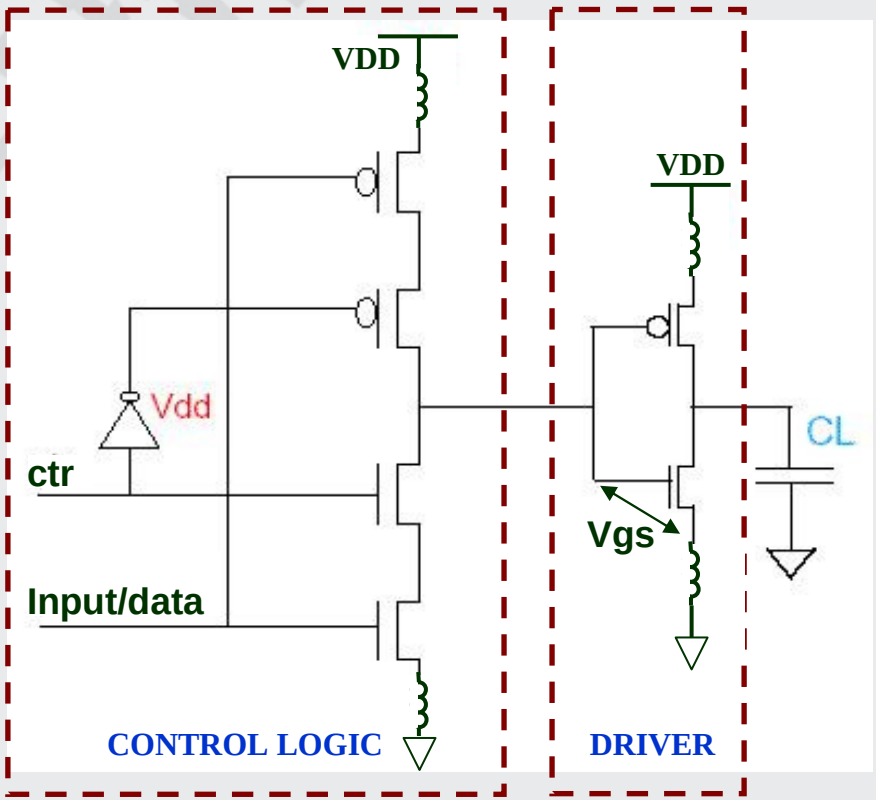
Max ringing = 18% (25% IBIS std)

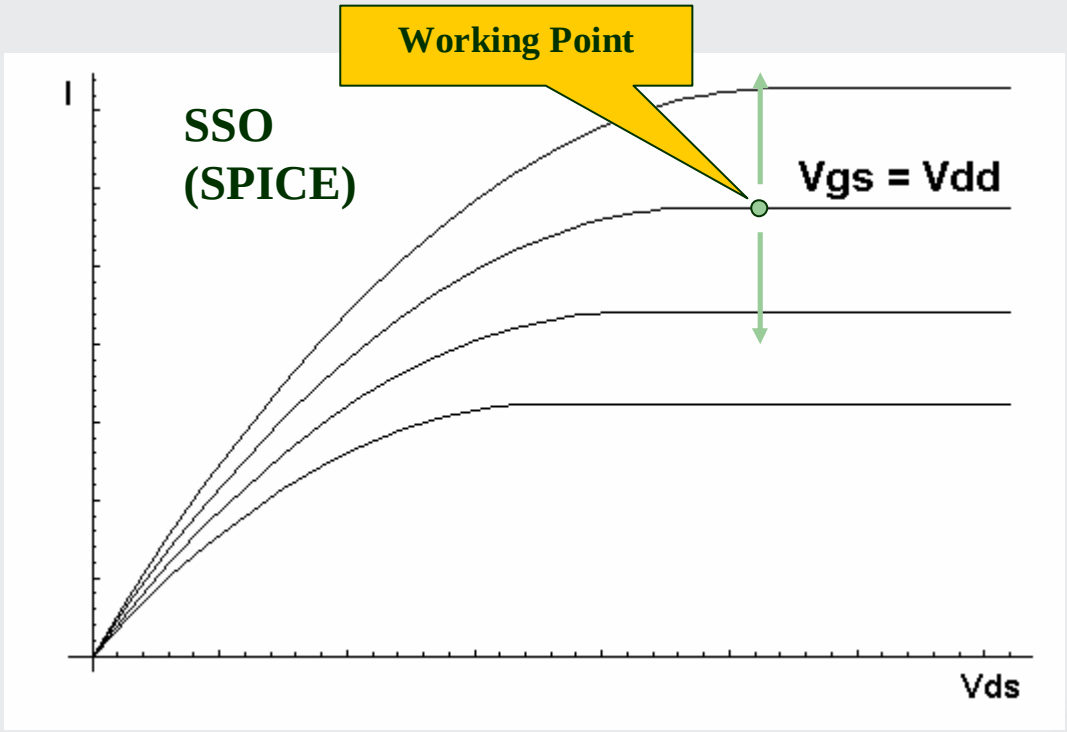
Diff. Power supply = 4% (32% IBIS std)

SSO – Fall Transition



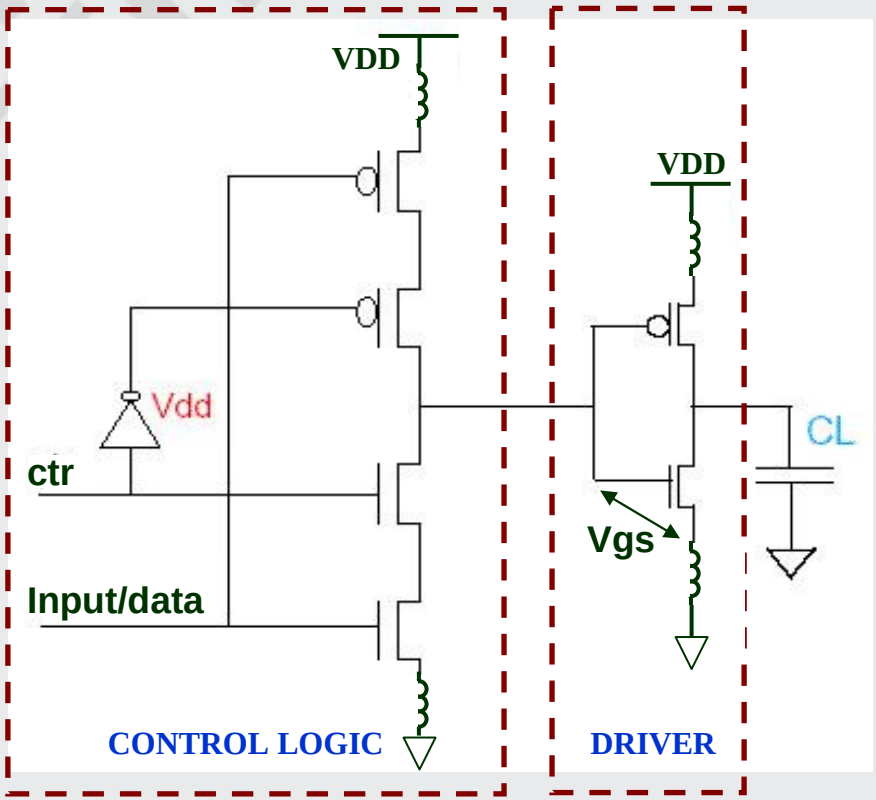
Gate Modulation Effect

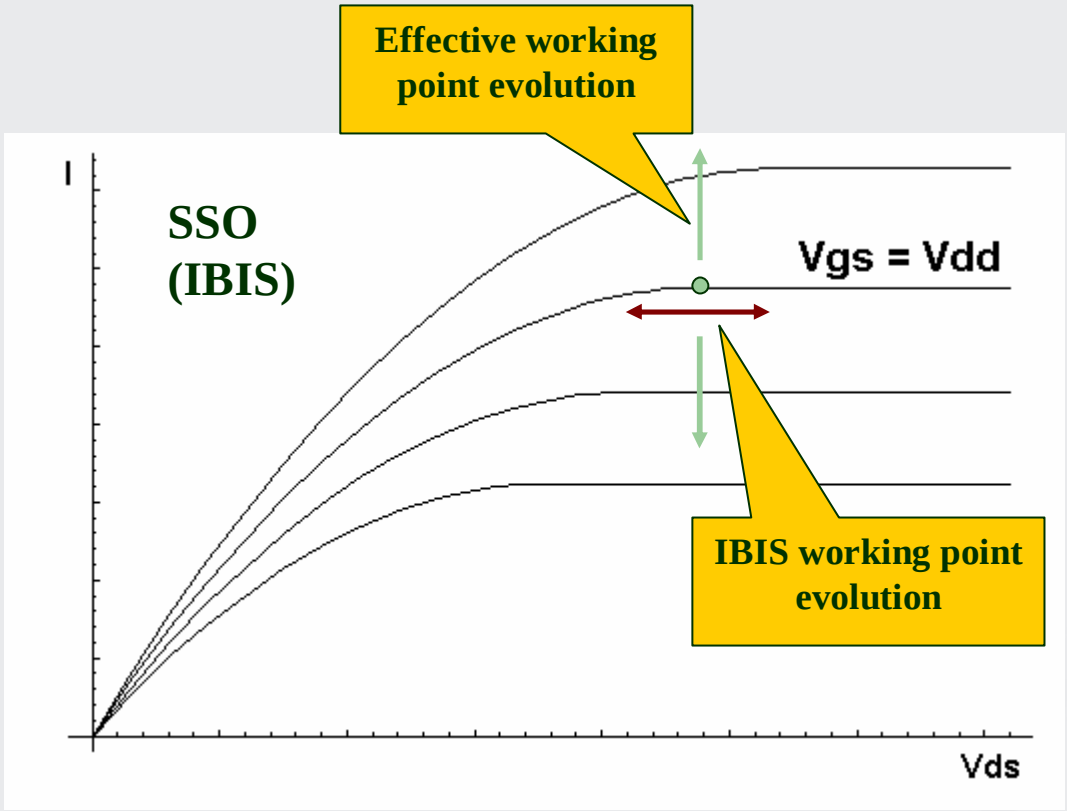




The simultaneous switching noise causes a change of the MOS Vgs voltage, therefore the working point will move along different Vgs characteristics

IBIS Gate Modulation Criticality





The IBIS simulation of a simultaneous switching noise does not model correctly the MOS Vgs voltage variation because the working point will move only along the same Vgs =Vdd characteristic.

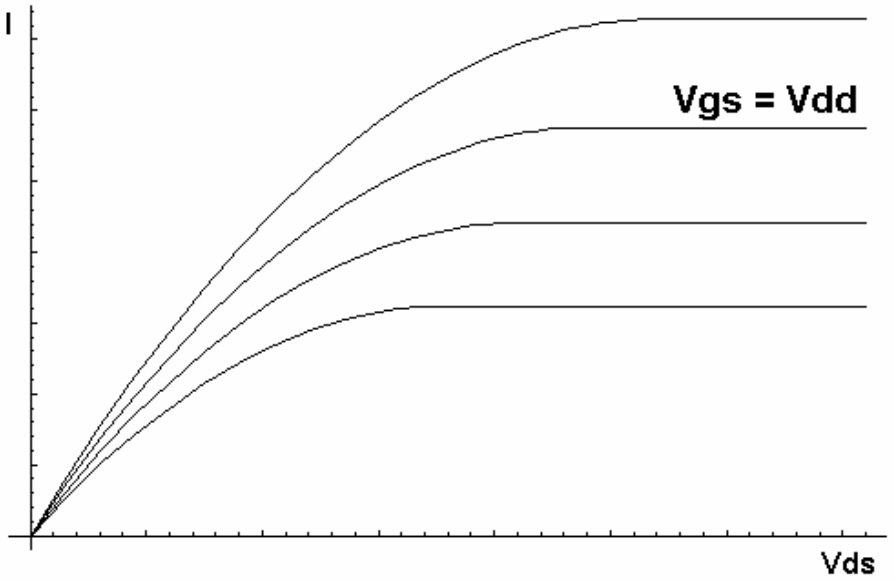
The higher is the bouncing noise, the higher is the mismatching between IBIS and Spice results

Gate Modulation Coefficients

MOS Level 1 equation (threshold voltage 0.6V):

$$y = \{[2(v_{gs}-0.6)x - x^2]u(v_{gs}-x-0.6) + (v_{gs}-0.6)^2 u(x-v_{gs}+0.6)\}u(v_{gs}-0.6)$$

MOS Level 1 characteristics:



$$k_{ssn-pulldown} = \frac{I(v_{gs}, vds)}{I(v_{gs}=vdd, vds)}$$

$$k_{ssn-pullup} = \frac{I(v_{sg}, vsd)}{I(v_{sg}=vdd, vsd)}$$

I(Vgs, Vds) = Kssn(Vgs,Vds)*I(Vgs=Vdd,Vds)

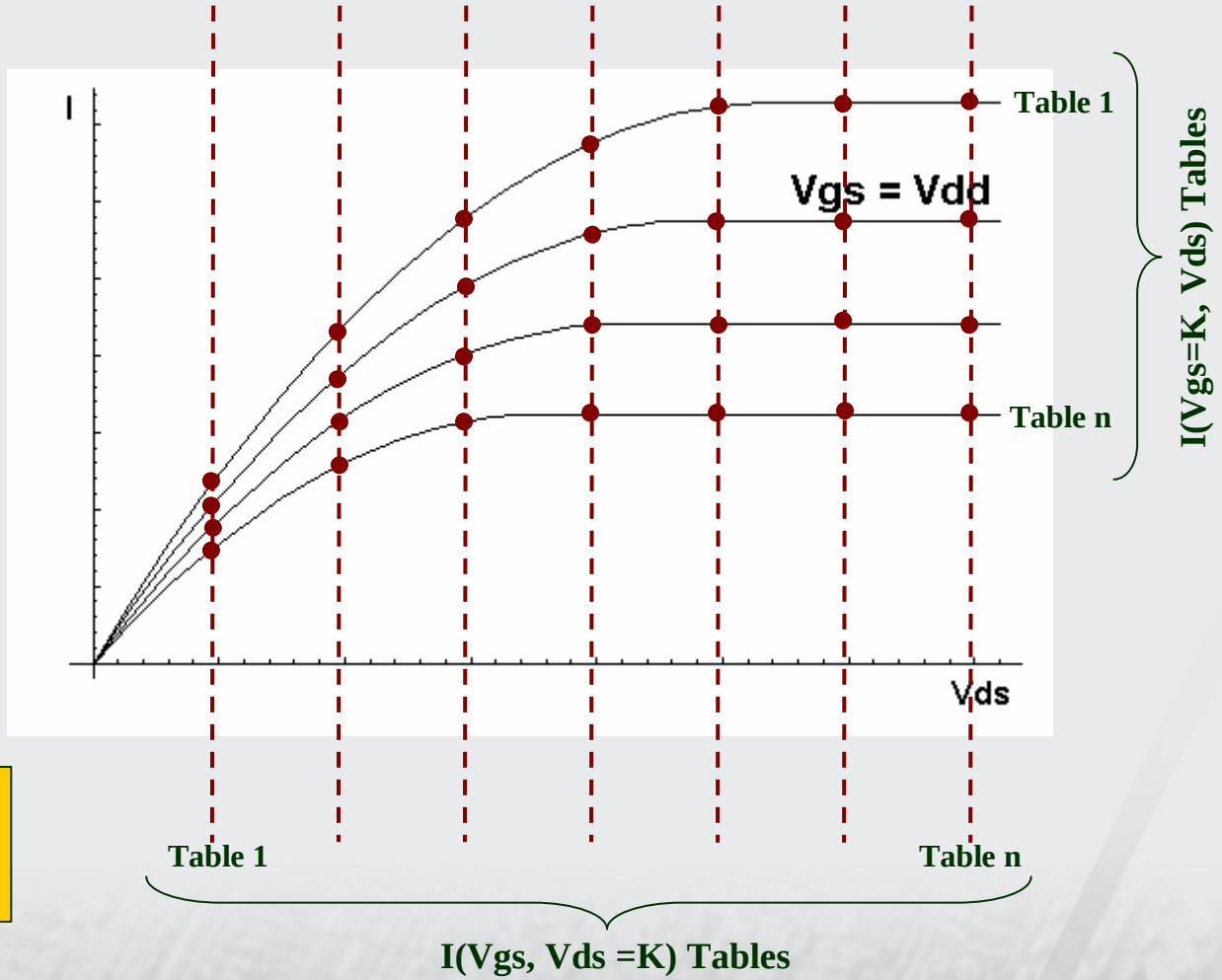
Effective SPICE current

IBIS standard current

Ieff = Kssn(Vgs,Vds)*Istd

I(Vgs,Vds) Tables Choice

Note: K means constant value!!!

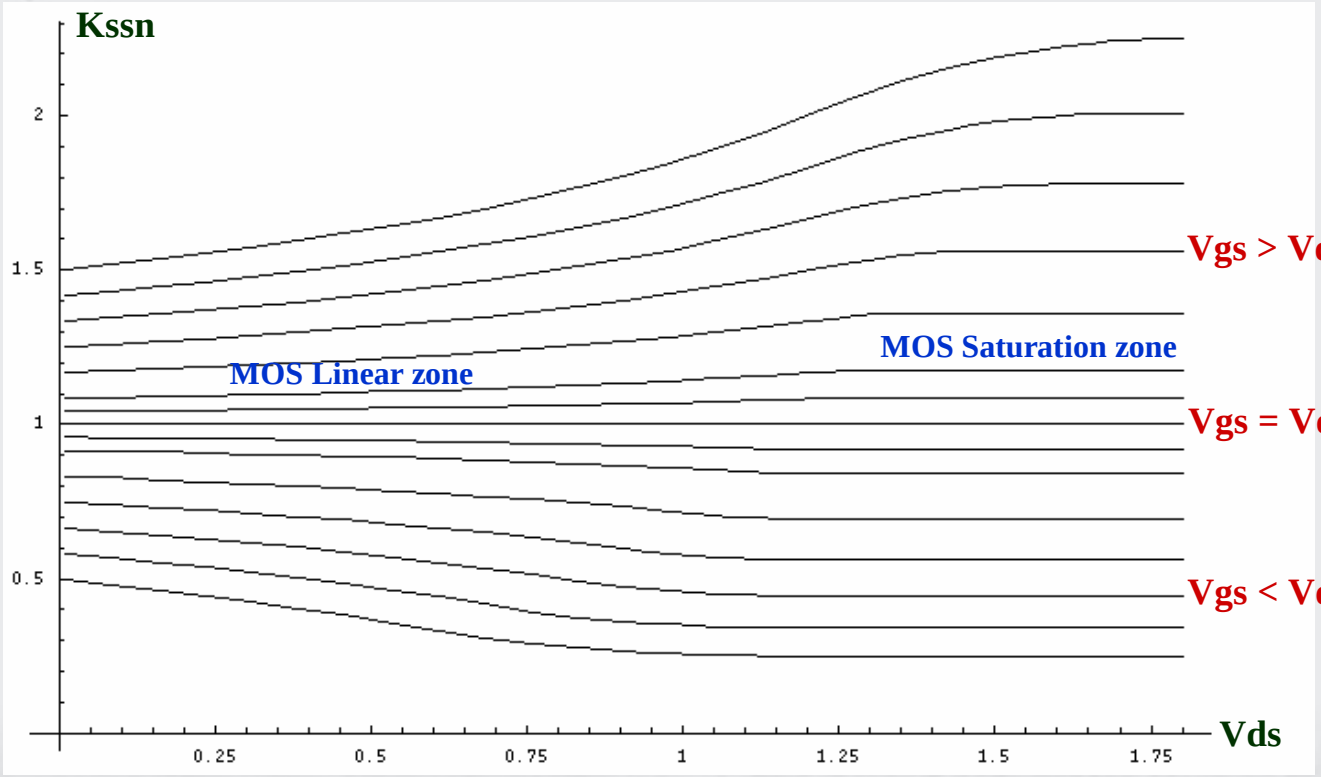


The effort has been focused to identify an easy implementation of the Kssn coefficients, which also guarantees a good level of accuracy and computational time.

Gate Modulation Coefficient Characteristics

Gate modulation coefficient equation based on the MOS level 1 equation (Vdd=1.8V):

$$k_{ssn-pulldown} = \frac{[2(v_{gs}-0.6)x - x^2]u(v_{gs}-x-0.6) + (v_{gs}-0.6)^2 u(x-v_{gs}+0.6)}{[2.4x - x^2]u(v_{gs}-x-0.6) + (1.2)^2 u(x-v_{gs}+0.6)}$$



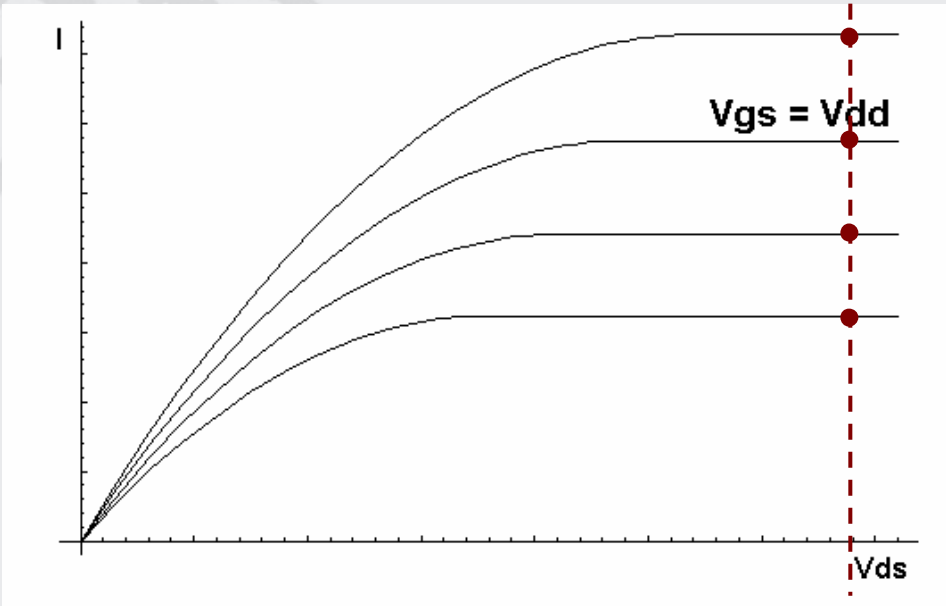
Vgs > Vdd ⇒ Kssn > 1 ⇒ Ieff > Istd

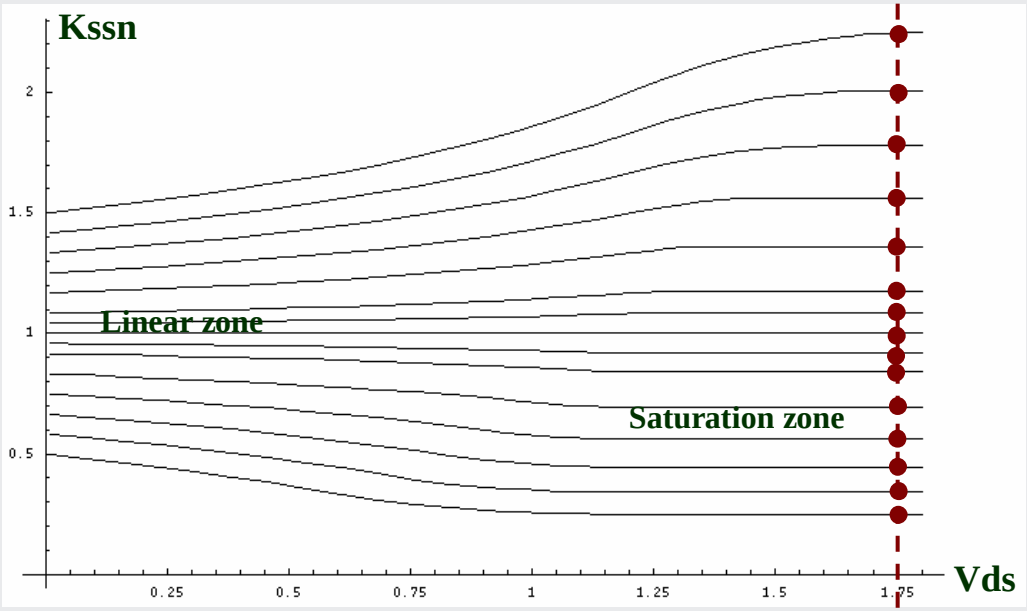
Vgs = Vdd ⇒ Kssn = 1 ⇒ Ieff = Istd

Vgs < Vdd ⇒ Kssn < 1 ⇒ Ieff < Istd

The Kssn coefficient is indipendent from the Vds voltage in the saturation zone and, approximatively, also in the linear zone, in the case of small Vgs changes. Might be enough one I(Vgs, Vds=k) table?

Gate Modulation by one I(Vgs,Vds=K) Table

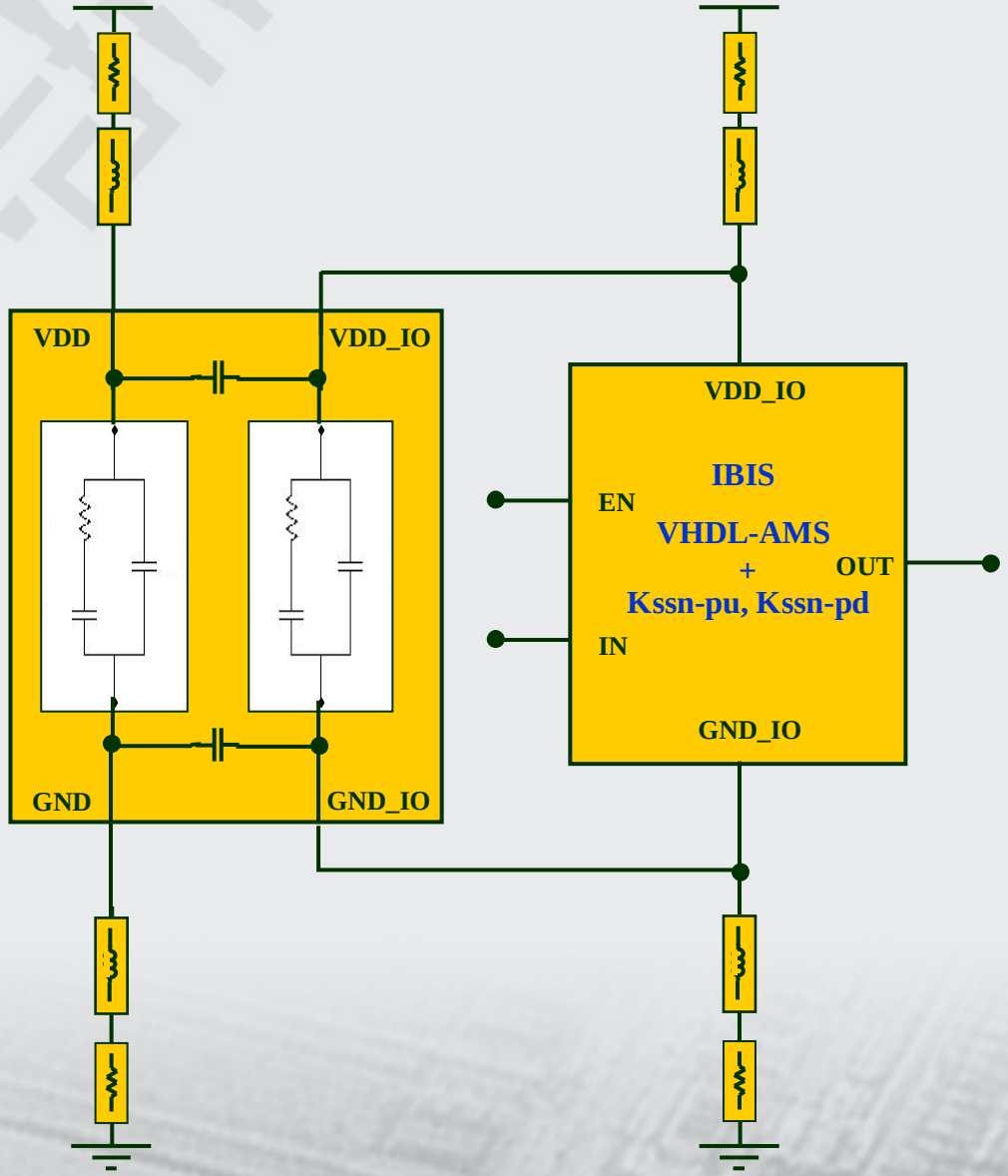


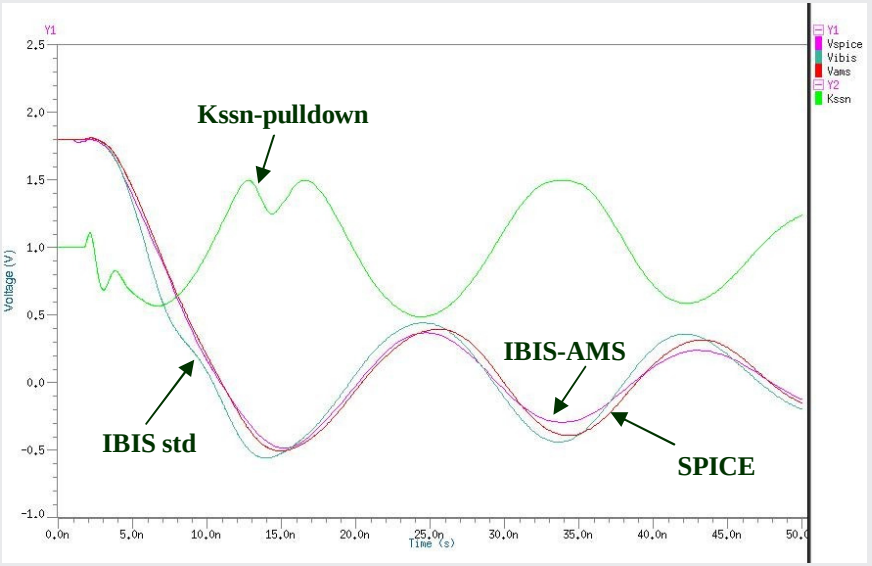


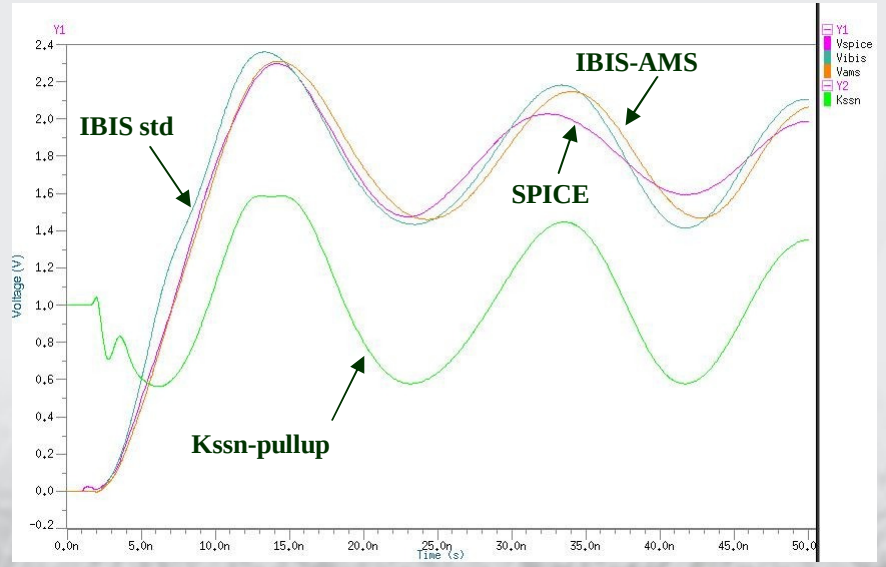
I(Vgs, Vds=K) Table → **Kssn - pulldown**, **Kssn – pullup**, **Ieff = Kssn*Istd**, **VHDL-AMS** → **Kssn-pu, Kssn-pd, Ieff = Kssn*Istd**

As it is not possible to change the EDA tools code which manage the IBIS models, the unique way to implement the Kssn's coefficients is to use the IBIS-VHDL-AMS implementation, adding the Gate modulation coefficients routine.

SSO simulations by IBIS-VHDL-AMS + Kssns coefficients

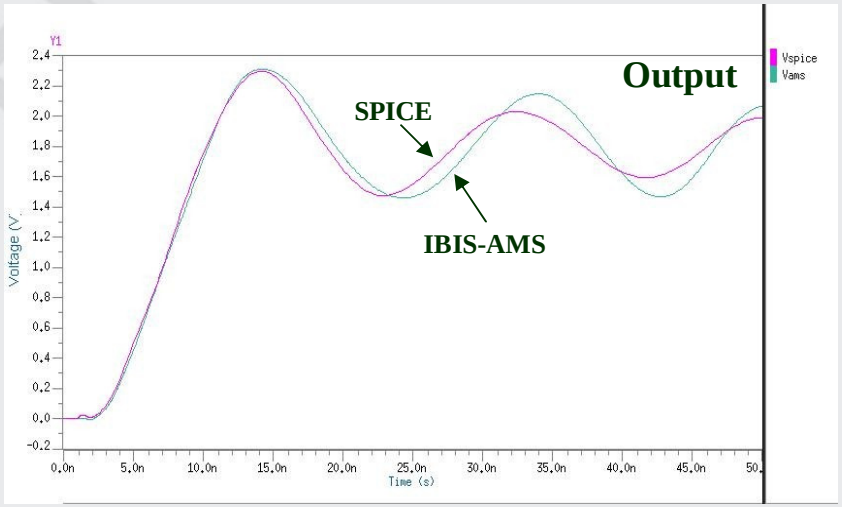


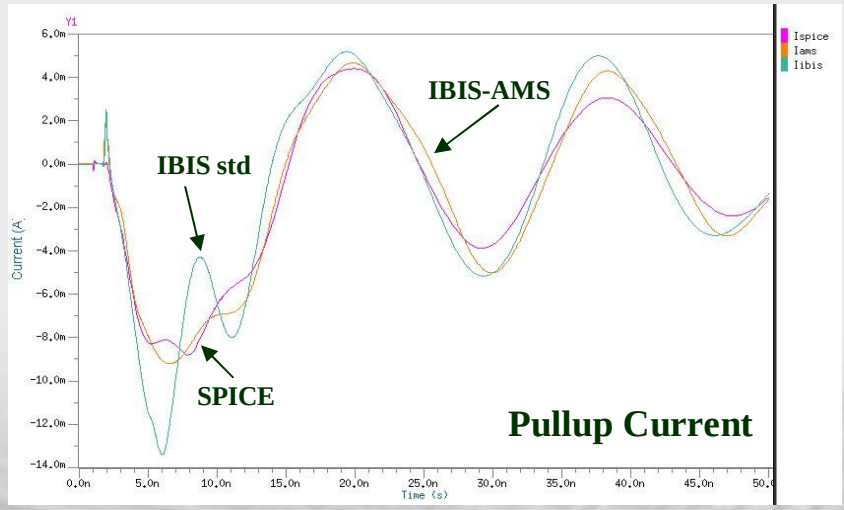




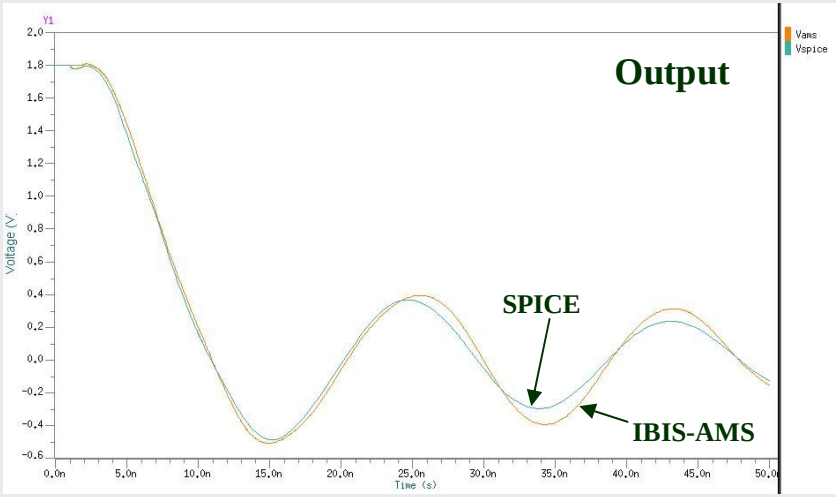
Pullup and Pulldown Currents

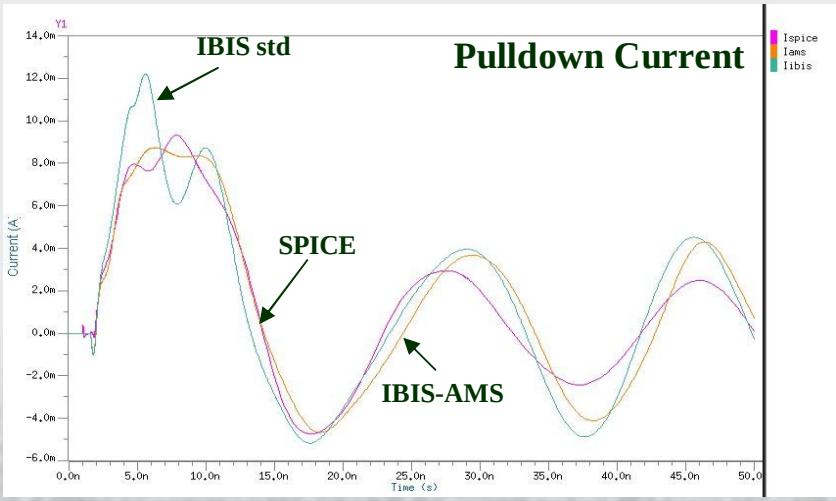
SSO – Rise Transition





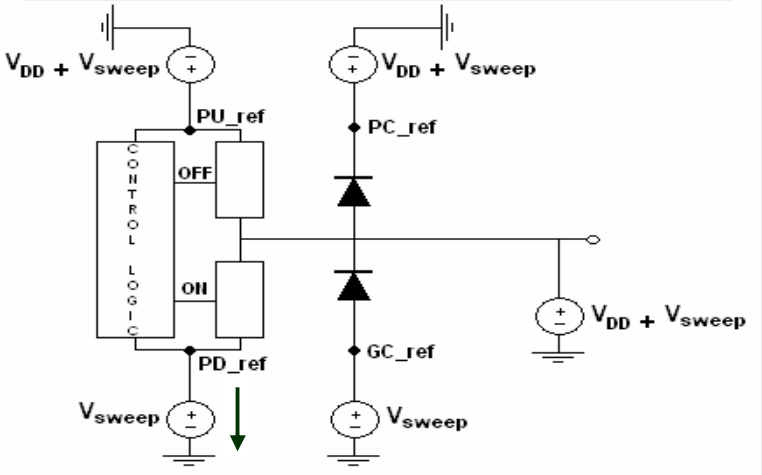
SSO – Fall Transition



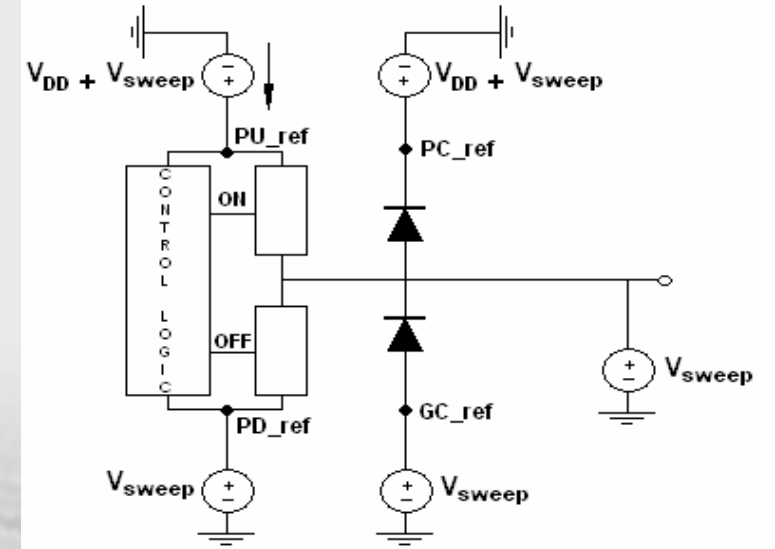


Extraction of the I(Vgs,Vds=K) Table: Initial Choice

Pulldown I(Vgs, Vds=k) table extraction



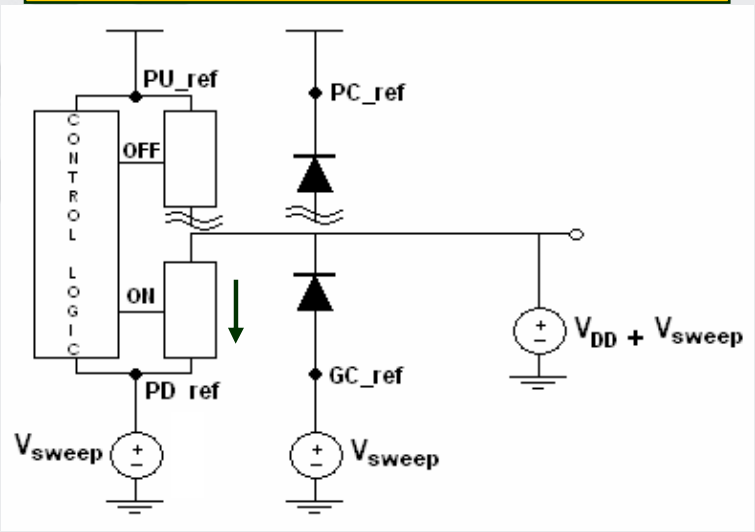
Pullup I(Vgs, Vds=k) table extraction



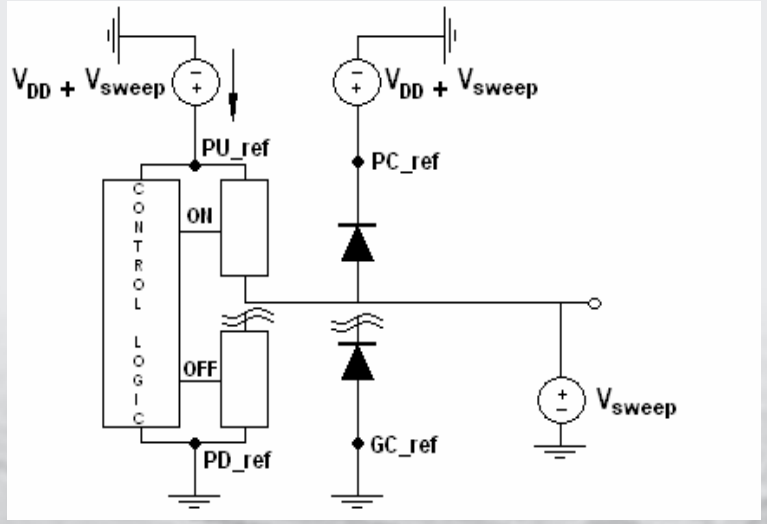
- **Vsweep = [-Vdd, Vdd]**
- **The I-Vgs Pullup and Pulldown tables are extracted with Vds = Vdd**
- **These circuits do not work very well when the control logic and the final stages are powered by the same supply voltage: the behaviour of the control logic and its driving capability to final stage is not modelled correctly.**
- **During the bouncing, gnd and vdd nodes will change together by the bypass+parasitic capacitance, but the magnitude and phase of noise will be different on each one. Therefore, it is not correct to extract the I(Vgs, Vds=Vdd) tables considering the same Vsweep on both Vdd and Gnd nodes.**
- **The best way identified is to disconnect the stage that is not under investigation**

Extraction of the I(Vgs,Vds=K) Table: Final Choice

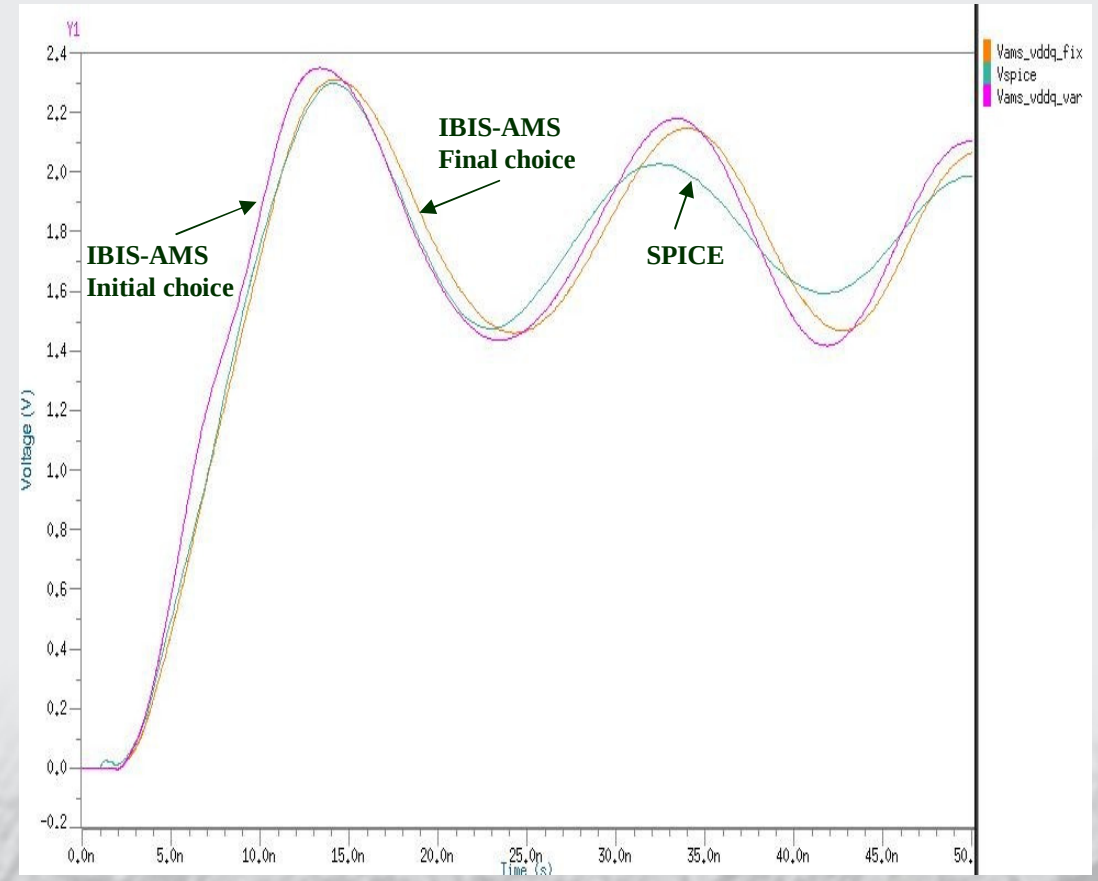
Pulldown I(Vgs, Vds=k) table extraction



Pullup I(Vgs, Vds=k) table extraction



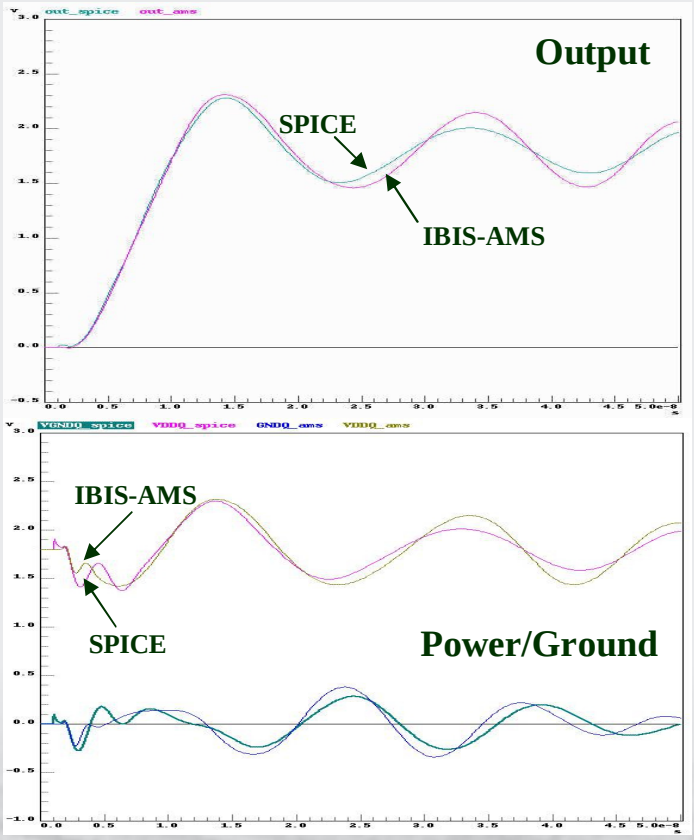
These circuits can be used for extracting I(Vgs, Vds=Vdd) tables for either common and separate power pins of the final stage and control logic circuits.



Benchmark SPICE vs IBIS (Gate Modulation Coefficients)

Very good IBISvsSpice matching for both outputs and power/ground signals

SSO – Rise Transition



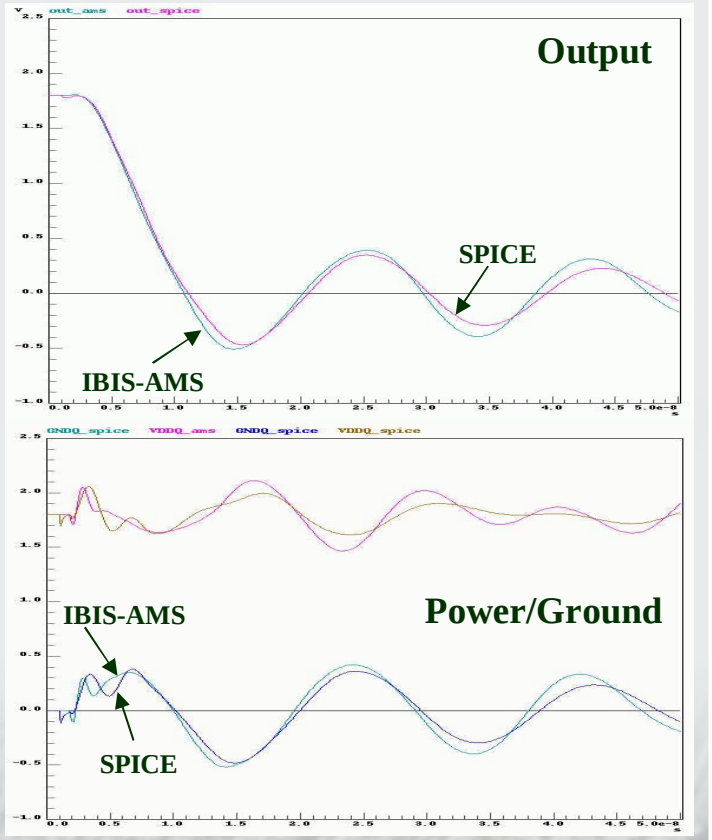
Relative Percentage Error

Max delay = 3% (22% std IBIS)

Max ringing = 8% (25% std IBIS)

Diff. Power supply = 1% (32% std IBIS)

SSO – Fall Transition



Future Plan: Gate Modulation by two I(Vgs,Vds=K) Tables

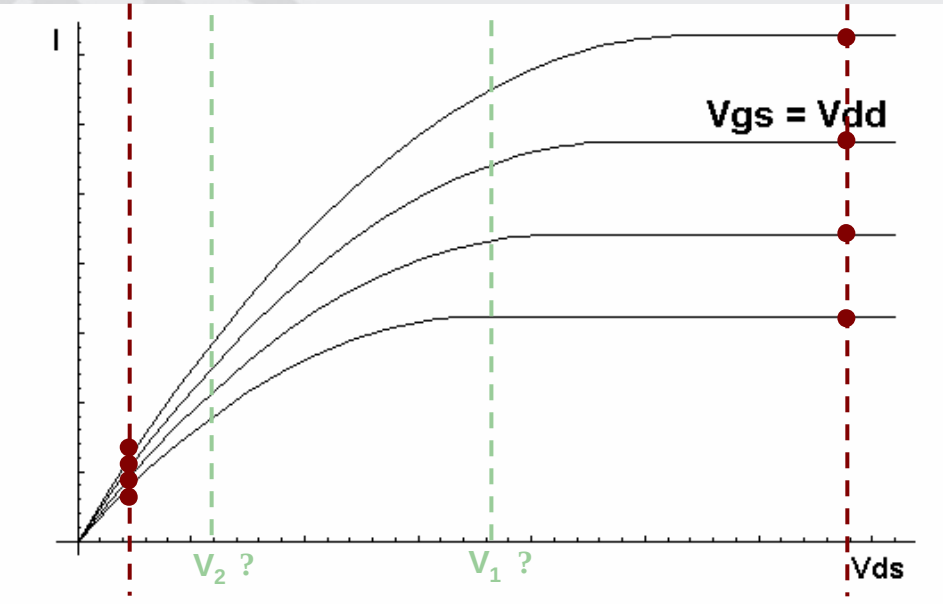


Table 2

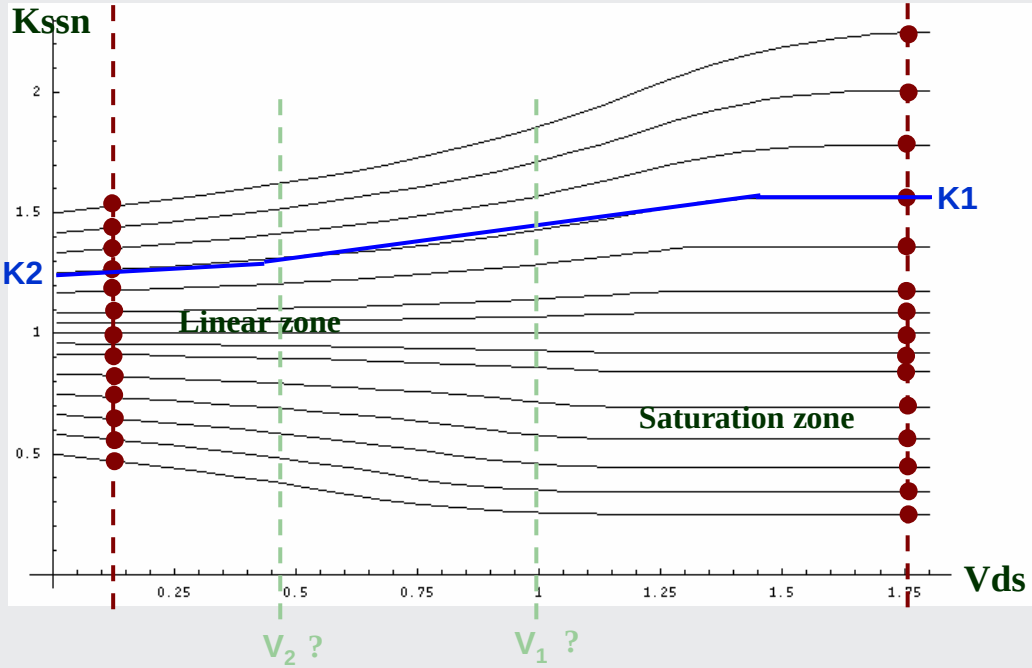
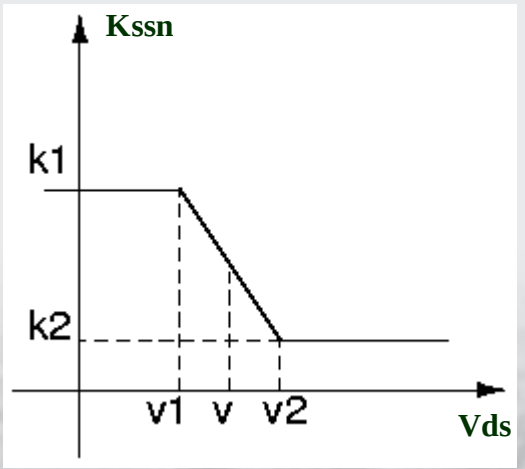


Table 1



To improve Vgs modulation accuracy in the linear zone, a solution with two Kssn coefficients for both pullup and pulldown stages, is under investigation.

- K_1 and K_2 coefficients are extracted in the saturation and linear zone, respectively
- V_1 and V_2 threshold voltages delimitate the interpolation zone
- the best choice of V_1 and V_2 has not yet been identified
- the increase of computational time and IBIS-AMS simulation's speed has to be evaluate

Conclusions

- Actually the IBIS Simultaneous switching output simulations are not accurate
- A power network model back-annotation and a “Gate modulation effect” implementation are needed
- RC model for power network is a rough solution but enough accurate
- Two modulation coefficients, based on table format, seem the best trade-off between accuracy and computational time effort for describing the “Gate modulation effect”
- At the moment, the most flexible way to implement the modulation coefficients is to extend the IBIS description by VHDL-AMS language
- The “Gate Modulation Effect” algorithm might be suggested to CAD vendors and implemented in the EDA tools which manage IBIS models
- A solution with two Kssn coefficients, for both pullup and pulldown stages, is under investigation.