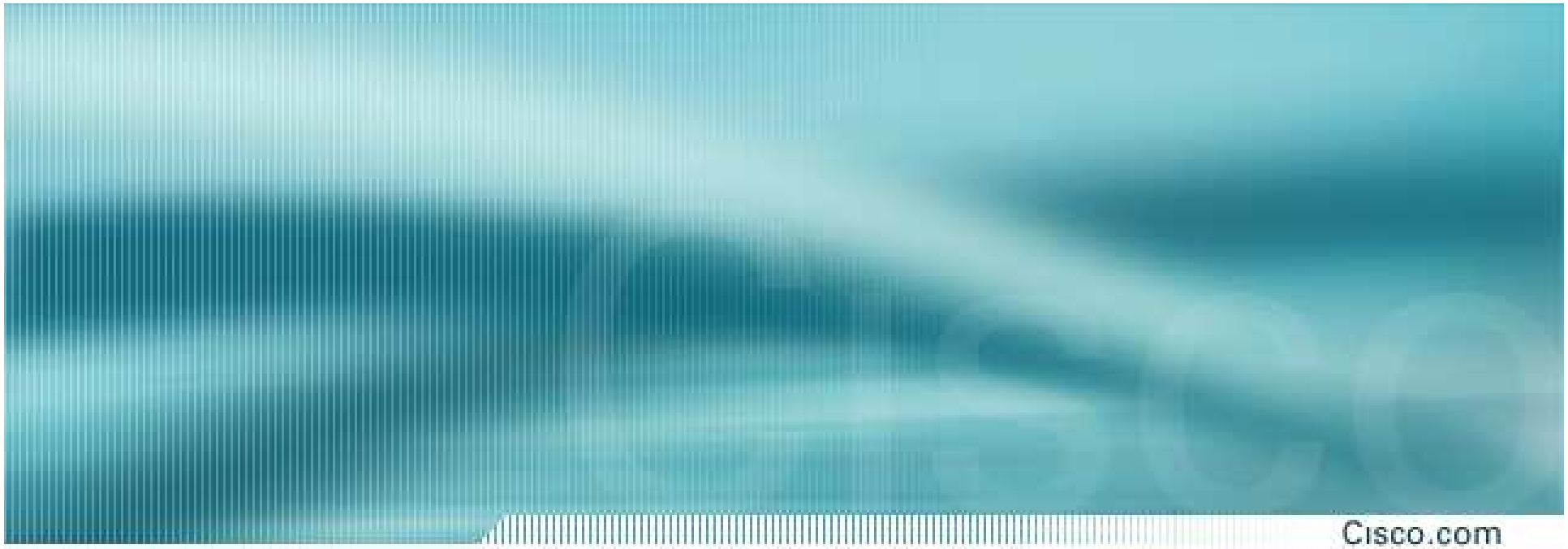

Why the ground parasitic should be removed for high-speed simulation correlations between HSPICE and IBIS model

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IBIS cookbook/future meeting on 8/30/05

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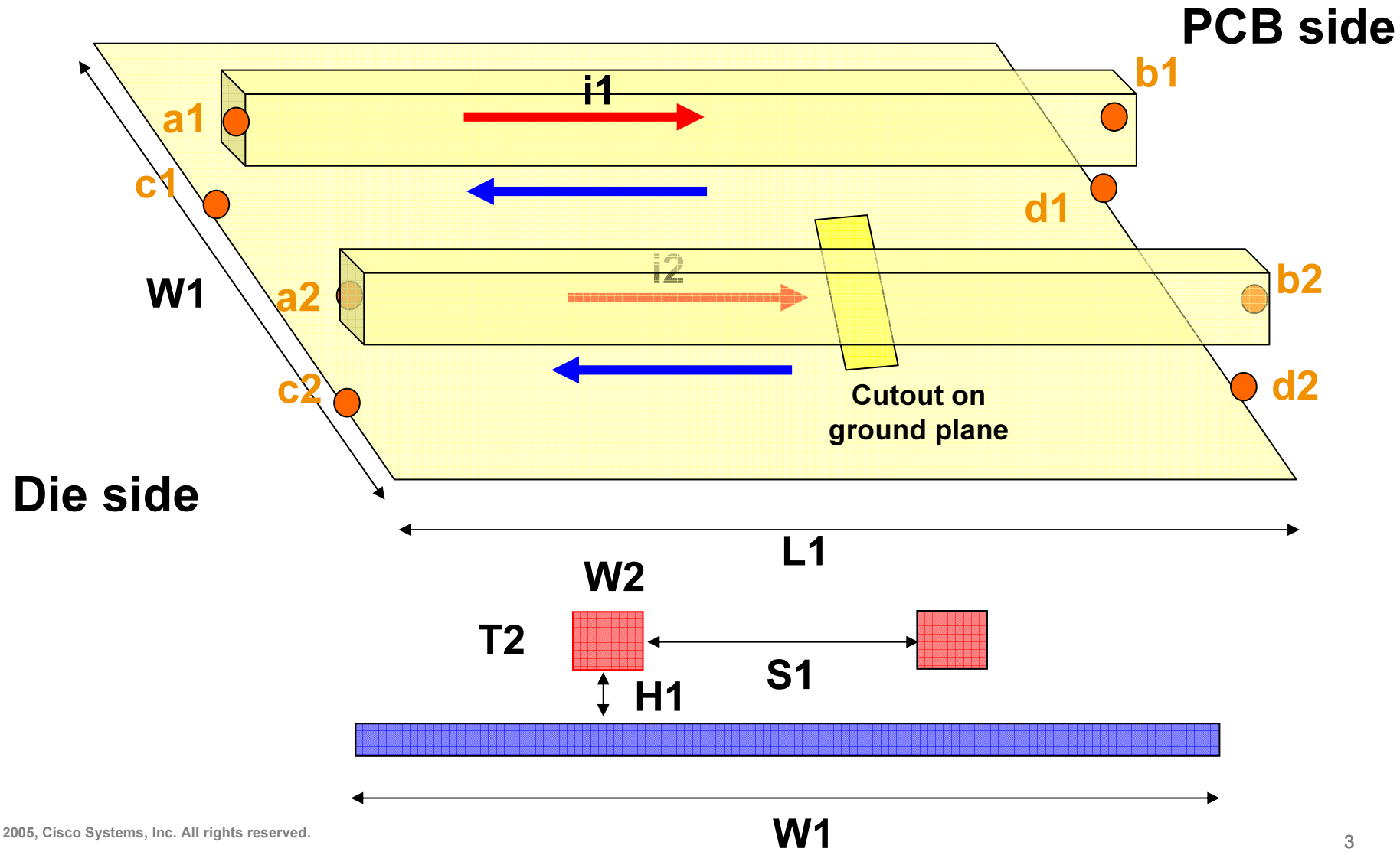
Content

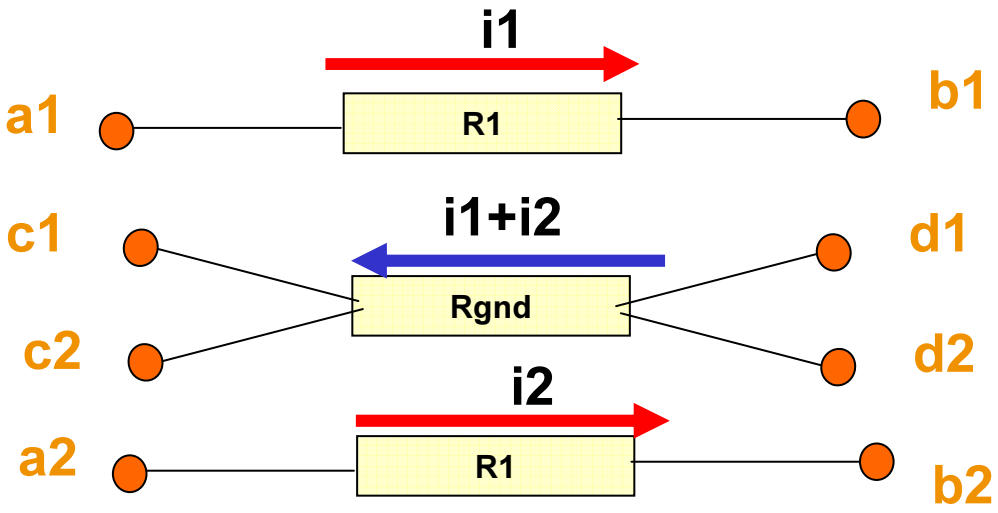
- Reason #1: ground parasitic is not needed for high-speed circuit modeling. It could easily cause more problems than solve problem.
- Where did the ground parasitic come from?
- How is the misconception of ground parasitic broken at high frequency?
- The best and simplest high-speed model for is no parasitic on ground net.
- Reason #2: current IBIS is a three-terminal device, so it can not correlate transistor-level Spice model well when the transistor-model has more than 3 terminals carrying current and the ground net is not ideal.

Where did the misconception of ground parasitic come from?



Extracted circuit model at very low frequency

Die side

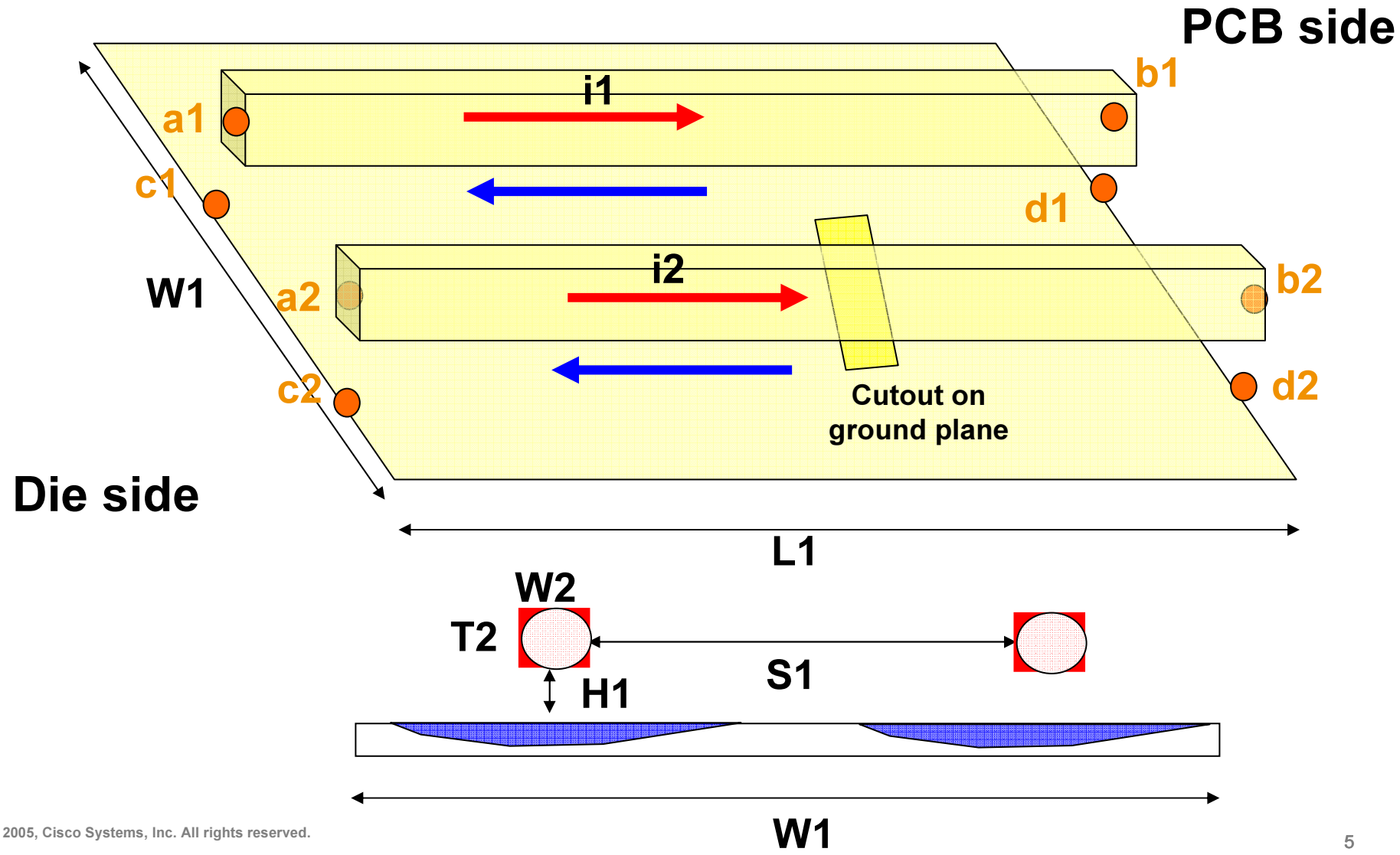


PCB side

Good things about this model:

1. It is valid at very long frequency at which current is evenly distributed across the ground plane and c1/c2 & d1/d2 have the same voltage potential.
2. You can actually probe the voltage across any two points in this circuit and it is meaningful and could match the measured data very well, so ground bounce (voltage difference between c1/c2 and d1/d2) is well defined.

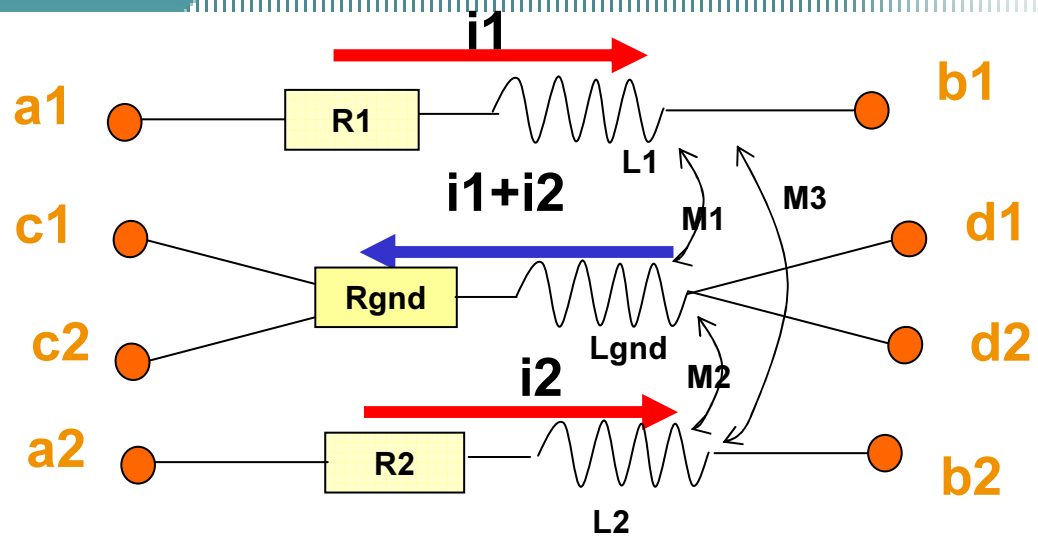
Same structure at high-frequency



How is the low-frequency model broken at high frequency?

- At high-frequency, when wave length is close to the structure size, (such as L in the above figure). The voltage is not well defined between die ground and PCB ground.
- It is clearly shown that the return current for conductor 1 and 2 are not the same. For this reason, it is impossible to have same partial parasitic for two different return paths.

The circuit model with parasitic on ground net

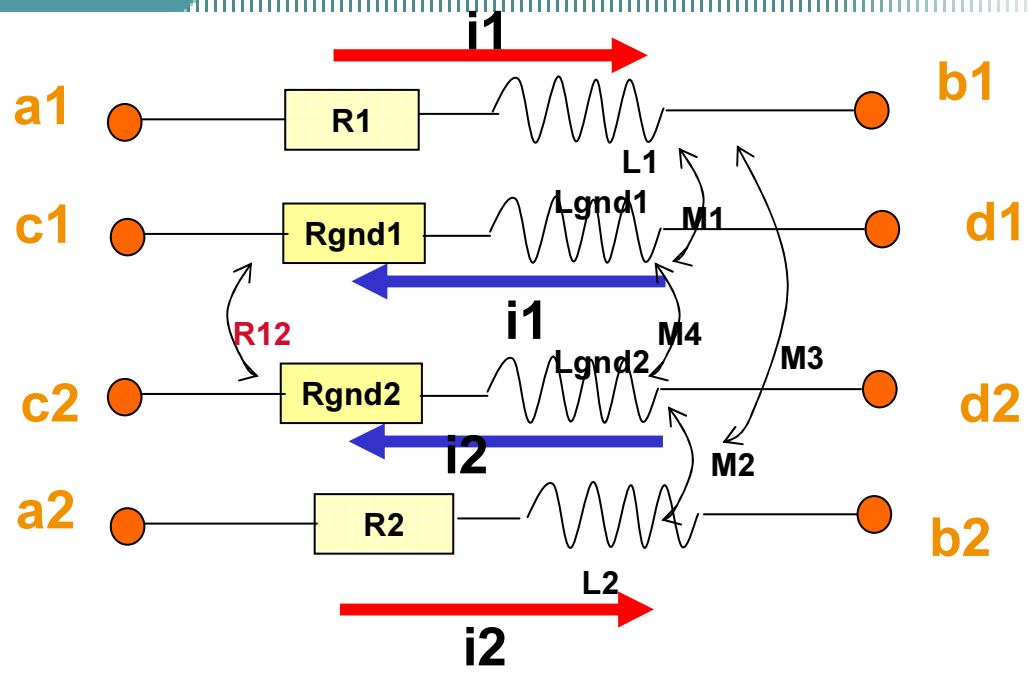


Problems with the above model:

1. **Return current i1 and i2 does not share the common path, how the Rgnd and Lgnd can be well defined?**
2. **How to separate the L1, Lgnd and M1 from the physical loop inductance? No unique definition for L1, Lgnd and M1.**
3. **Local reference voltage definition is the only meaningful voltage at high frequency. For example, Va1_c1, Vb1_d1, Va2_c2 and Vb2_d2 are the only meaningful voltages in above figure. The ground bounce (Vc1_d1 or Vc2_d2) is not well defined and meaningless. You may still probe this voltage in the lab, but the distance between right side and left side cause unwanted probe loop.**

A better model

Die side

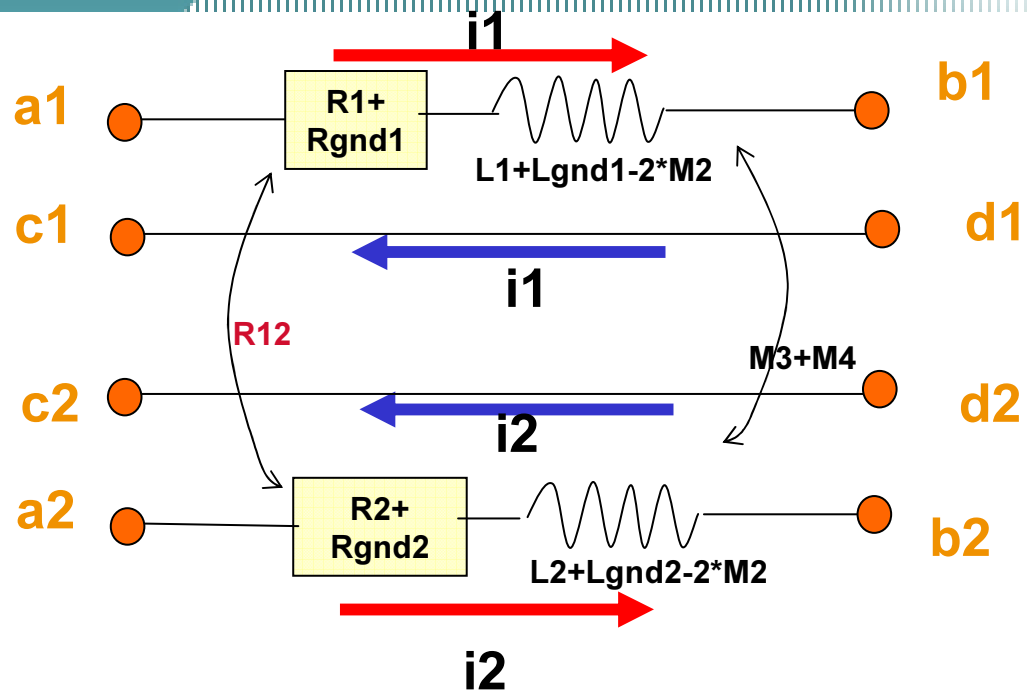


PCB side

Compared with previous model, the above is a much better and accurate model. The only drawback is too many components, especially partial and mutual inductances, and these inductances is not well defined. Since we only care about the voltage with local reference, this model can be further simplified by model reduction.

A Simplified model

Die side



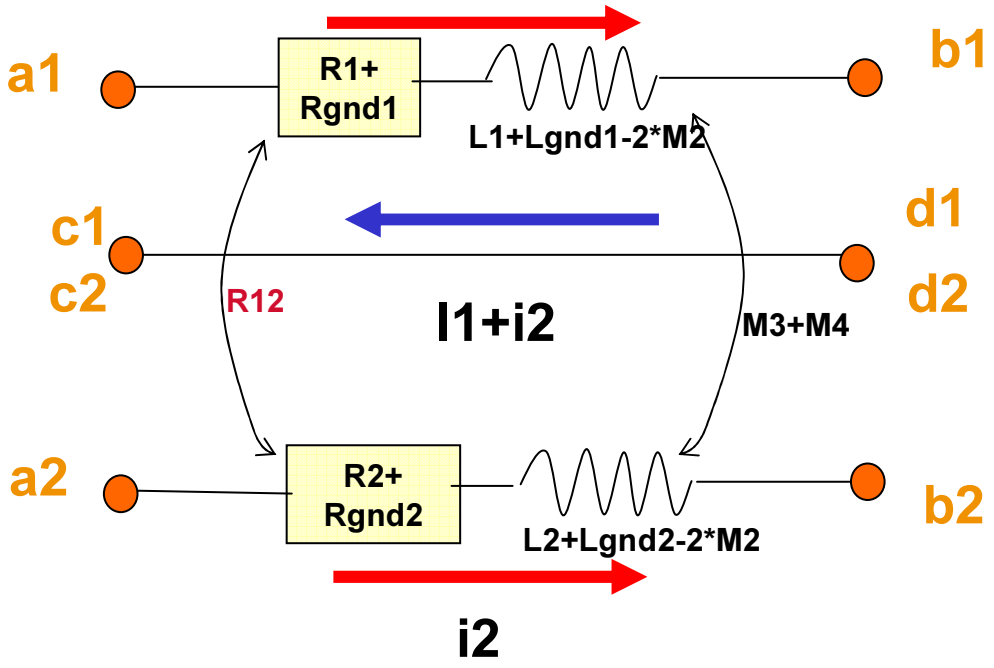
PCB side

This model is much simple and it is accurate from DC to very high-frequency. All components in this circuit are well defined and have unique physical meanings.

The ground nodes c1/c2/d1/d2 could shorted together (by doing so, it losses the mapping between physical locations and circuit nodes.

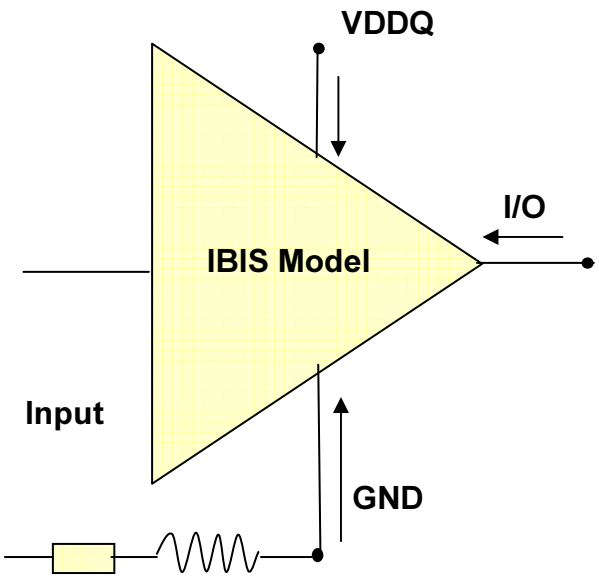
A model without ground parasitic is better

Die side

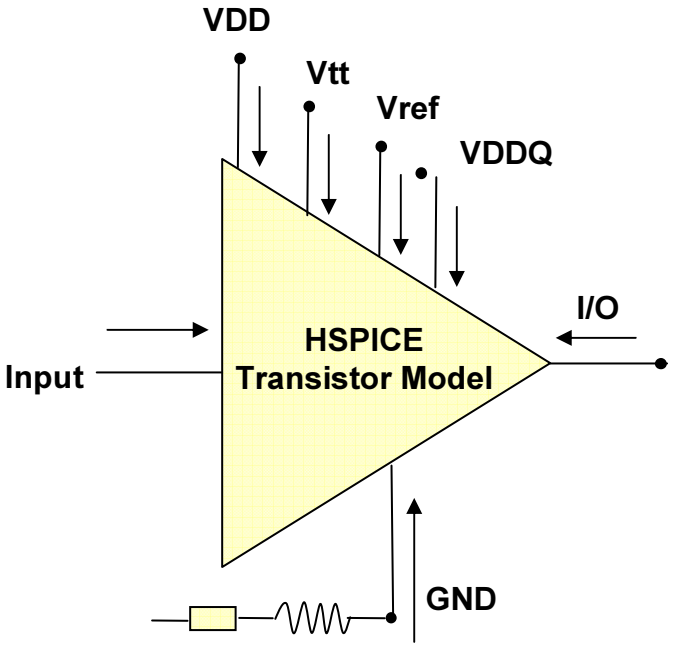


PCB side

Reason #2



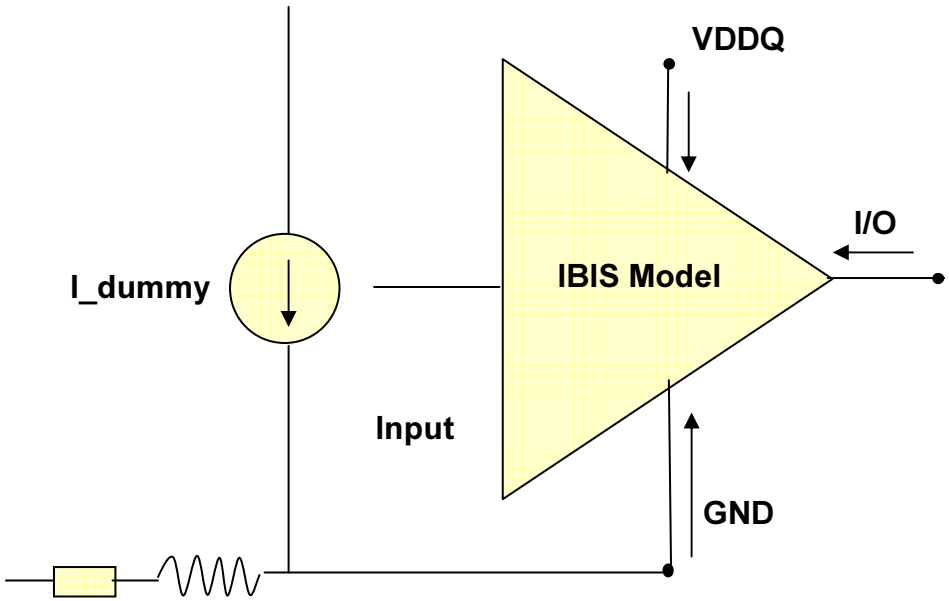
I_vddq+I_gnd+I_i/o=0



I_vddq+I_gnd+I_i/o+I_vdd+I_vtt_Ivref+I_input=0

*** BIRD95 only defined the total current through VDDQ node. The current flow through ground node is constrained by KCL. It should work fine if there is no ground parasitic. In the future, if IBIS would like to expand to support nonideal ground circuit model. A IvsT table for ground pin could be included.**

Possible solution for future IBIS



I_dummy=I_vdd+I_vref+I_vtt+I_input+I_misc

Q&A