Issues with C_comp and Differential Multi-stage IBIS Models

Michael Mirmak
Intel Corporation

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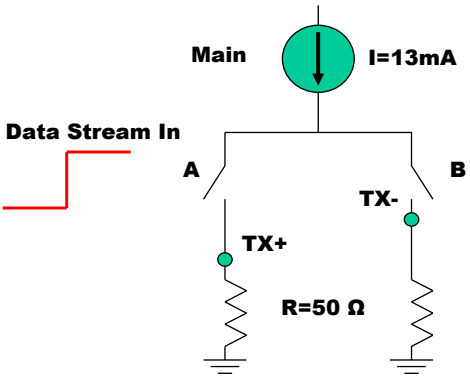
Agenda

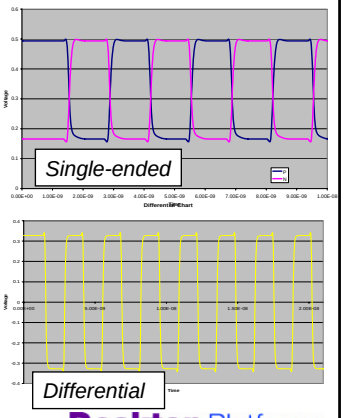
- Background
  - Typical serial/diff. interface buffer design
  - How Pre-emphasis is addressed in IBIS
- Initial Approach to C_comp
  - How tools use C_comp
  - Proportional splitting
  - Over-estimation of buffer loading
- New Approach
  - "Backing Out" C_comp
  - Adding external capacitance
  - Combined V-t correlation
  - Multi-variate c_comp
- Guidelines and Future Work

Typical Ser/Diff TX Design

- Single stage buffer
  - Example shown in S-ATA Gen. I specification
  - http://www.serialata.org

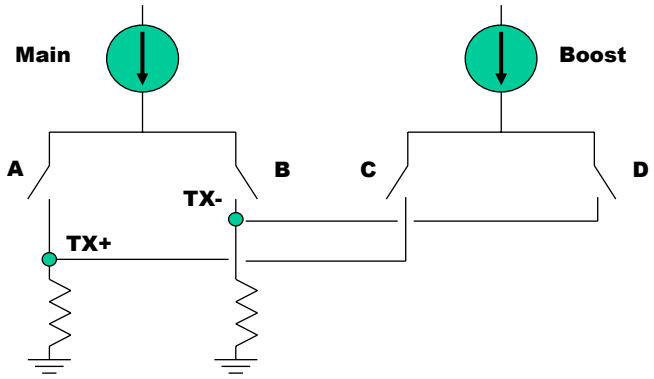


Output
(into 100 Ω load)



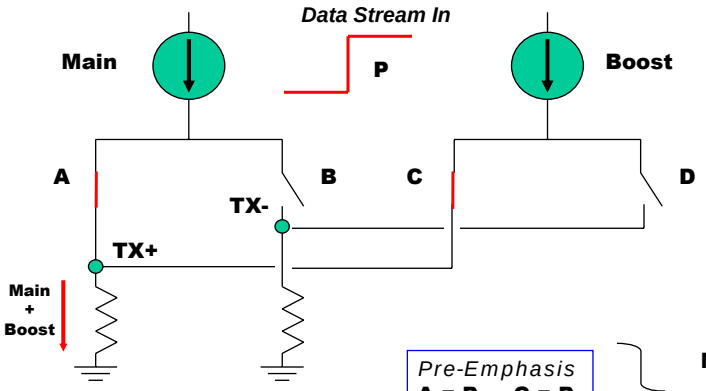
Adding Pre-emphasis

- Another source with different stimulus
  - Second source usually a fraction of the first



Adding Pre-emphasis

- Another source with different stimulus



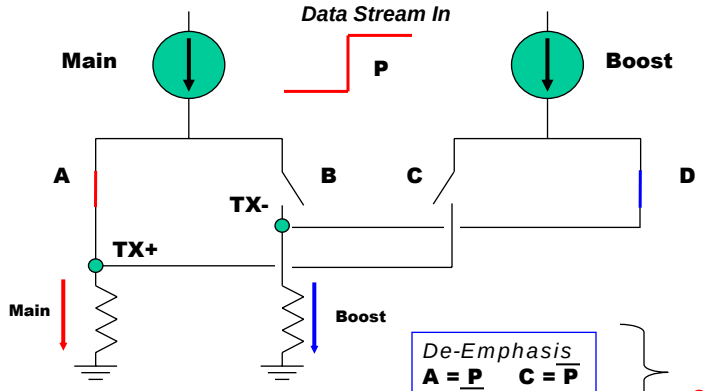
Load between TX+ & TX- sees *Main + Boost*

Pre-Emphasis
A = $\overline{P}$ C = P
B = $\overline{P}$ D = $\overline{P}$

Main & Boost in concert

Adding Pre-emphasis

- Another source with different stimulus



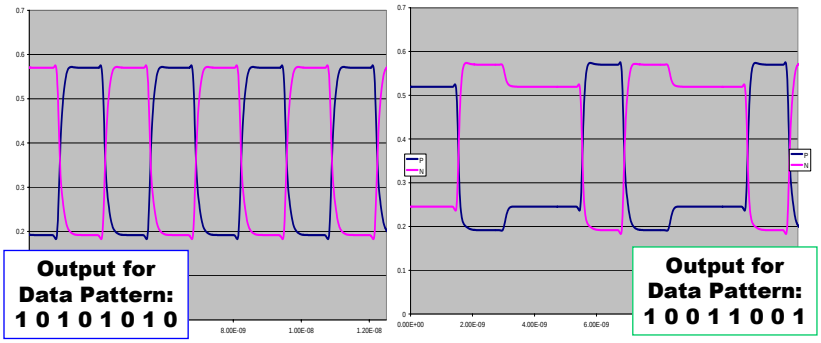
Load between TX+ & TX- sees *Main - Boost*

De-Emphasis
A = P C = $\overline{P}$
B = $\overline{P}$ D = P

Main & Boost opposing

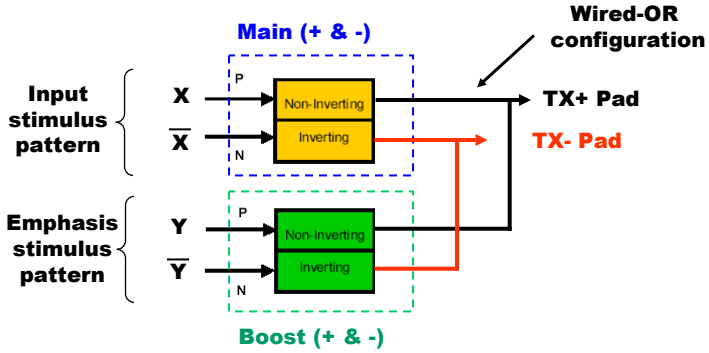
Pre-emphasis Output

- Typical implementation
  - 1 Bit = Crossover to Crossover
  - Each bit after a crossover is emphasized
  - Compensates for ISI and other loss effects



IBIS Implementation

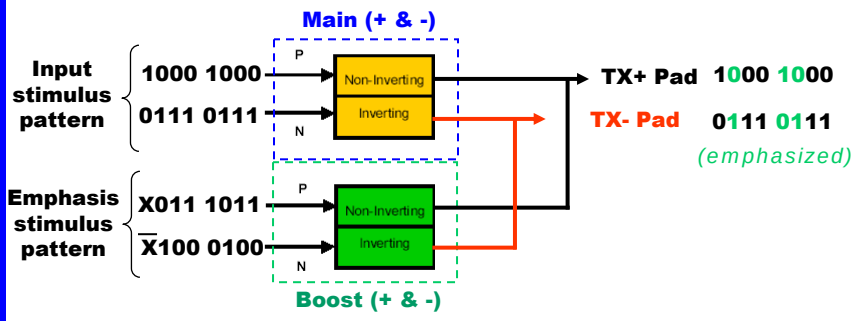
- In IBIS, two differential pairs are combined
  - One differential pair represents the main
  - One differential pair represents the boost
- Each pair has a distinct stimulus pattern
  - Main pair driven by the desired output pattern
  - Emphasis pair driven by different data pattern



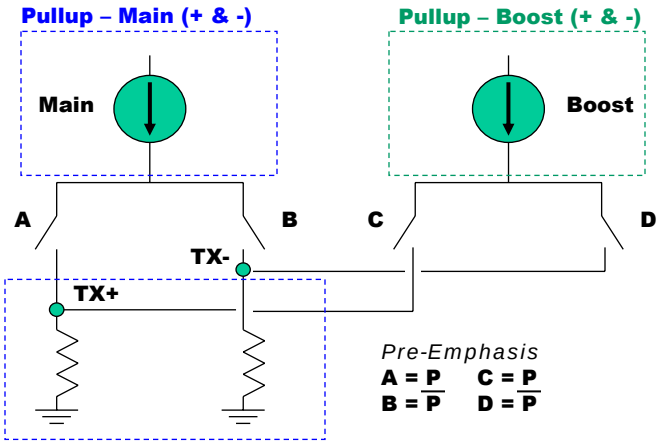
IBIS Implementation

- What is the emphasis pair's stimulus pattern?
  - If only transition bits are emphasized…
  - *Emphasis bit = inverse of input bit, delayed by 1 bit time*
  - Logical proof has 20+ steps
  - Fairly simple to demonstrate empirically

Emphasis (t) = $\overline{\text{Input (t-1)}}$



IBIS Grouping



Pre-Emphasis
A = P C = P
B = $\overline{P}$ D = $\overline{P}$

De-Emphasis
A = P C = $\overline{P}$
B = $\overline{P}$ D = P

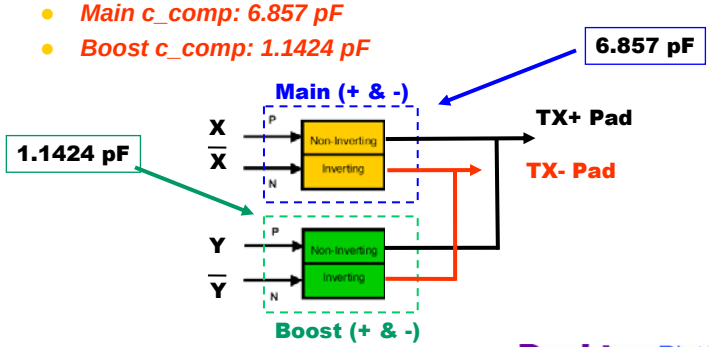
Ground Clamps
Main + & -

IBIS Data Extraction

- As pre-emphasis uses two buffers…
  - I-V curves are individual to each buffer
    - *Main I-V & Boost I-V are separately generated*
    - *Internal terminations should NOT be double-counted!*
  - V-t curves are individual to each buffer
    - *Main V-t & Boost V-t are separately generated*
    - *Internal terminations should NOT be double-counted!*
- ***Good designs will have test modes for disabling the sources and the terminations***
- ***What about c_comp?***
  - C_comp is collected only once, for entire buffer
  - "Turning off" sections will not remove loading effects
  - Most designs cannot be easily "split" into main and boost for purposes of c_comp measurement

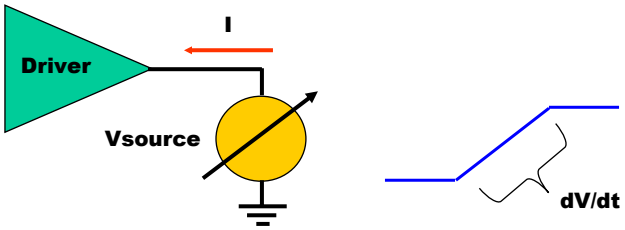
Two Approaches to C_comp

- Method 1: split c_comp proportionally to Main and Boost relative drive strengths
  - Example: "Buffer X" has total die capacitance of 8 pF
    - *See below for calculation*
  - *Main is 18 mA*
  - *Boost is 3 mA (6:1 ratio)*
  - *Main c_comp: 6.857 pF*
  - *Boost c_comp: 1.1424 pF*



How was C_comp generated?

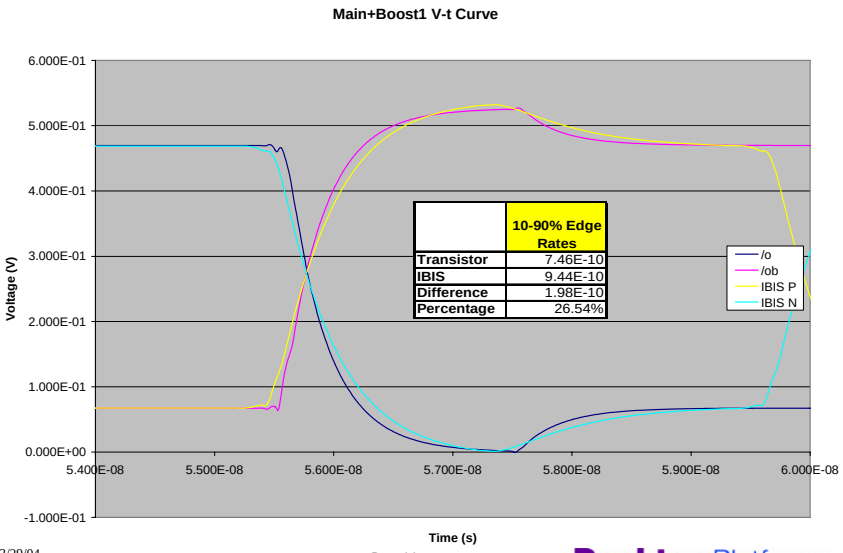
- Initial method used to get 8 pF value



1. Use Vsource with known edge rate, dV/dt
2. Measure the input current
3. Calculate capacitance (may have to take an average)

$$I = C * \frac{dV}{dt} \quad \rightarrow \quad C = \frac{I}{(\frac{dV}{dt})}$$

Results of Method 1 on Buffer X



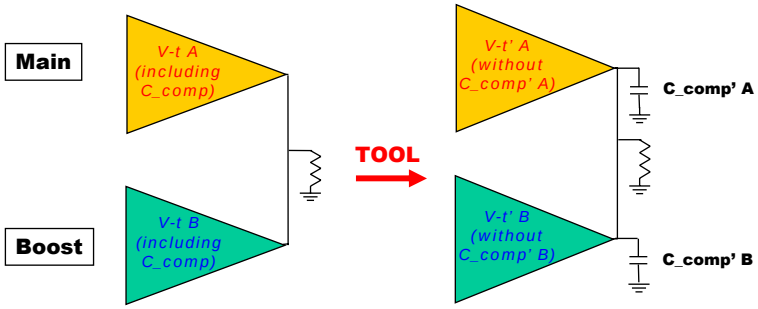
	10-90% Edge Rates
Transistor	7.46E-10
IBIS	9.44E-10
Difference	1.98E-10
Percentage	26.54%

The Problem

- IBIS is 27% slower than the transistor model!
  - *Same Main V-t curve as transistor model*
  - *Same Boost V-t curve as transistor model*
  - *I-V curves match to within 1%*
  - *Die capacitance (C_comp) is only area of change...*
- Question: How is C_comp treated by EDA tools?
  - IBIS V-t curves include C_comp effects
  - C_comp also affects incoming (and reflected) waves
  - Tools therefore remove C_comp effects from V-t curves
    - *Cap with C_comp value is placed external to buffer*
    - *"Cap-less" V-t curves are used for driving simulations*
    - *Output waveform at pad should be equivalent to IBIS*

The Problem with Method 1

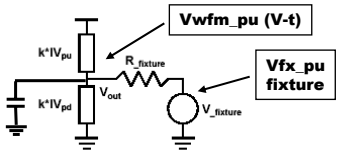
- For Pre-Emphasis, tool approach breaks down…



- Assuming…
  - C_comp (transistor) = C_comp' A + C_comp' B
- When Buffer A drives with adjusted curves…
  - A sees its own cap load PLUS the load at Buffer B
  - A's V-t curves were only adjusted for C_comp' A!
  - *Equivalent output edge rate will be too slow!*

Proposed Fix

- Method 2: Adjust all V-t curves for the total C_comp value before using the models for simulation
  - *Each V-t curve reflects total C_comp load*
  - *Adjust each curve (Main, Boost) for total C_comp*
  - *Set IBIS C_comp for Main, Boost to 0 pF*
  - *Add external cap equal to original total C_comp*



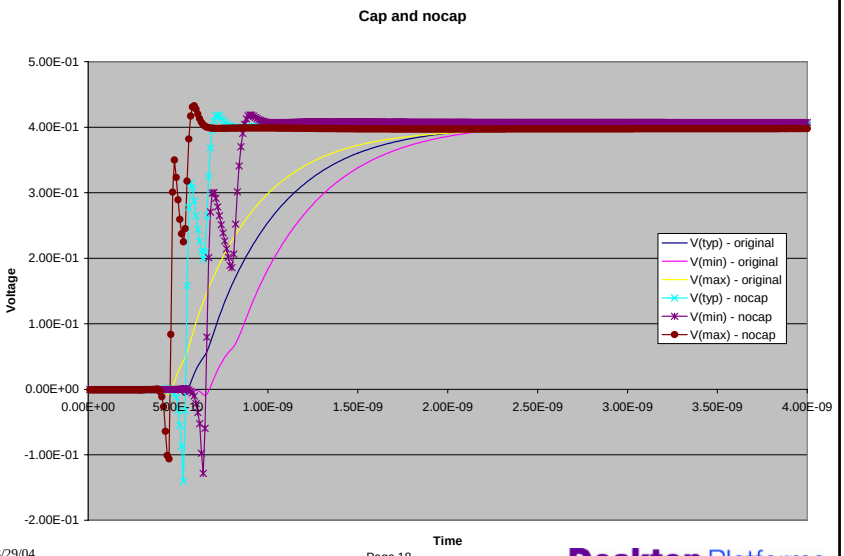
Current through fixture is function of current through pullup AND through die cap

```
Ifx1 := ((Vwfm_pu(index) - Vfx_pu) / Rfx_pu) + C_comp * dVwfm_pu(index);
Ifx2 := ((Vfx_pd - Vwfm_pd(index)) / Rfx_pd) - C_comp * dVwfm_pd(index);
```

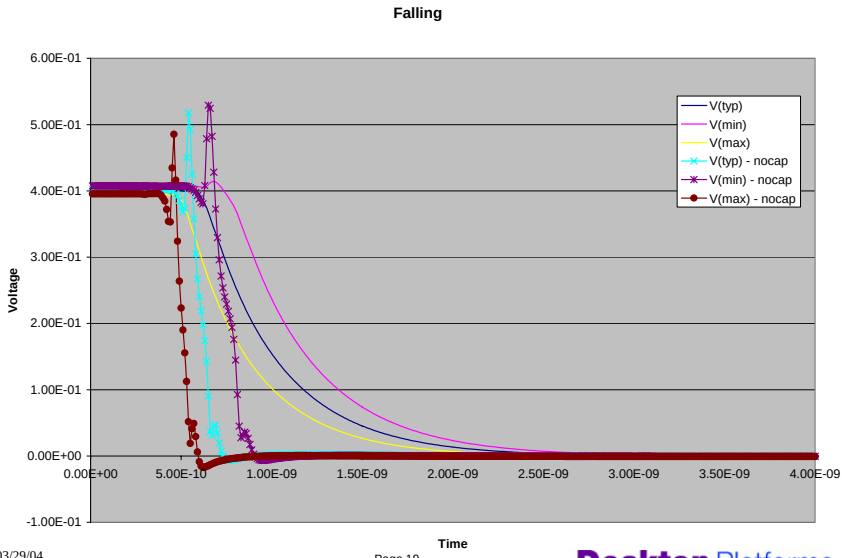
C_comp compensation

images and equations from A. Muranyi

Extraction – Main Rising



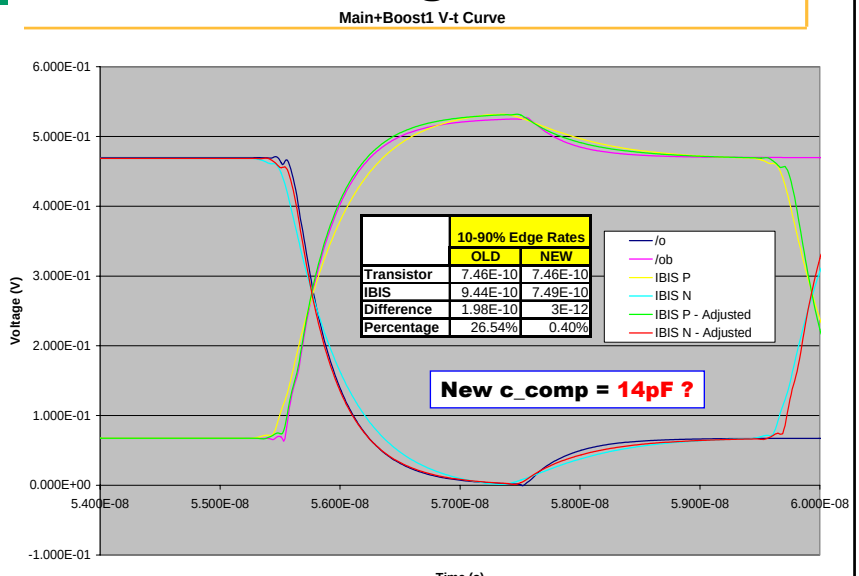
Extraction – Main Falling



Steps & Notable Features

- New curves should be much sharper
  - *I-V setting point should be the same*
- Non-monotonic "bumps"?
  - C_comp does not differentiate between sources of capacitance
  - Possibly due to Miller cap effects
- Adjustment Procedure Details
  1. Start with V_{load}-t curve (IBIS V-t curve)
  2. Use R_{load} to calculate I_{load}-t curve (V = IR)
  3. Take derivative of V_{load}-t to get dV_{load}/dt curve
  4. Multiply C_comp by dV_{load}/dt to get I_{cap} (I = C*dV/dt)
  5. Subtract I_{cap} from I_{load} to get I_{adj} (watch signs!)
  6. Multiply I_{adj} * R_{load} to get V_{adj}-t curve
     - *Easily done in Microsoft Excel**
  7. Add C_comp external to buffers in simulation

Results of Using New Method



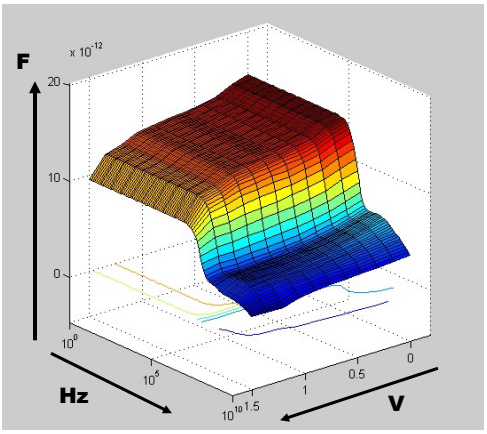
	10-90% Edge Rates	
	OLD	NEW
Transistor	7.46E-10	7.46E-10
IBIS	9.44E-10	7.49E-10
Difference	1.98E-10	3E-12
Percentage	26.54%	0.40%

Comments

- Matching
  - *IBIS edge rate now < 0.5% match to transistor edge rate*
- Issues
  - *Peak voltage & settling still not matching transistor*
  - *Match only good for 1100 pattern*
    - *IBIS lacks ISI coupling to current sources*
    - *Matching to other patterns not yet studied*
  - *Needed to add 14 pF externally, not 8 pF, to match edges*
    - *Recall: C_comp is added external to adjusted buffers*
    - *Transistor and IBIS edge rates only matched with 14 pF*
    - *What explains discrepancy?*
      - *Under investigation (see below)…*

A Further Complication

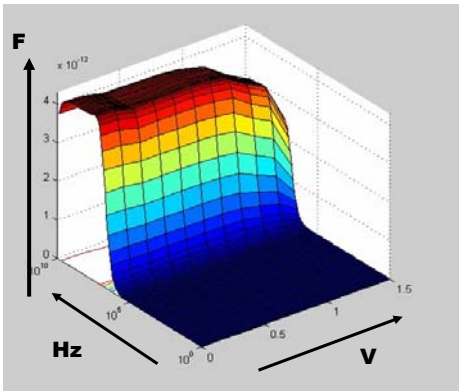
- Transistor model capacitance behaviors are not simple
  - Capacitance for "Buffer X" vs. Frequency and bias V
  - Frequency-based measurement *not* constant 8 pF



Recall A. Muranyi's analyses:
"Details on True Differential Buffer Characterization Revisited"
October, 2003

A Further Complication

- Differential view of transistor model capacitance
  - Differential capacitance not included in adjusted model
  - Note that finding of femto-farad differential capacitances described in previous summits may not always apply!



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Guidelines and Future Work

- Collect three types of V-t curves from source
  - Main-only V-t
  - Boost-only V-t
  - 1100 correlation curve from full model
    - *Combination of main and boost, at pad with R load*
    - *Pre- and de-emphasis behaviors will be shown*
    - *Other data patterns may yield different results!*
- Use equations to "back out" c_comp
  - Adjust external capacitance to match 1100 correlation curve
  - Measurement method used for c_comp could make a difference!
- Alternatives for investigation
  - Equation-based capacitance, for example: C(V,f)
    - *Would require collecting additional data from source*
    - *Very possible under IBIS 4.1*
    - *"Backing out" c_comp from Main, Boost is non-trivial*
  - Driver Schedule
    - *Check sim tool implementation of c_comp adjustment*
    - *V-t curve adjustment may still be needed before simulations*