SIGRITY

# *Adding On-Chip Capacitance in IBIS Format for SSO Simulation*

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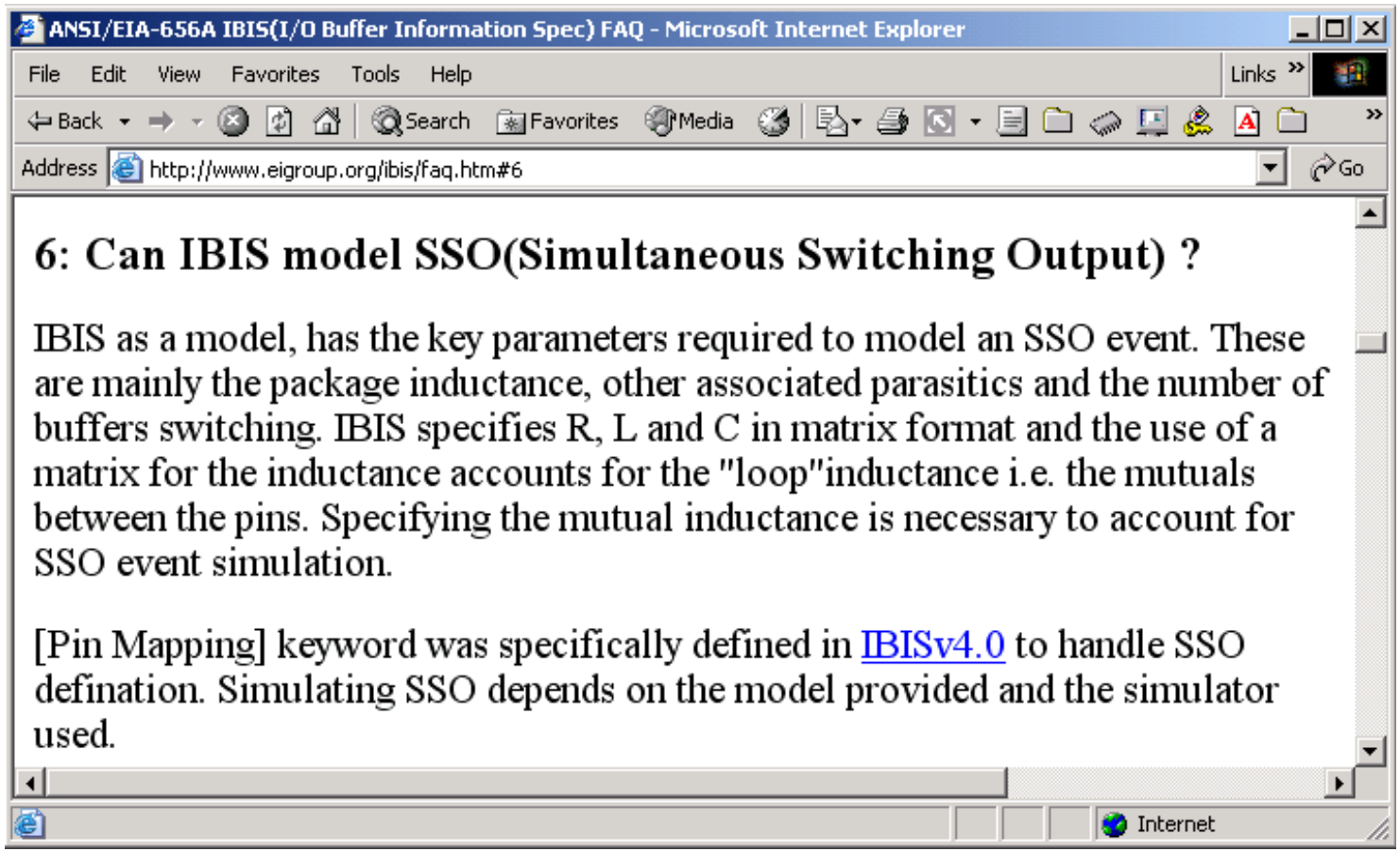
# Agenda

1. Is IBIS good for SSO simulation
2. SSO simulation flow using IBIS
3. Improve SSO simulation accuracy by adding Cdie for on-chip power/ground parasitics
4. Further discussion

# Can IBIS Model SSO (From Official IBIS FAQ)



# Examine IBIS Model of Device, IC Package and PCB for SSO Simulation

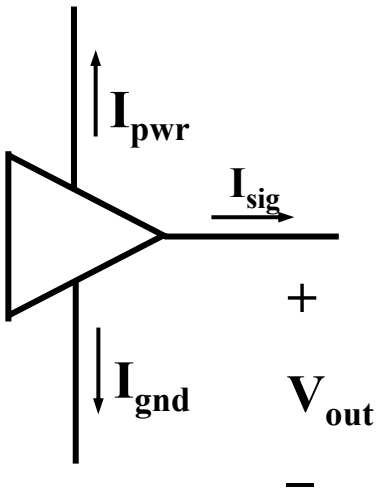
- Lumped IC package model and PCB model (EBD) in an IBIS file are for rough SSO estimation since semiconductor company usually will not give out details on their package and modules. For real world high speed system design, geometry based EM field solvers are must for package + PCB system level simulation including SSO.

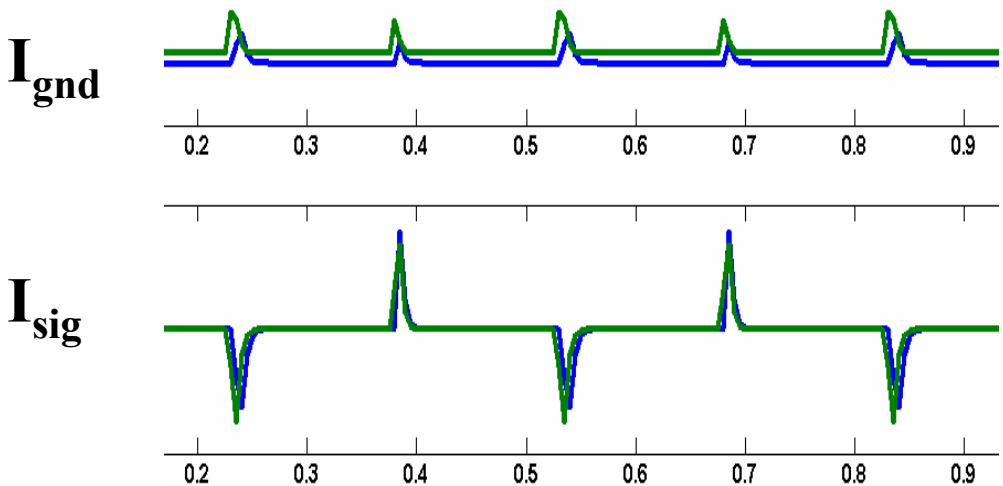
- IBIS is developed for device modeling, as a behavioral model, it can be used for, and actually is good for SSO simulation, provided if a few IBIS parameters can correlate well with original SPICE transistor model (next slide).

- SSO simulation must include many non-linear devices in one simulation run. IBIS has the natural speed advantage over SPICE transistor level model, therefore, SSO is a very good Signal Integrity (SI) application for IBIS.

# Examine IBIS for Device Model in SSO Simulation

- The pull-up and pull-down currents of an IBIS model must have the accuracy close to the transistor level model for proper SSO simulation, because most system level noise voltage are due to these currents flowing through the signal and power distribution system.



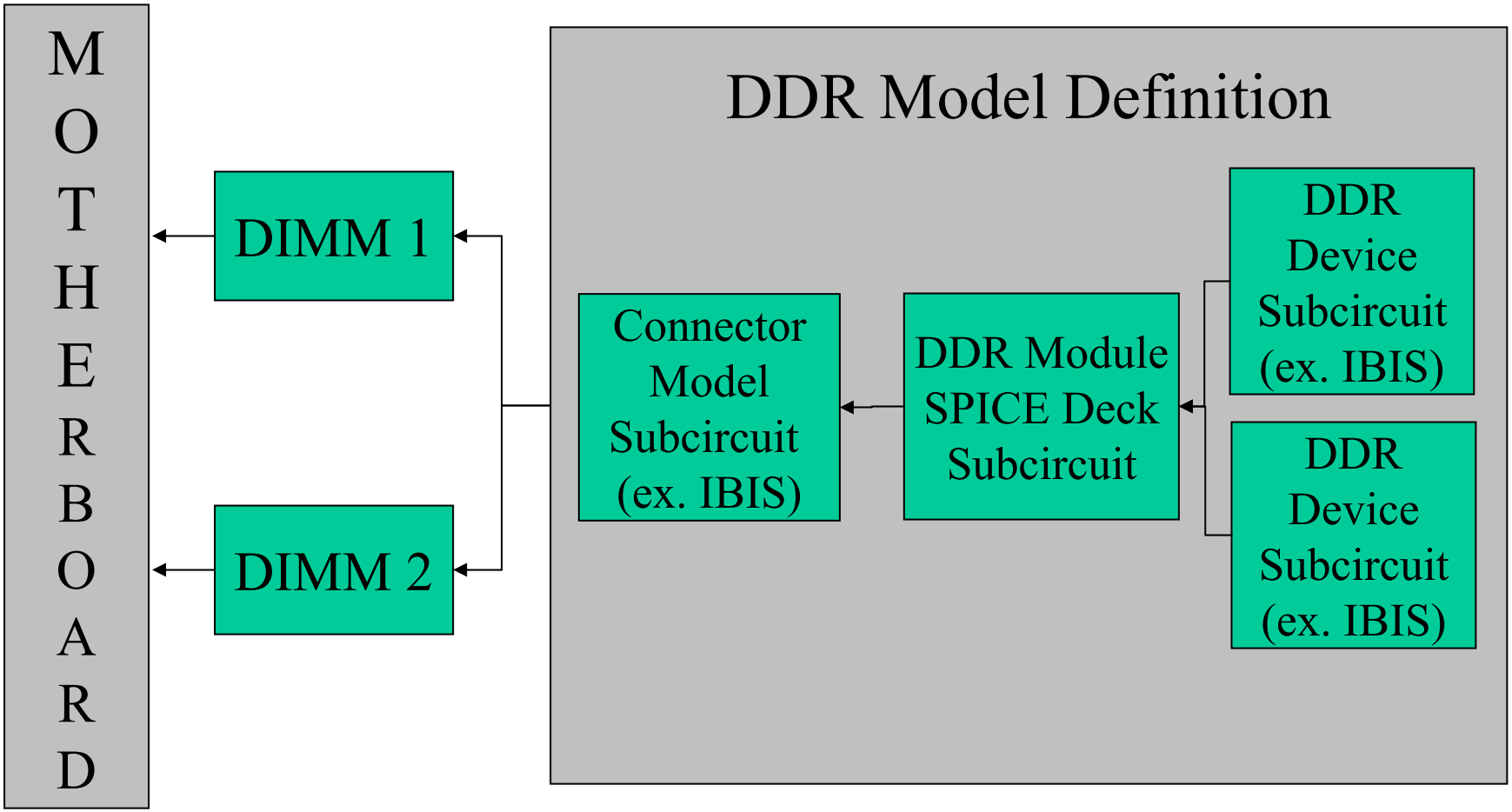




**Blue line: IBIS Green line: Transistor**

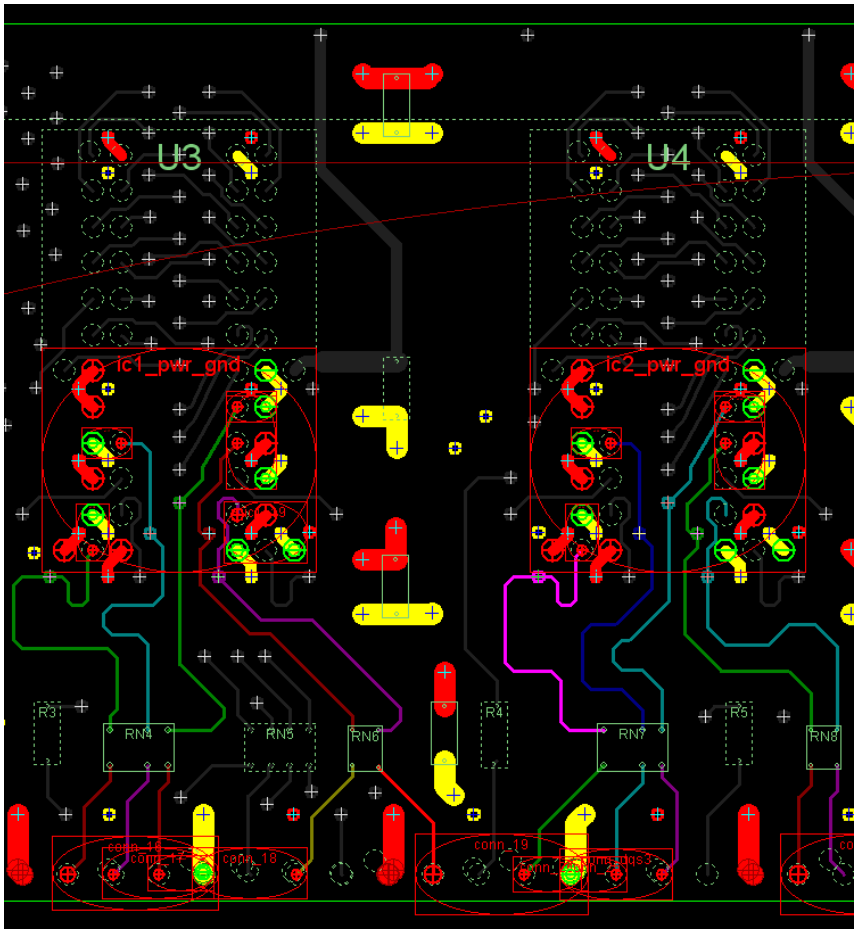
# A Sample SSO Simulation Flow Using IBIS – DDR + Motherboard

- Prepare DDR model in PowerSI
  - Define ports depending on nets of interest
  - Extract S paramter of the DDR module
  - Convert S parameter data to SPICE subcircuit with Broadband Spice
- Prepare Motherboard model in Speed2000
  - Connect voltage sources for +2.5V and Vtt rails; verify capacitor models
  - Connect Northbridge driver models and termination resistors for DDR nets
- Connect the DDR module subcircuit, chip loads, and connector models in Speed2000
- Use Speed2000 to analyze the complete system

# Circuit Linkage Block Diagram



# Prepare DDR Module for Extraction in PowerSI



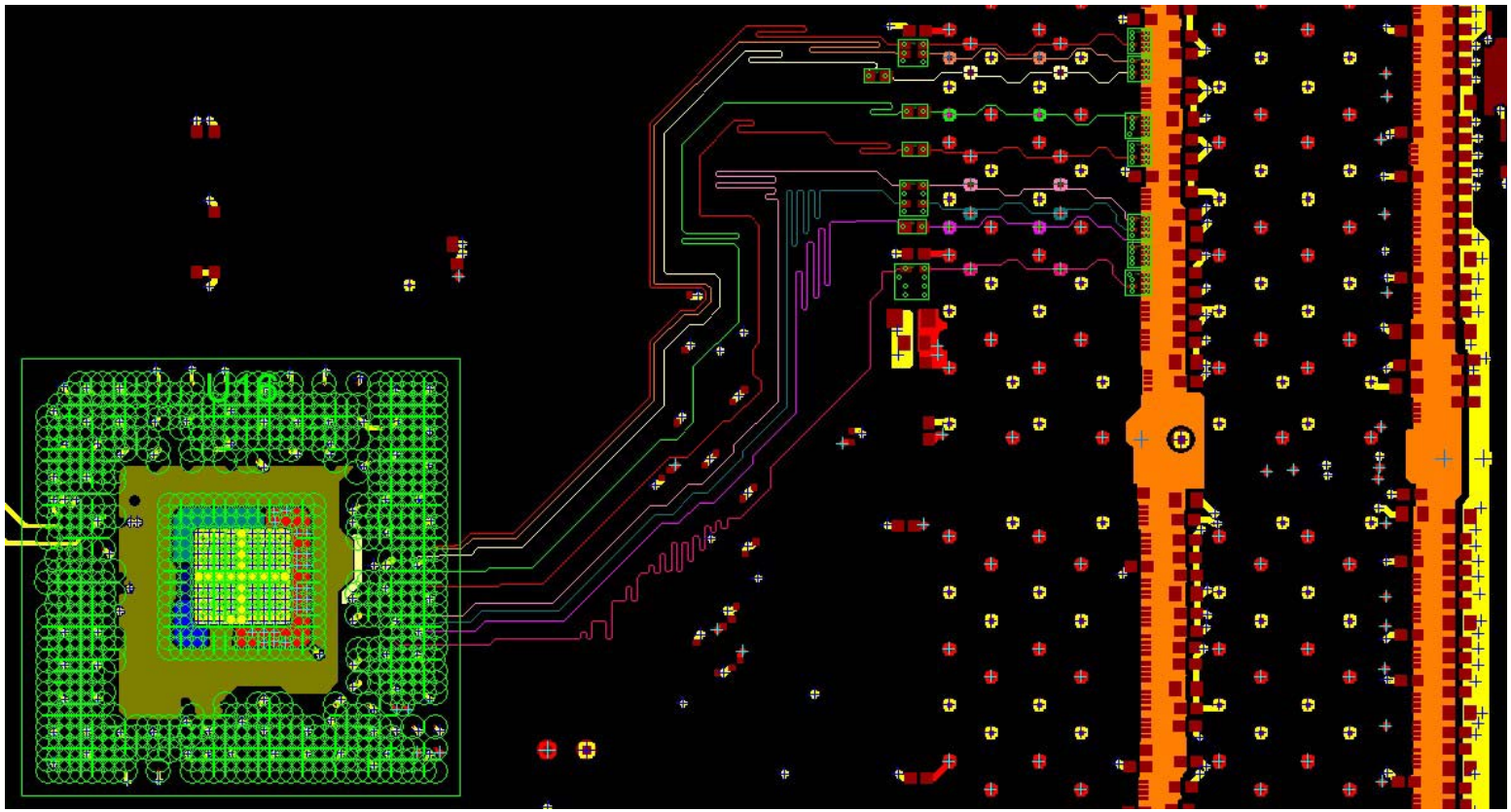

**Read in DDR layout.**

**Define power / ground ports on the top and bottom of the edge connector and at the active devices. Define ports for signals for SSO. For example, DQ16, DQ17, DQ18, DQ19, DQS2, DQ24, DQ25, DQ26, and DQS3. Ports are defined at the edge connector and at the device pins for these signal nets (two ports per signal net).**

**Set the appropriate frequency sweep parameters and extract the S parameter information for the module. Then covert S parameters to SPICE circuit using Broadband SPICE.**

```
.SUBCKT   DDR_module_model
+   n1   n2   n3   n4   n5   n6   n7   n8
+   n9   n10   n11   n12   n13   n14   n15
+   n16   n17   n18   n19   n20   n21   n22   ref
Rd1_1            n23  ref  50.000000
Rd1_2            n24  ref  1
Vd1n1  n23  0
F1   ref  n24  Vd1  1.0
G1   ref  n24  n1  ref      0.02
Rd2_1            n25  ref  50.000000
....
```

# Prepare Motherboard in Speed2000




Connect Northbridge driver and package model for write cycle analysis.

(IBIS model for the drivers are used in this example.)

Verify decoupling capacitors and termination resistor linkages.

Connect voltage sources for +2.5V (yellow) and Vtt (orange) rails.

# Connect the Subcircuits

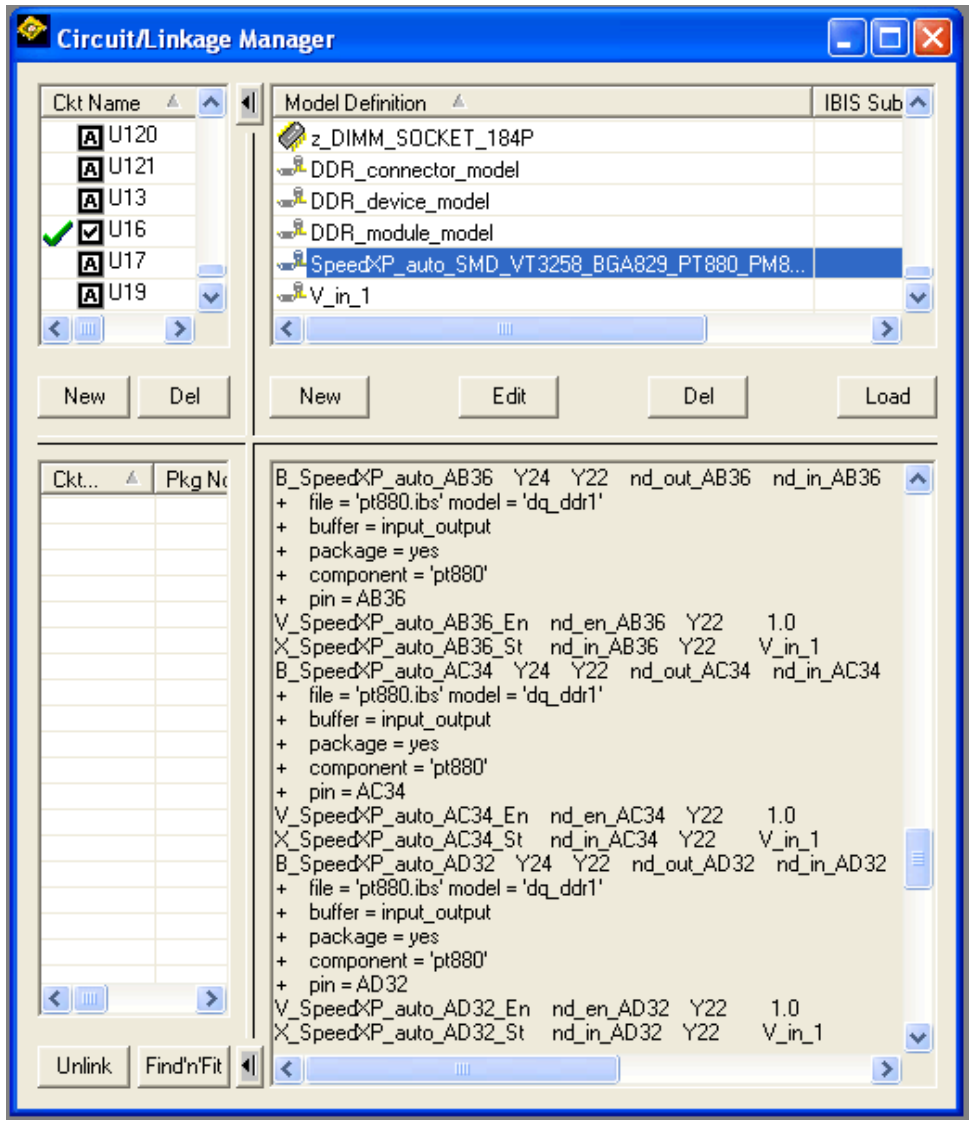
**The automatic IBIS linkage feature was used to connect the Northbridge IBIS drivers.**

**Pin mapping section must be complete before using automatic IBIS connection feature.**

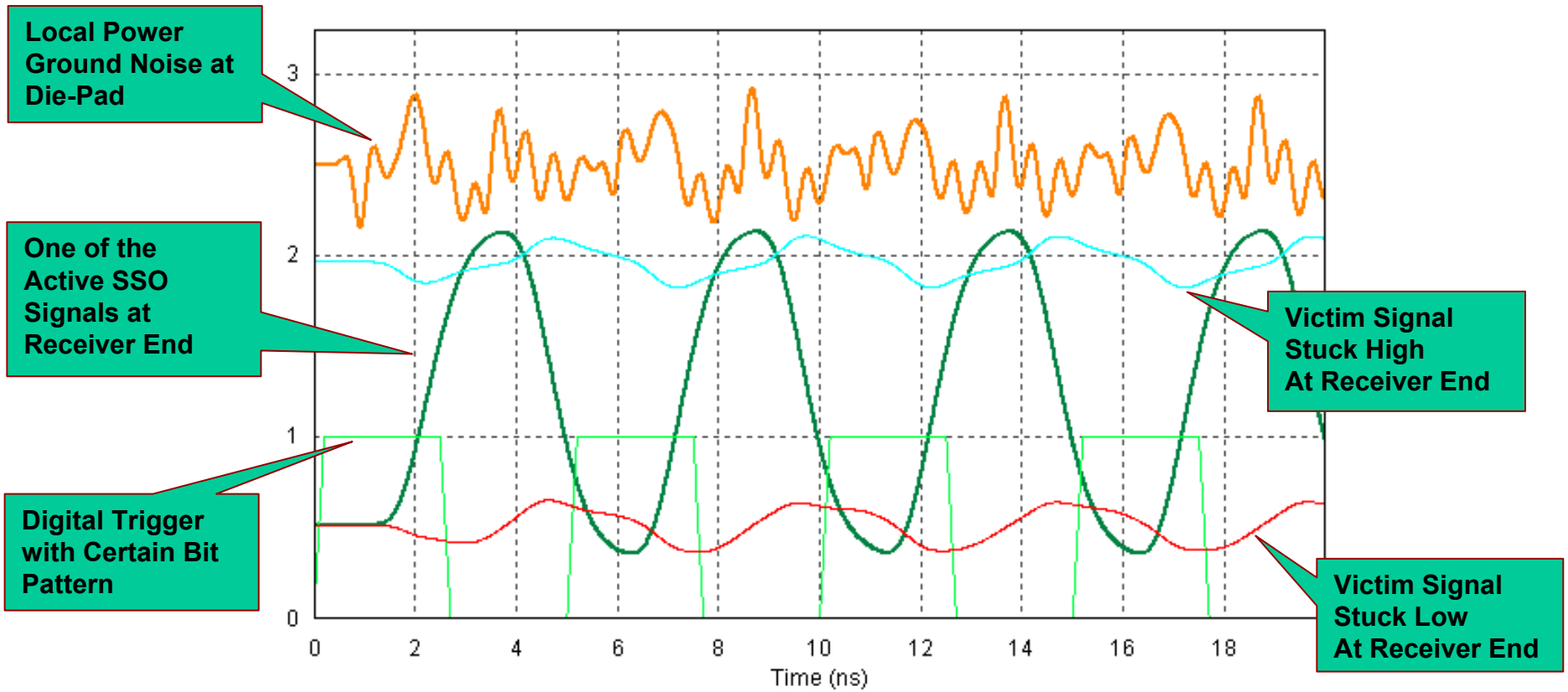
**A few IBIS driver definitions are shown here.**

**With the automatic IBIS feature, numerous SSO simulations are possible: even / odd mode, stuck high, stuck low, and variable number of drivers / aggressors.**

**After the Northbridge driver is defined, add circuit voltage views for all waveforms of interest (receiver waveforms, power / ground bounce, etc.).**

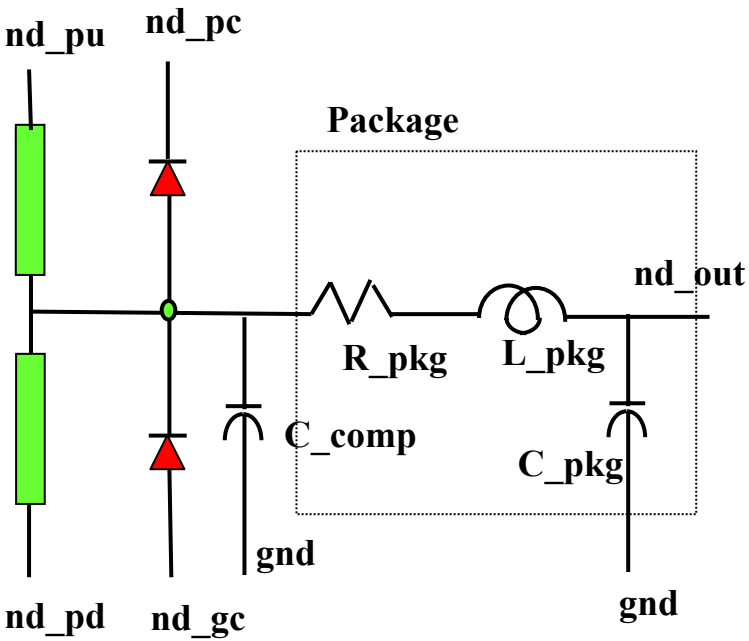


# SSO Simulation Results

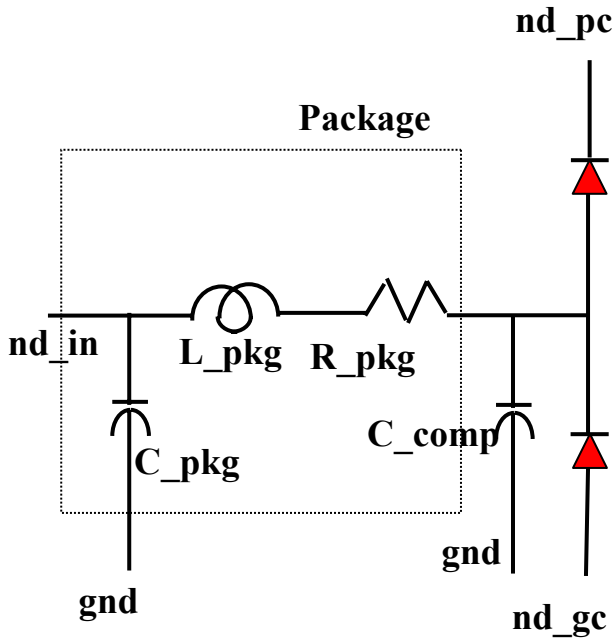


# Why We Need Cdie

1. We have C_comp in IBIS, but we don't have the parasitics between pull-up and pull-down for the on-chip power distribution.
2. Cdie will affect SSO noise at die pad and at system level.
3. Without Cdie, IBIS based SSO results sometimes are more pessimistic than SPICE model.



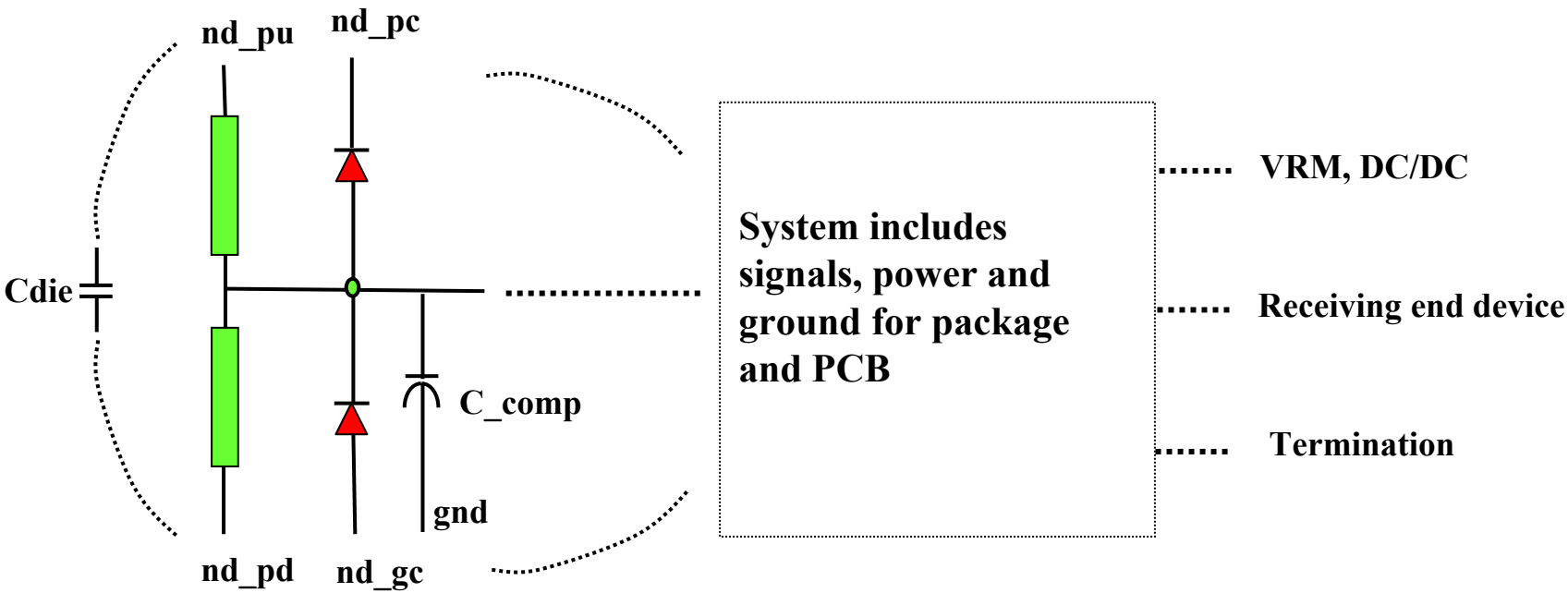

OUTPUT BUFFER




INPUT BUFFER

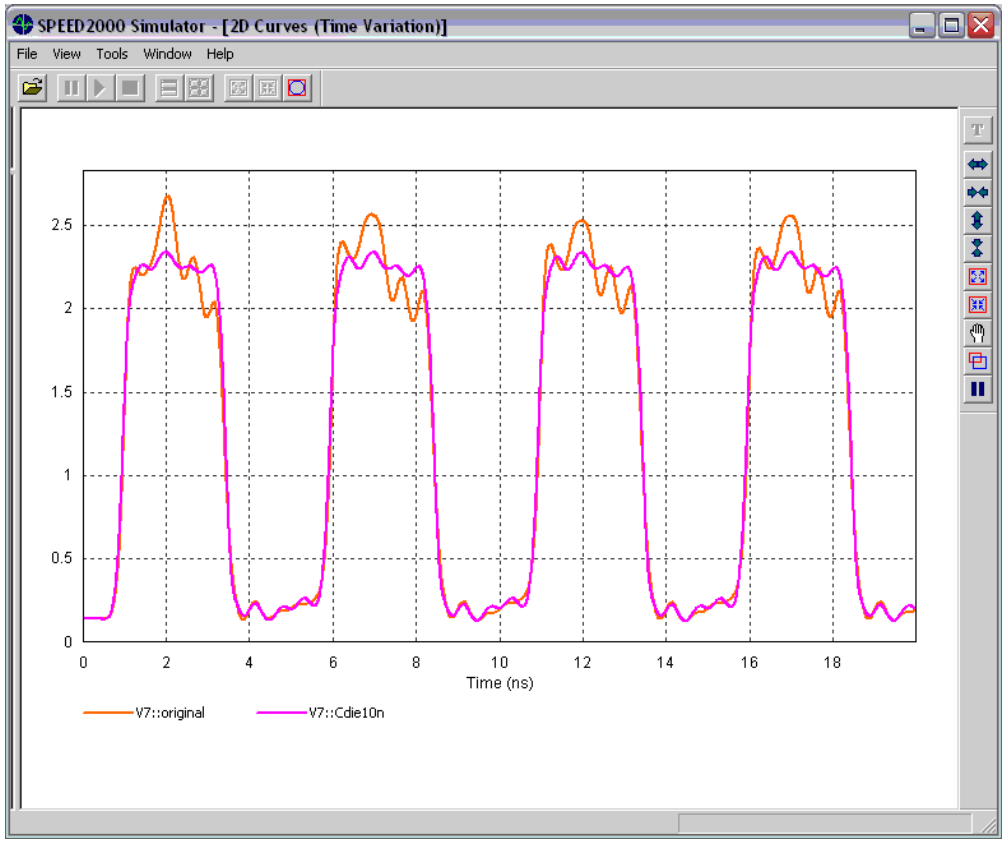
# After Adding Cdie

1. Driver end waveform will be more accurate.
2. Noise simulation will be more accurate, for example, power and ground noises at die pad.



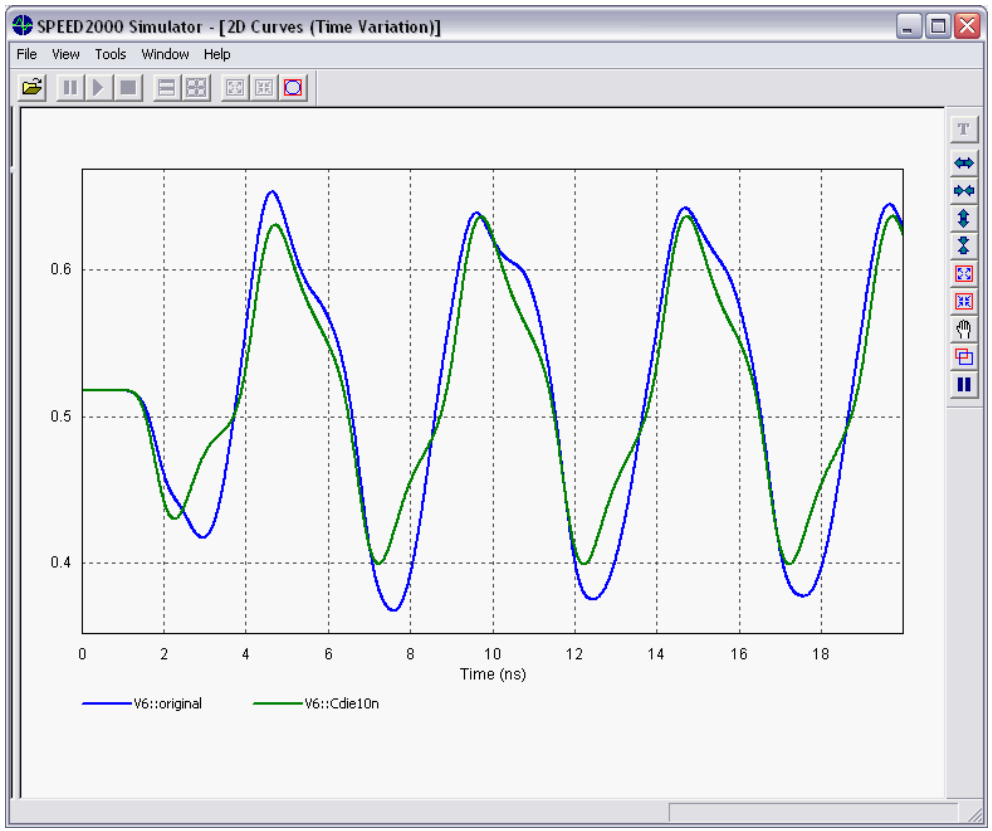
# After Adding Cdie

1. With a few nF Cdie, driver end waveform at die pad shows less ripple.



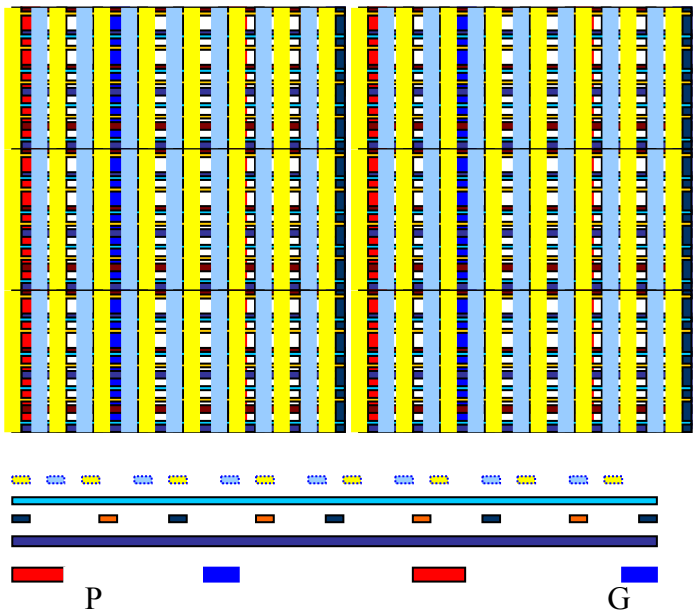
# After Adding Cdie

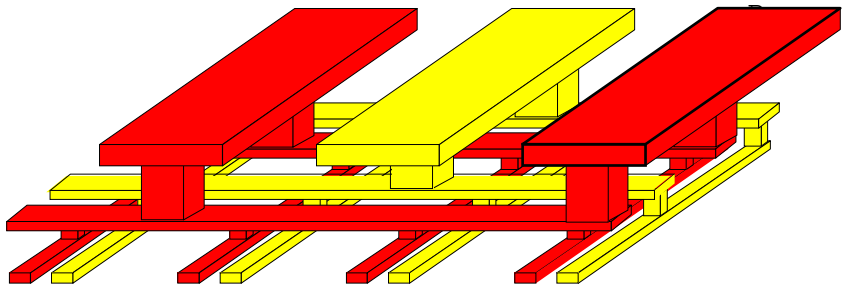
1. With a few nF Cdie, victim line (stuck low) at the board receiver end shows less noise.



# Further Discussion

- Lumped Cdie model is good for improving IBIS based system level SSO simulation.
- Adding lumped Rdie in series with Cdie can further improve simulation accuracy.
- For very accurate simulation of die pad noises, distributed on-chip power ground model is necessary, plus broadband EM models for IC package and PCB.



Distributed model for on-chip power and ground system is important to predict noises at each die pad, whereas lumped Cdie will fail. Adding good on-chip power ground model in system level simulation requires new tools.