



True Differential Buffer Models (case study)

IBIS Summit at DesignCon 2004

Santa Clara Convention Center, CA

February 2, 2004

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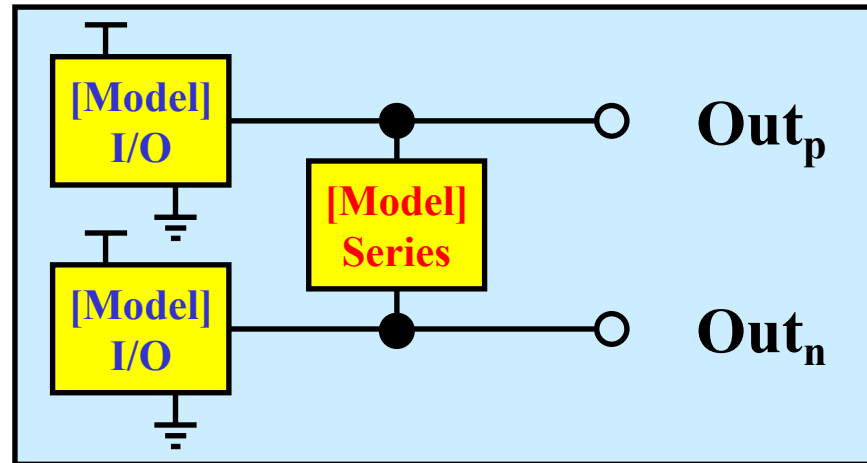
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Background

- **A new characterization technique for “true differential buffers” was introduced at the October 15, 2002 IBIS Summit**
<http://www.eda.org/pub/ibis/summits/oct02/muranyi.pdf>
- **A correlation study using the new technique was shown at the October 21, 2003 IBIS Summit**
<http://www.eda.org/pub/ibis/summits/oct03/muranyi.pdf>
- **A VHDL-AMS implementation of a true differential buffer model is shown in this IBIS Summit (today)**
- **Question:**
 - Now that we know how to make better differential models in IBIS, should we automate the process to make it easier?

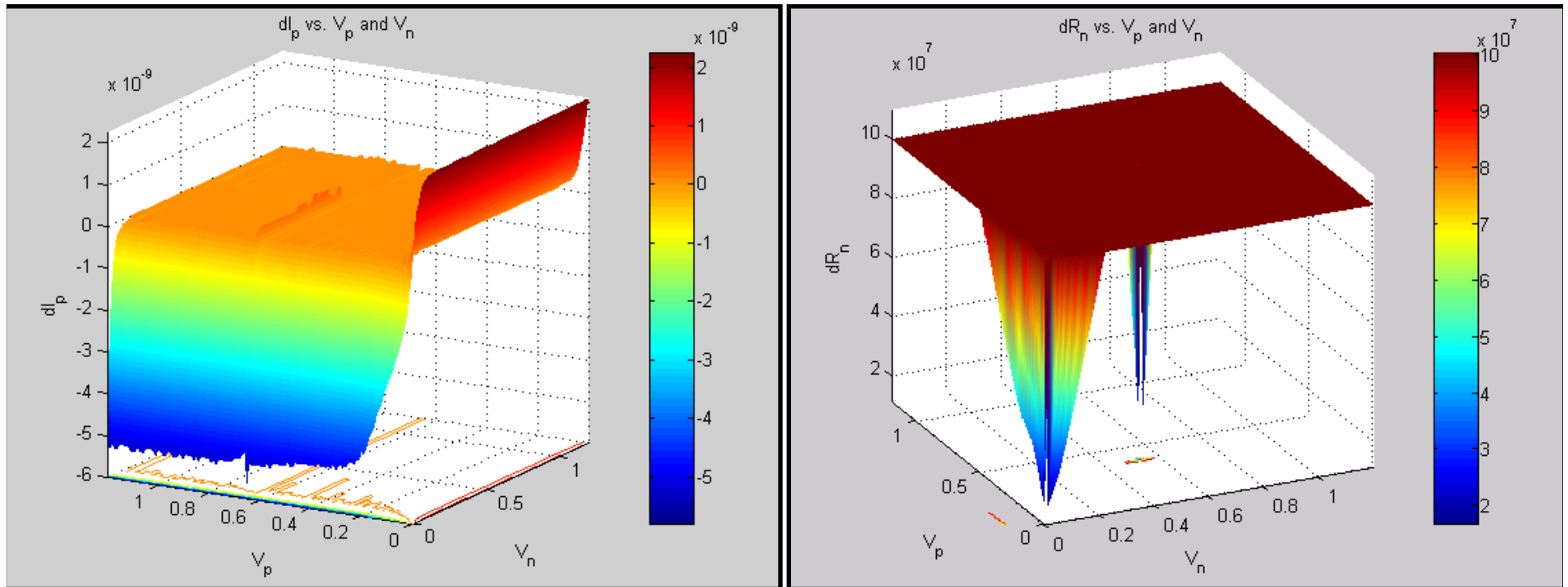
More questions



- **The new buffer characterization technique is only needed when there is a differential current flowing between the two signal pads**
 - Otherwise the [Diff Pin] association of two single ended [Model]s is sufficient
- **How much differential current flows between the signal pads in our differential buffers?**
 - We know it must be significant for buffers with on die differential termination
 - LVDS, etc...
 - ??? - for buffers without on die termination
 - USB, LVDS, etc...
 - ??? - for Pre/De-emphasis buffers
 - SATA, PCI Express, etc...

Differential current and impedance

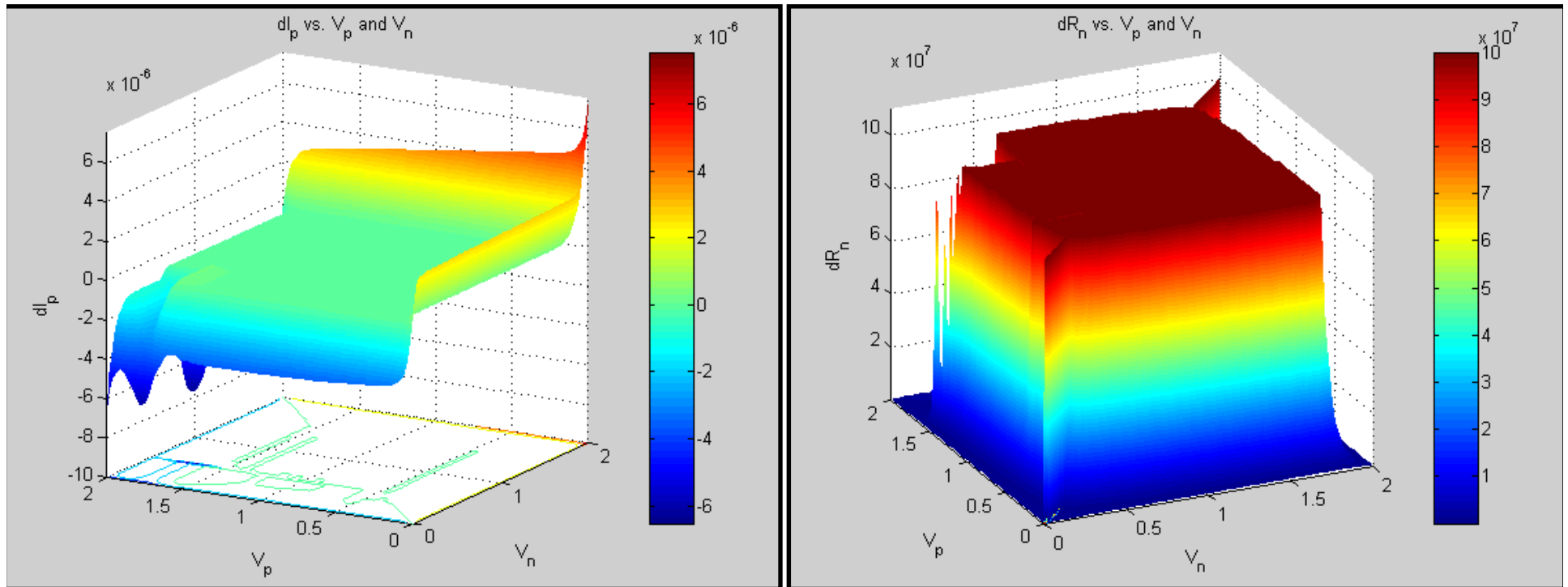
LVDS buffer – chipset “A”



Differential impedance over 100 M Ω in the operating region!

Differential current and impedance

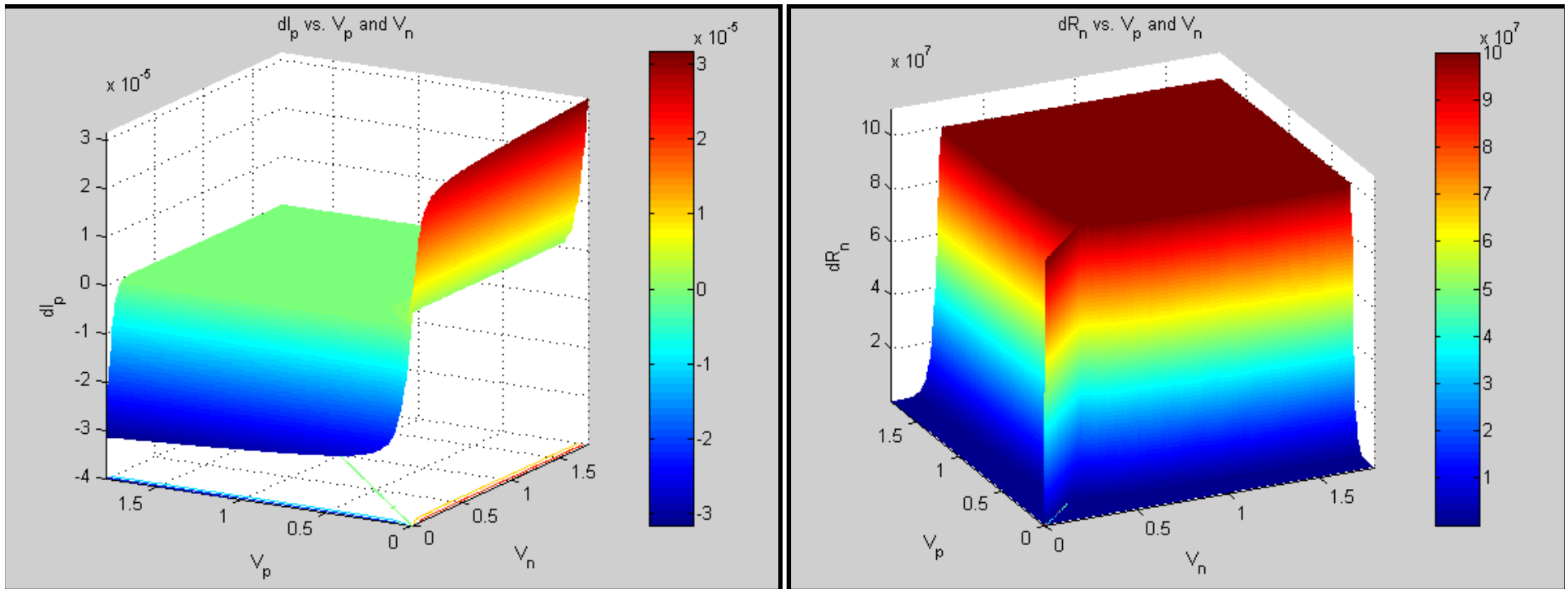
LVDS buffer – chipset “B”



Differential impedance over 100 M Ω in the operating region!

Differential current and impedance

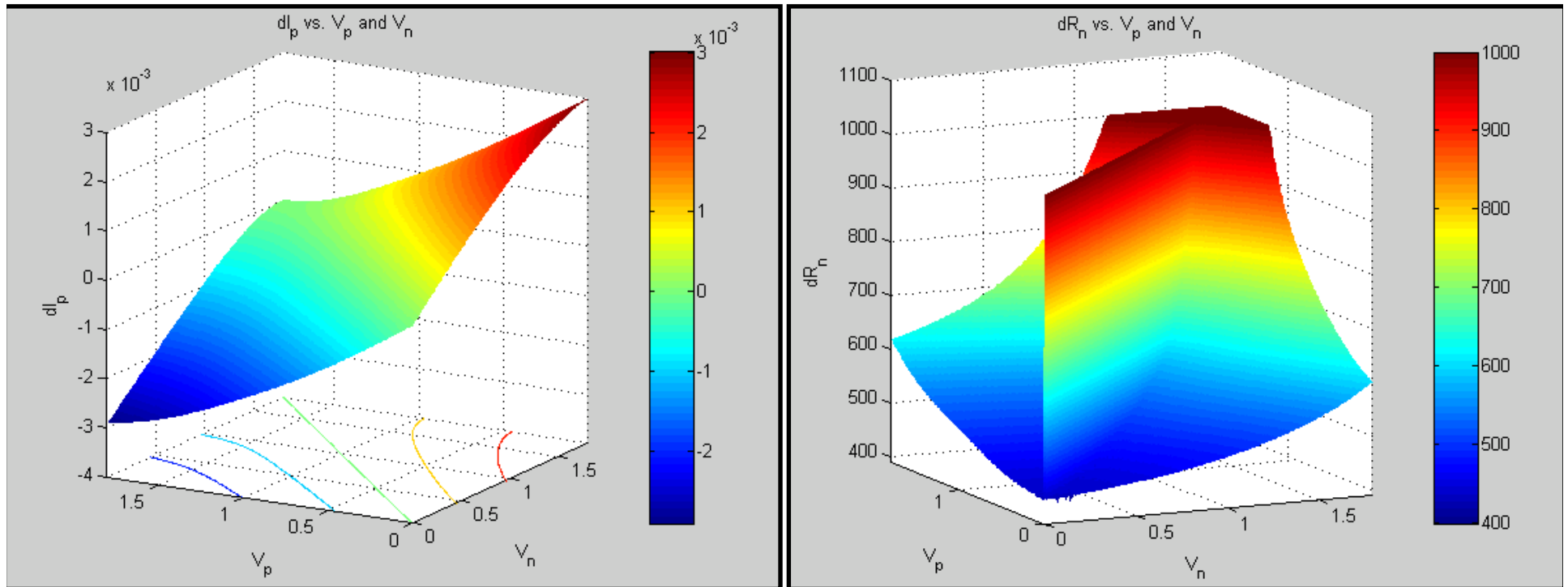
LVDS buffer with ODT turned off – chipset “C”



Differential impedance over 100 M Ω in the operating region!

Differential current and impedance

LVDS buffer with ODT turned on – chipset “C”



Differential impedance around 600 Ω !

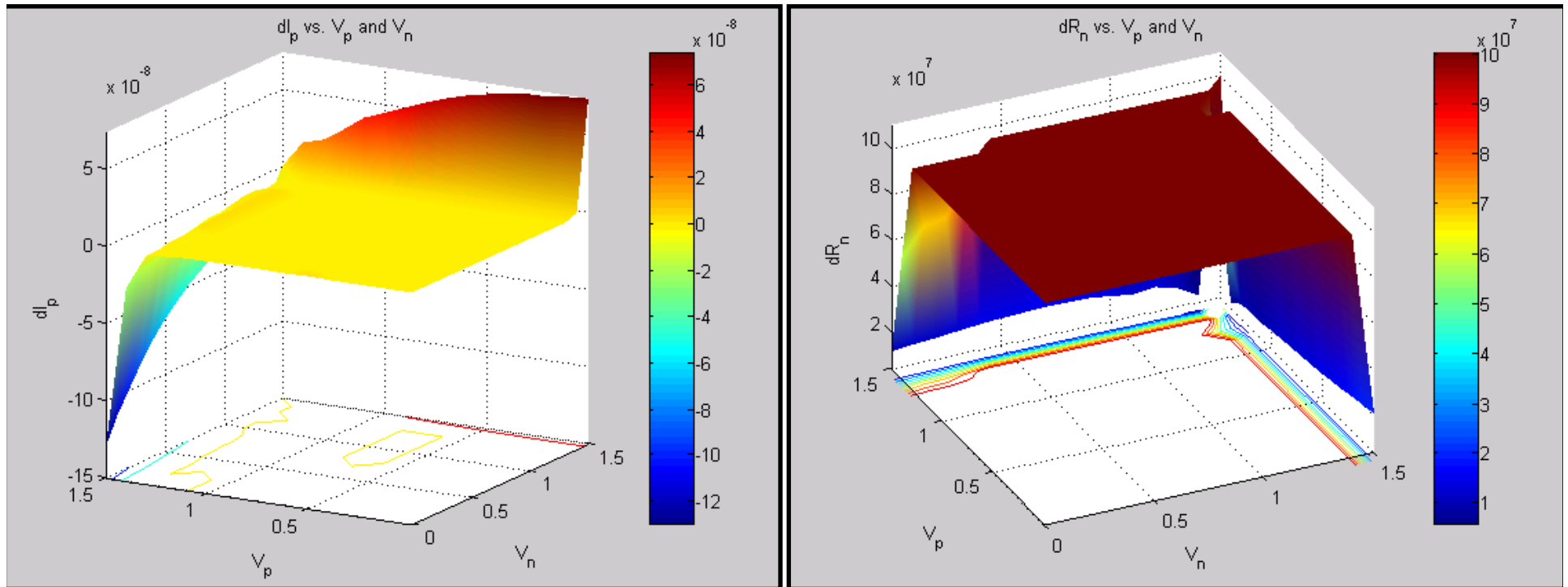
The diagram illustrates a 4T2C transmitter circuit. It consists of two main stages: a **Main** stage and a **DeE** (De-emphasis) stage. Both stages are driven by a common input signal, represented by a green circle with a downward arrow. The **Main** stage has two output nodes, **TX+** and **TX-**, which are connected to the **DeE** stage. The **DeE** stage has two output nodes, **C** and **D**. The circuit includes several components: a resistor labeled **A** in series with the input to the **Main** stage; a switch labeled **B** in parallel with the **TX-** node; a resistor labeled **C** in series with the input to the **DeE** stage; and a switch labeled **D** in parallel with the output of the **DeE** stage. The **TX+** and **TX-** nodes are connected to ground through resistors. The **TX+** node is also connected to the **DeE** stage. The **TX-** node is connected to the **DeE** stage. The **DeE** stage is connected to ground through a resistor. The **DeE** stage is connected to ground through a resistor. The **DeE** stage is connected to ground through a resistor.

Pre-emphasis
A & C = on
B & D = off

De-emphasis
A & D = on
B & C = off

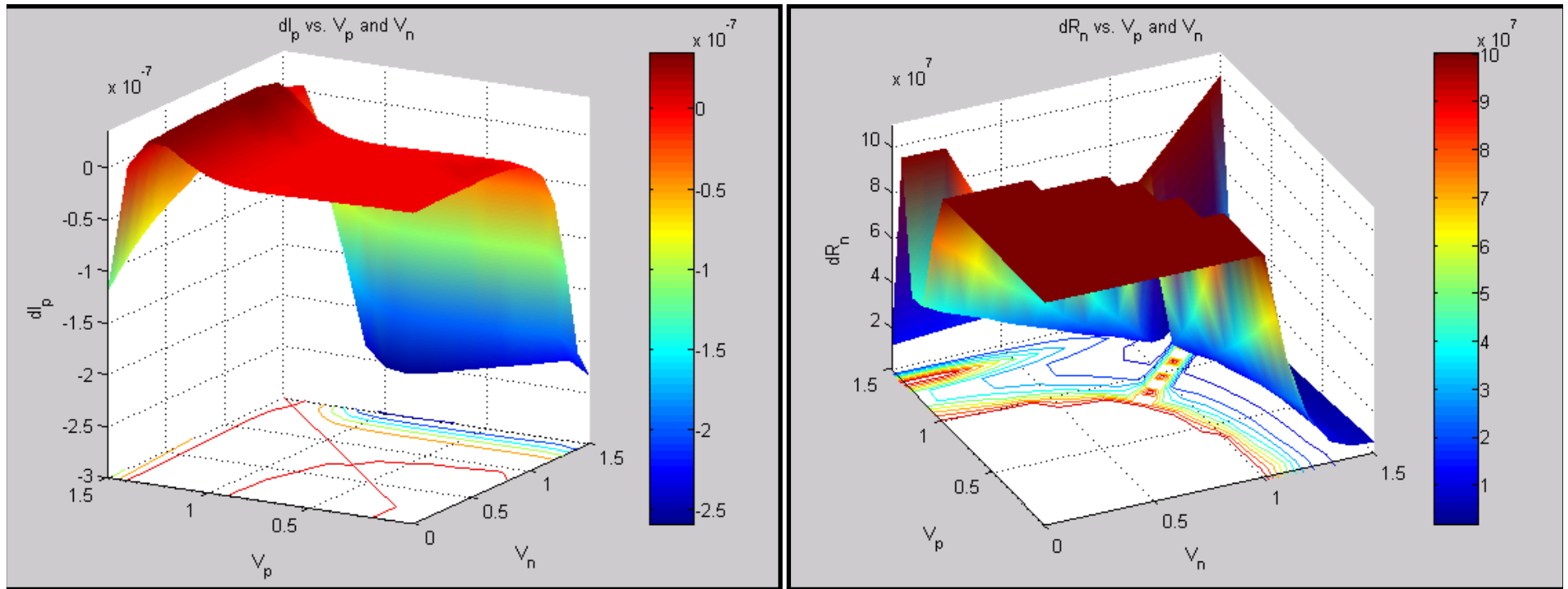
“strong bit” **“weak bit”**

Differential current and impedance SATA buffer – in “strong bit” mode



Differential impedance over 100 M Ω in the operating region!

Differential current and impedance SATA buffer – in “weak bit” mode



Differential impedance over 100 M Ω in the operating region!

Conclusion

- **All models used in this analysis were transistor level SPICE models**
- **All buffers analyzed in this study showed an extremely high differential impedance, except the one that had an on die termination**
 - Around 600 Ω when ODT was turned on
 - Otherwise over 100 M Ω in the operating region
 - Could be less outside the operating region but that will not effect the signals
- **Using the old, simple [Model] and [Diff Pin] keywords for making IBIS models for these buffers did not cause any loss of accuracy!**
- **Most of the simulations using models made with the old technique were not as bad as some feared!**