True Differential Buffer Models (case study)

IBIS Summit at DesignCon 2004

Santa Clara Convention Center, CA

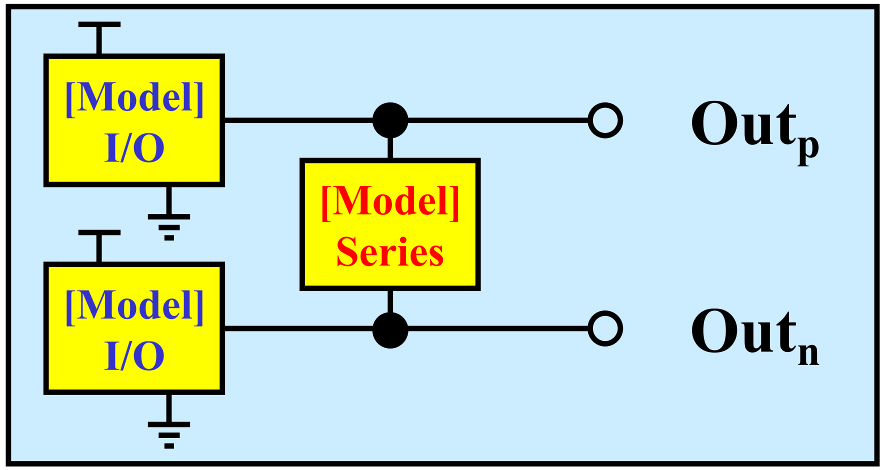
February 2, 2004

Arpad Muranyi
Signal Integrity Engineering
Intel Corporation
arpad.muranyi@intel.com

Background

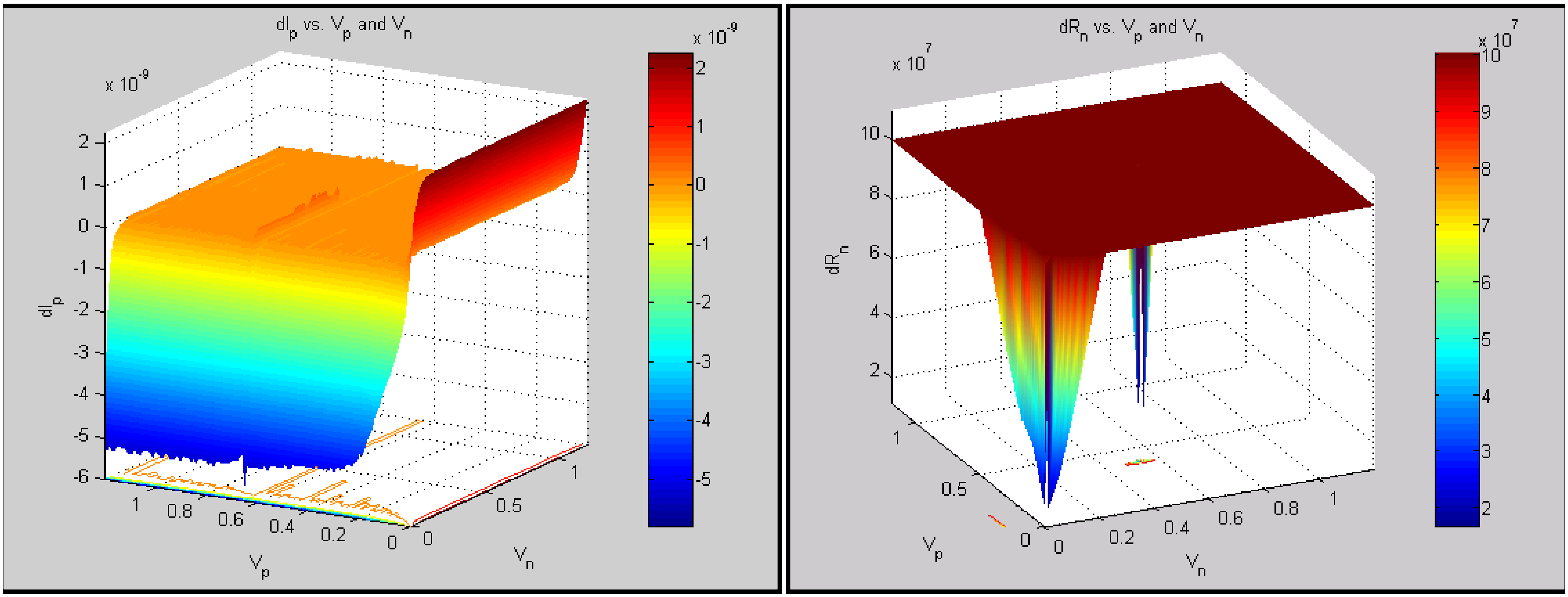
- **A new characterization technique for “true differential buffers” was introduced at the October 15, 2002 IBIS Summit**
  http://www.eda.org/pub/ibis/summits/oct02/muranyi.pdf
- **A correlation study using the new technique was shown at the October 21, 2003 IBIS Summit**
  http://www.eda.org/pub/ibis/summits/oct03/muranyi.pdf
- **A VHDL-AMS implementation of a true differential buffer model is shown in this IBIS Summit (today)**
- **Question:**
  - Now that we know how to make better differential models in IBIS, should we automate the process to make it easier?

More questions



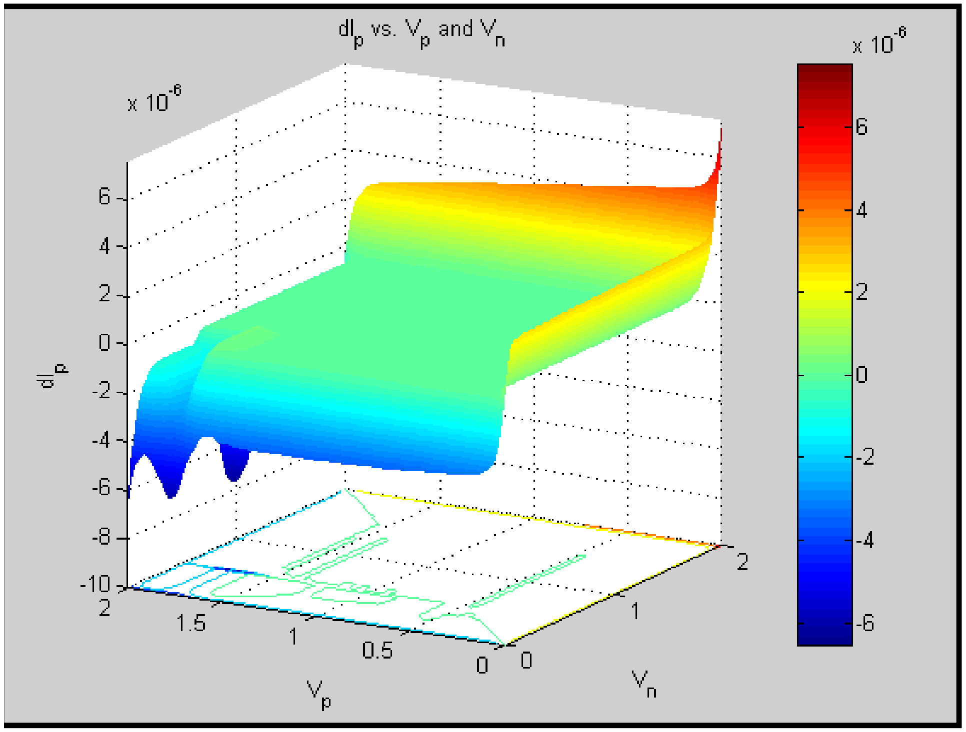
- **The new buffer characterization technique is only needed when there is a differential current flowing between the two signal pads**
  - Otherwise the [Diff Pin] association of two single ended [Model]s is sufficient
- **How much differential current flows between the signal pads in our differential buffers?**
  - We know it must be significant for buffers with on die differential termination
    - LVDS, etc…
  - ??? - for buffers without on die termination
    - USB, LVDS, etc…
  - ??? - for Pre/De-emphasis buffers
    - SATA, PCI Express, etc…

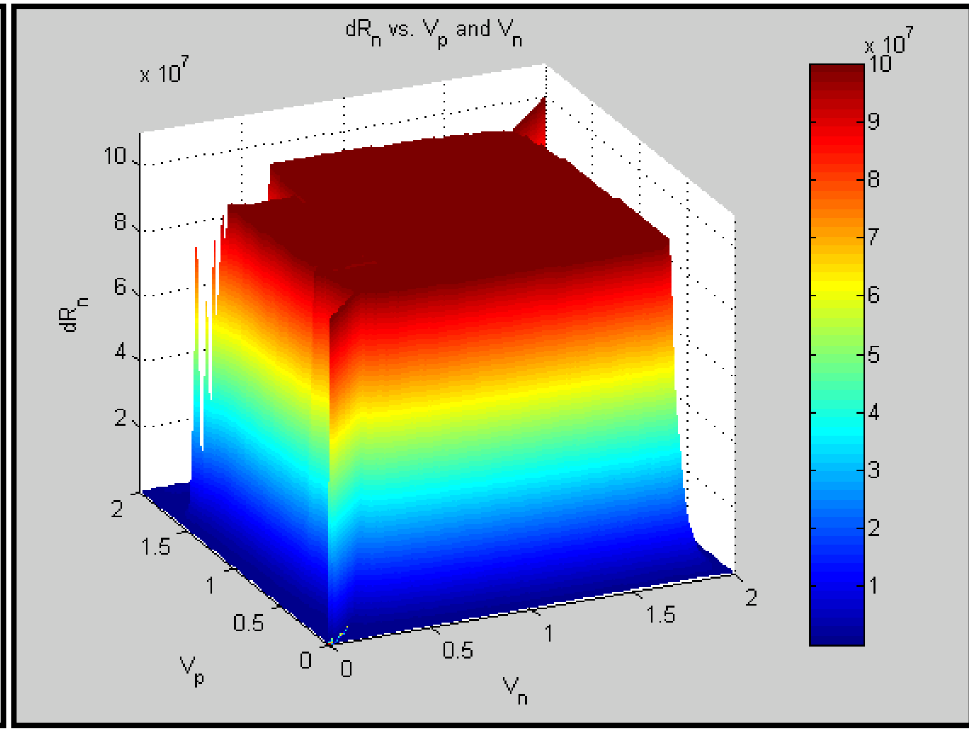
Differential current and impedance LVDS buffer – chipset "A"



Differential impedance over 100 MΩ in the operating region!

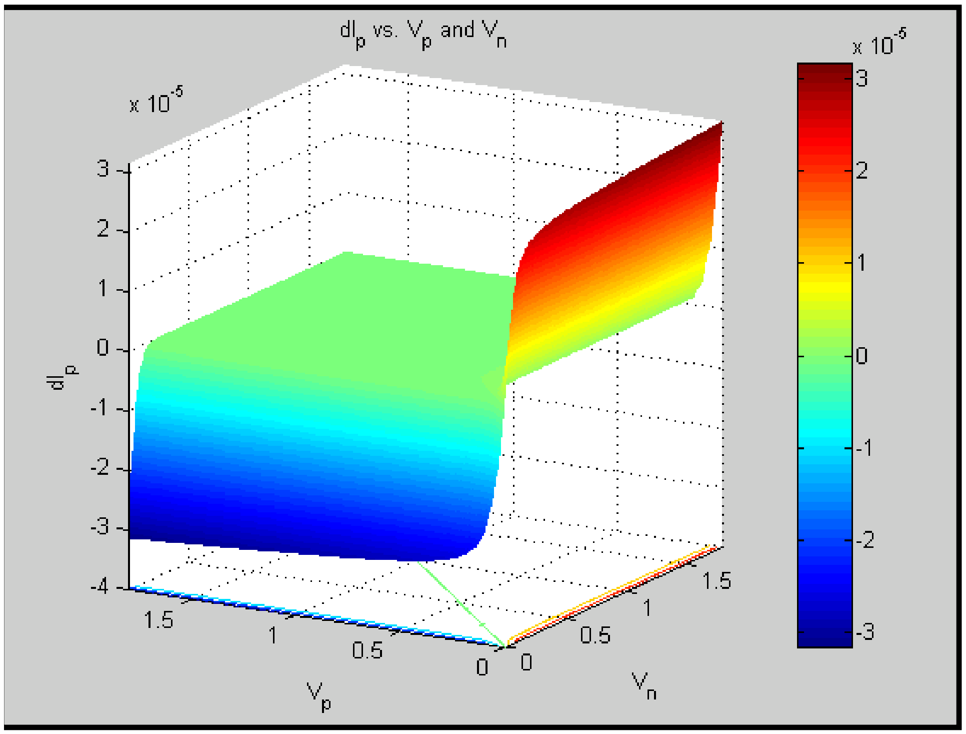
Differential current and impedance
LVDS buffer – chipset "B"

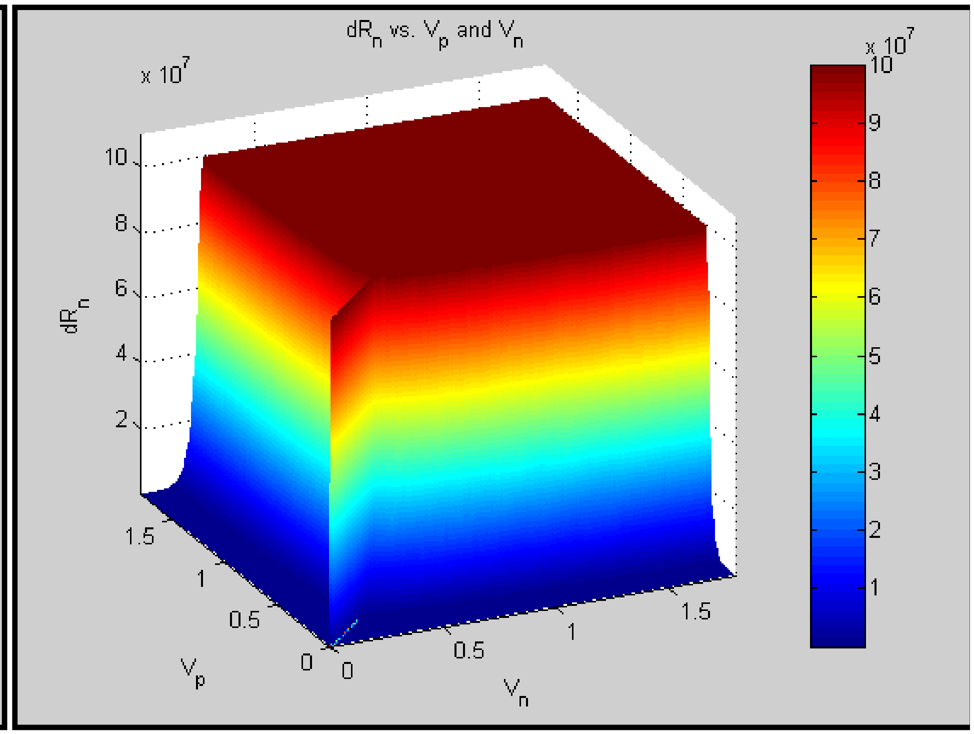




Differential impedance over 100 MΩ in the operating region!

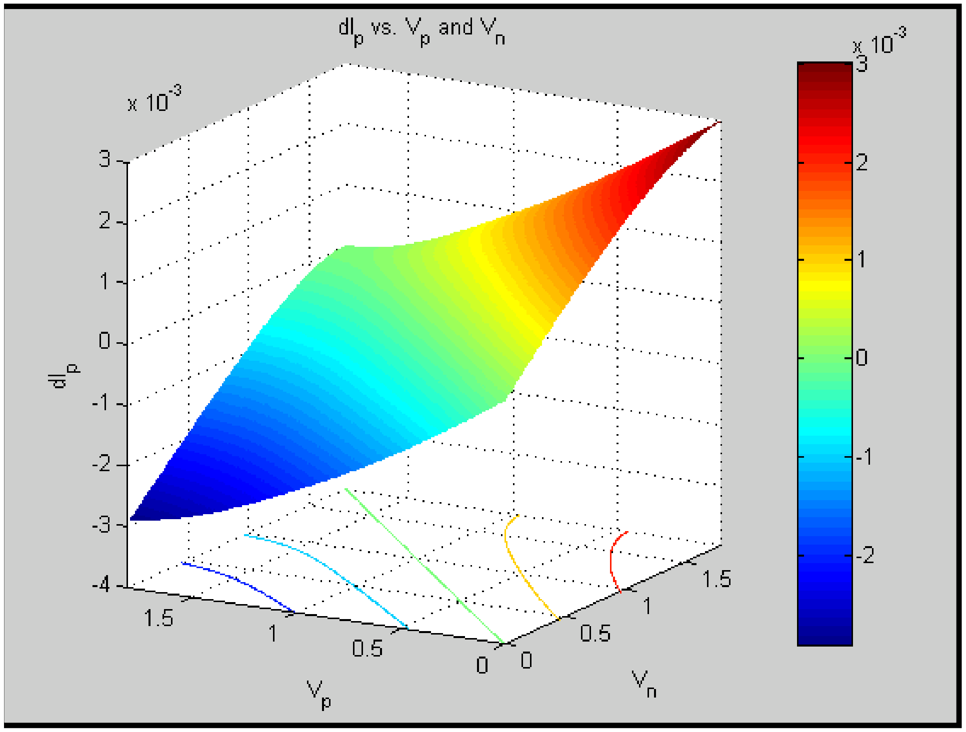
Differential current and impedance
LVDS buffer with ODT turned off – chipset “C”

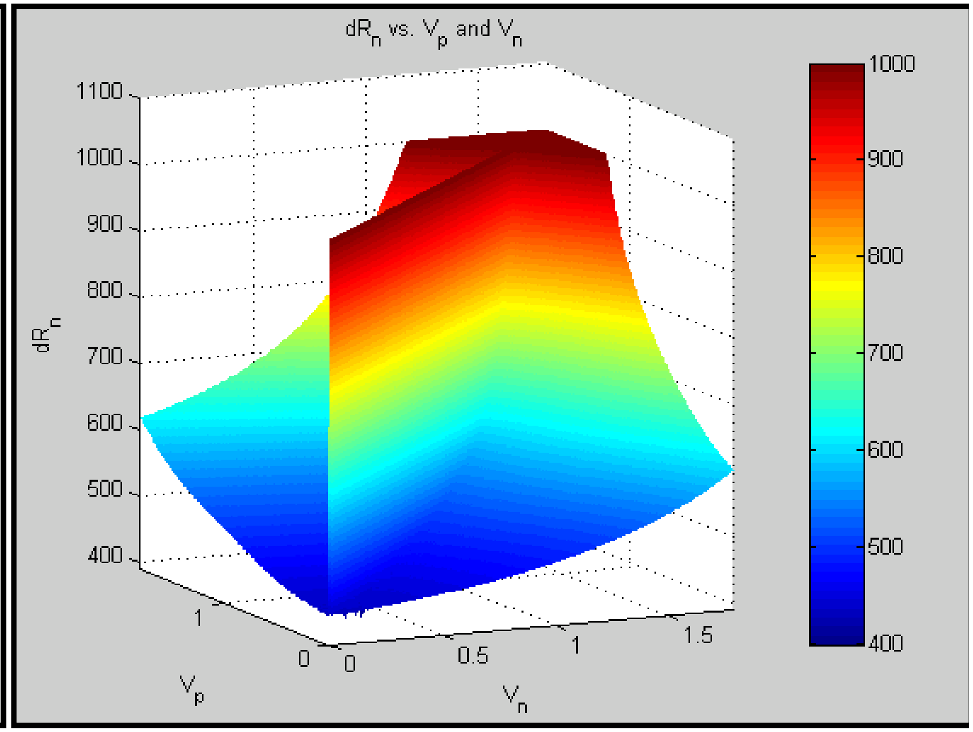




Differential impedance over 100 MΩ in the operating region!

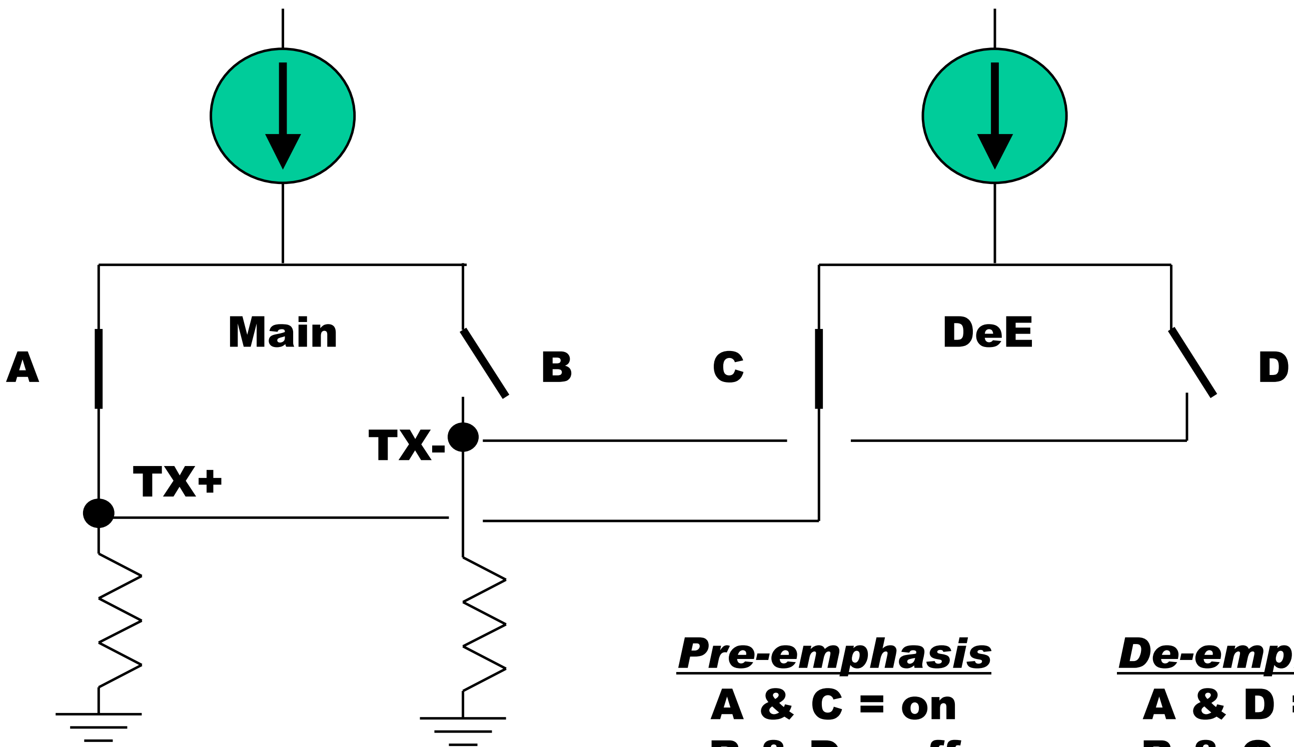
Differential current and impedance
LVDS buffer with ODT turned on – chipset "C"





Differential impedance around 600 Ω!

Pre/De-emphasis buffer overview (SATA)



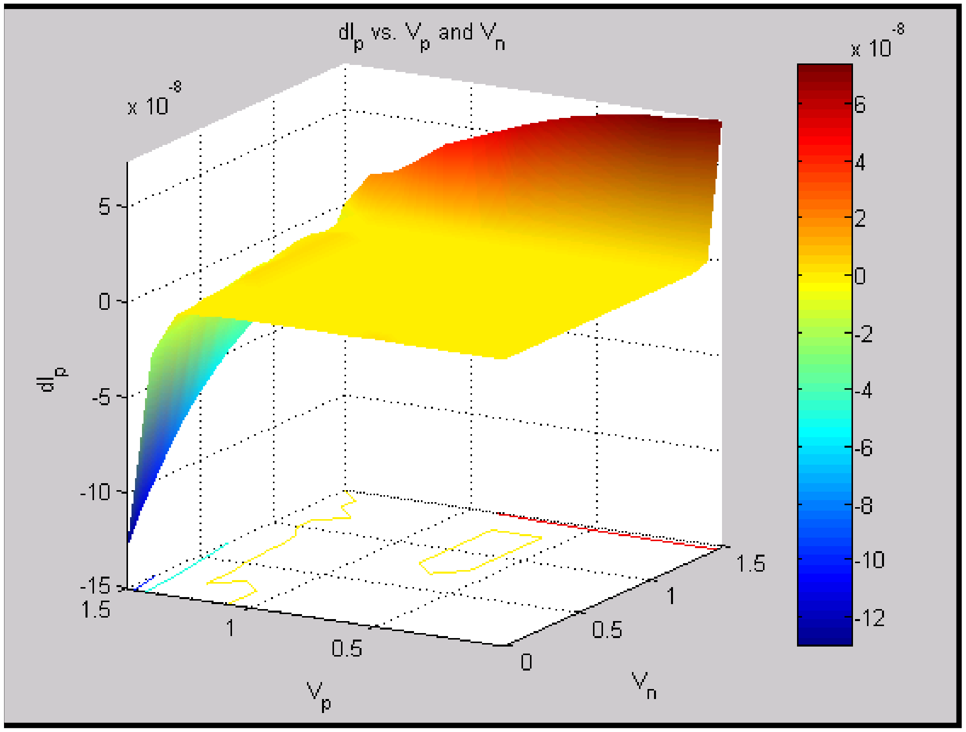
Pre-emphasis
A & C = on
B & D = off

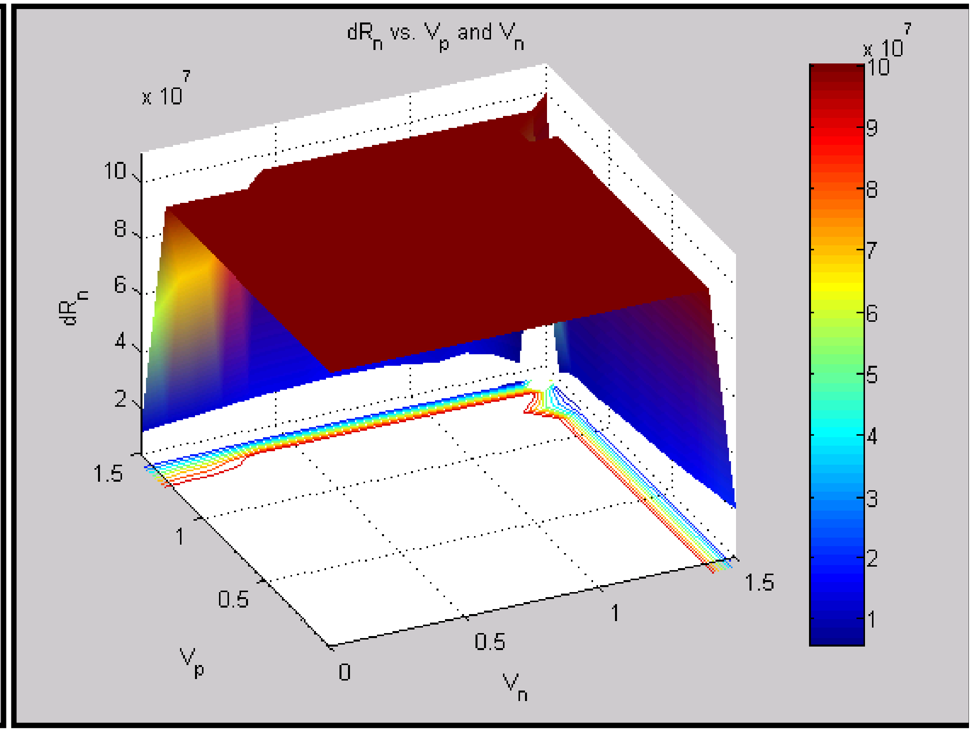
"strong bit"

De-emphasis
A & D = on
B & C = off

"weak bit"

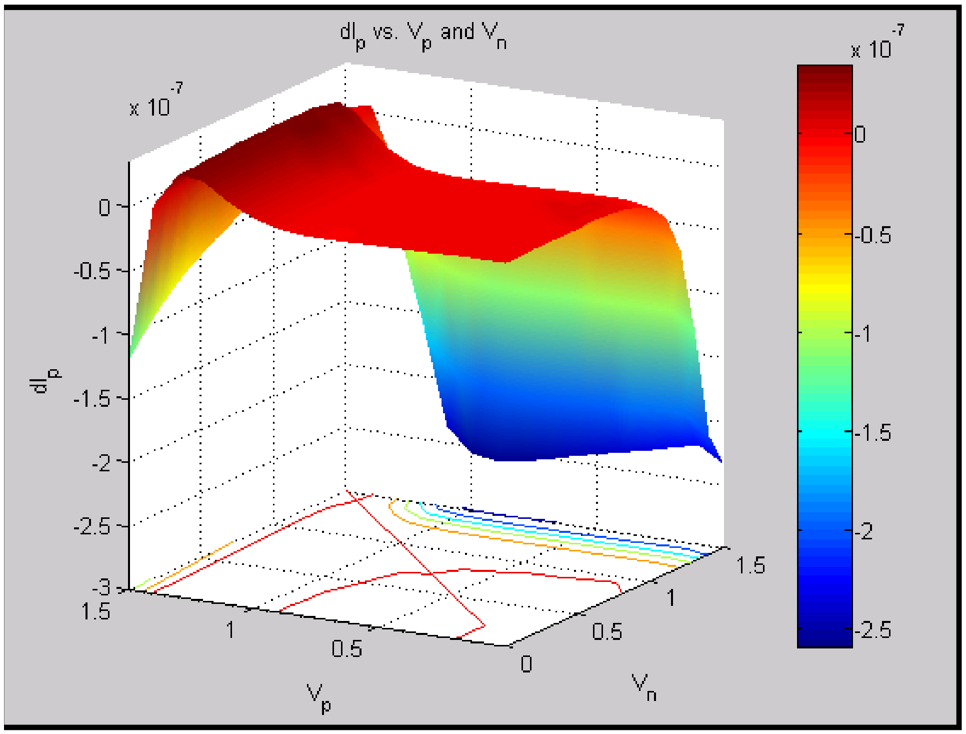
Differential current and impedance SATA buffer – in "strong bit" mode

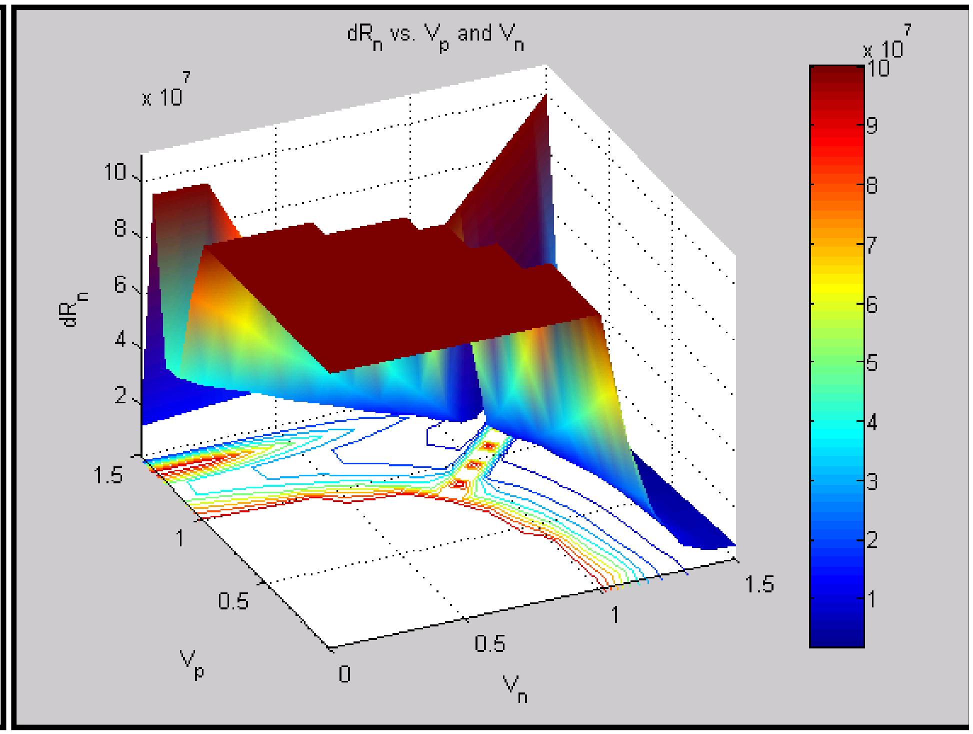




Differential impedance over 100 MΩ in the operating region!

Differential current and impedance SATA buffer – in "weak bit" mode





Differential impedance over 100 MΩ in the operating region!

Conclusion

- **All models used in this analysis were transistor level SPICE models**
- **All buffers analyzed in this study showed an extremely high differential impedance, except the one that had an on die termination**
  - Around 600 Ω when ODT was turned on
  - Otherwise over 100 MΩ in the operating region
  - Could be less outside the operating region but that will not effect the signals
- **Using the old, simple [Model] and [Diff Pin] keywords for making IBIS models for these buffers did not cause any loss of accuracy!**
- **Most of the simulations using models made with the old technique were not as bad as some feared!**