IBIS Die V-T Tables from Part or Board Measurements

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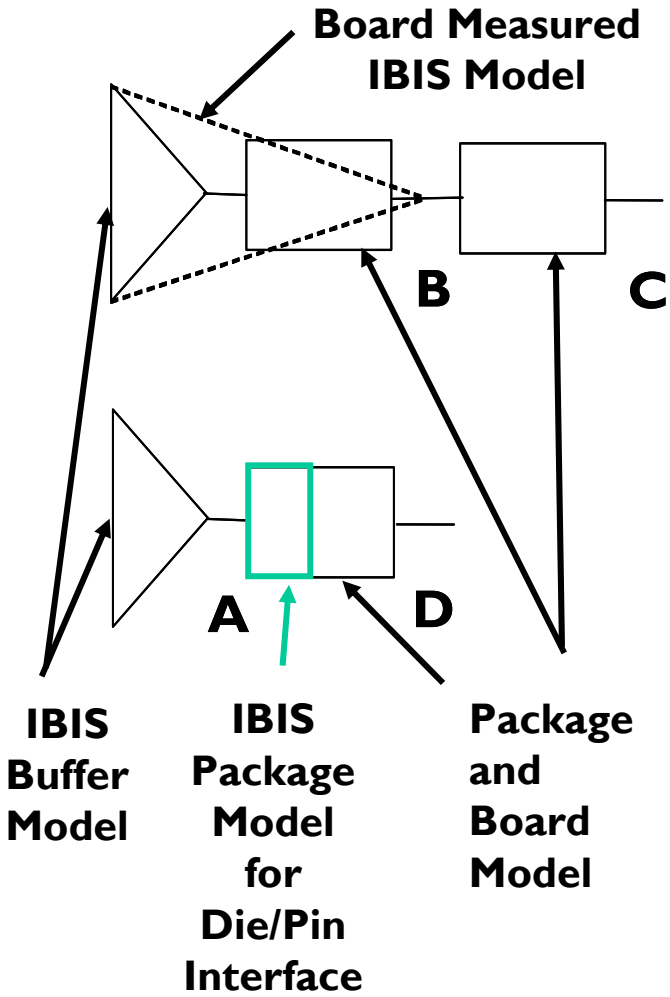
Contents

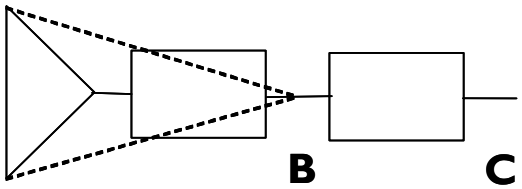
- Problem
  - Measurement based IBIS models get V-T data at hardware test fixture interface
    - Includes pin package (model) and test fixture
  - Need accurate estimate the IBIS Die V-T data
- "Delta" process illustrated
  - Transforms TIME axis of measured V-T data
  - Assumes the package/test fixture can be modeled (e.g., from TDR measurements)
- Observations and Conclusions

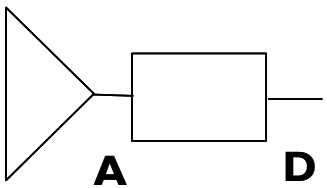
Steps for "Delta" Process IBIS Die V-T Tables from Pin/Board V-T Tables

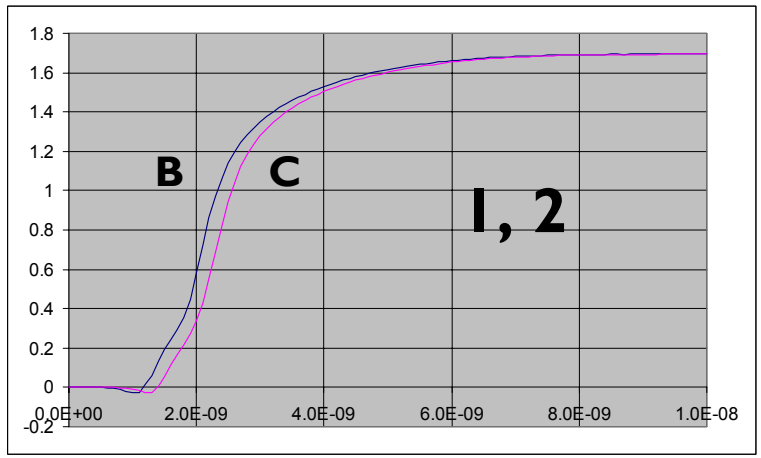


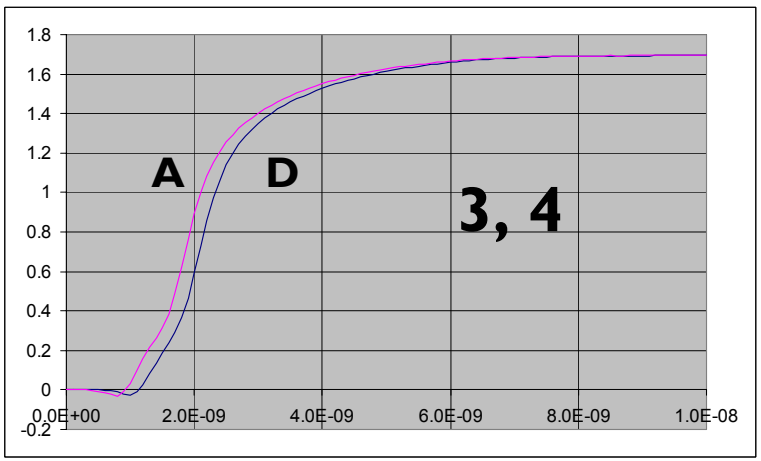
1. Create IBIS model using MEASURED V-T tables at **B**
2. Simulate **B**, then add package/ board and simulate "delta" **C**
3. Use inverse of linear transform of **B** time axis to derive new IBIS model DIE V-T table **A**
4. Add package/board to simulate V-T response at **D**
5. Compare **B** and **D**

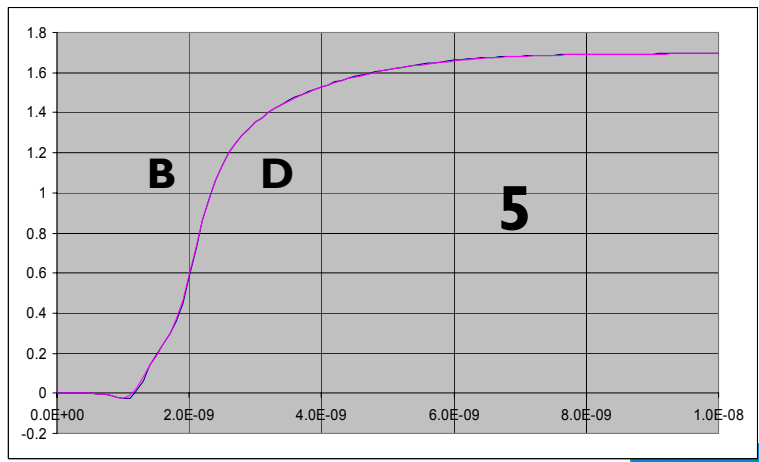
Illustrated Steps Using Real Measurement (50 Ohms to Gnd)











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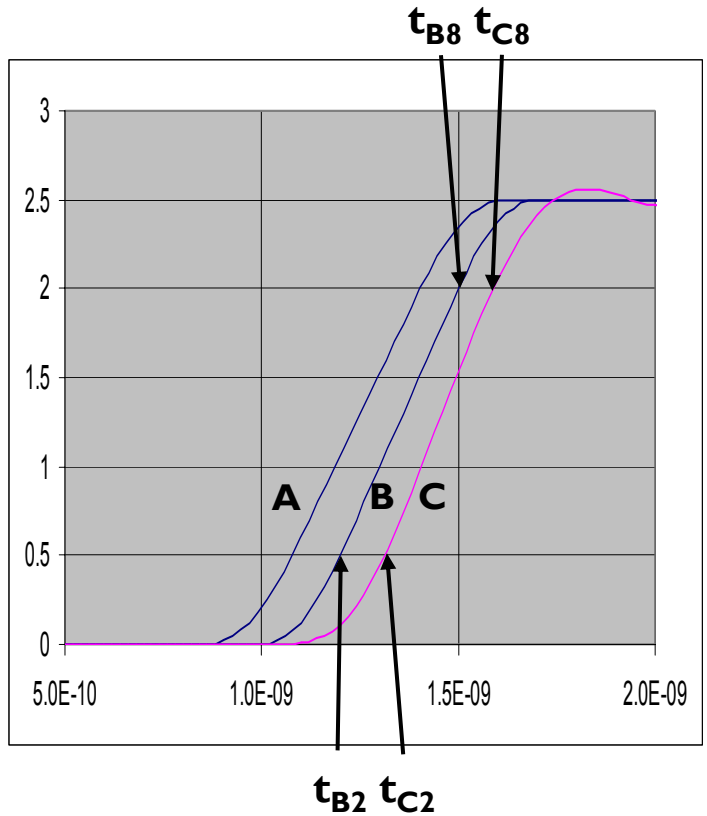
Step 3: Inverse Linear Transform to Find V-T table A from B

- Find times for 80% and 20% points of **B**, **C**: t_{B8}, t_{B2}, t_{C8}, t_{C2} (interpolate for accuracy)
- Solve transform for p and q:
  $\mathbf{t_C} = p * \mathbf{t_B} + q$
  (& assume $\mathbf{t_B} = p * \mathbf{t_A} + q$)
- Inverse transform time axis $\mathbf{t_B}$ to time axis $\mathbf{t_A}$ using:
  $\mathbf{t_A} = (\mathbf{t_B} - q) / p$
- $\mathbf{t_A} = t_{B8} + (\mathbf{t_B} - t_{C8}) * (t_{B8} - t_{B2}) / (t_{C8} - t_{C2})$



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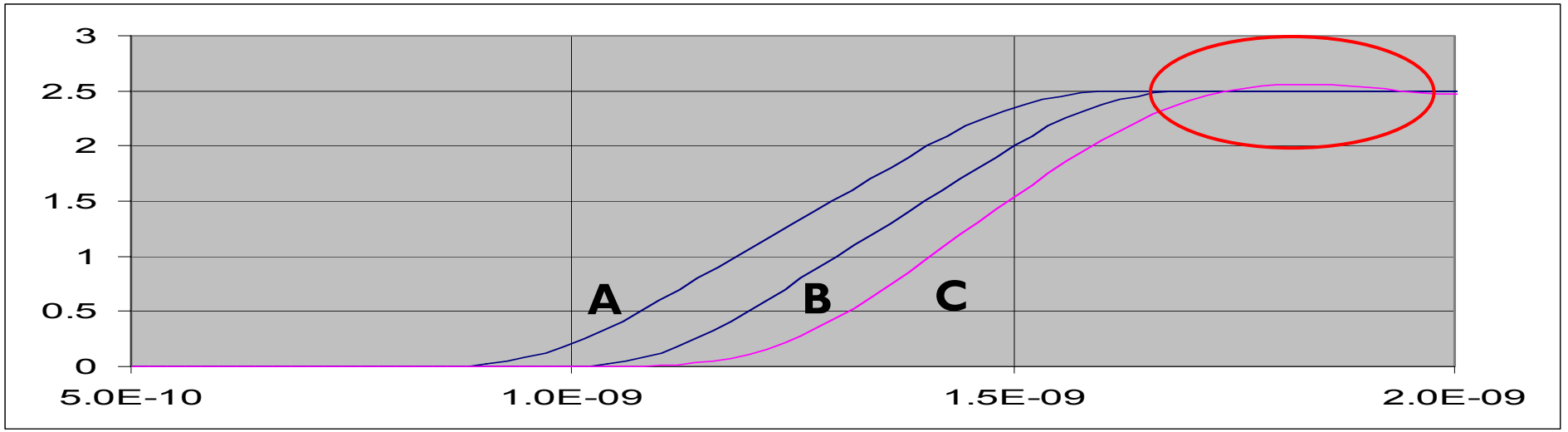
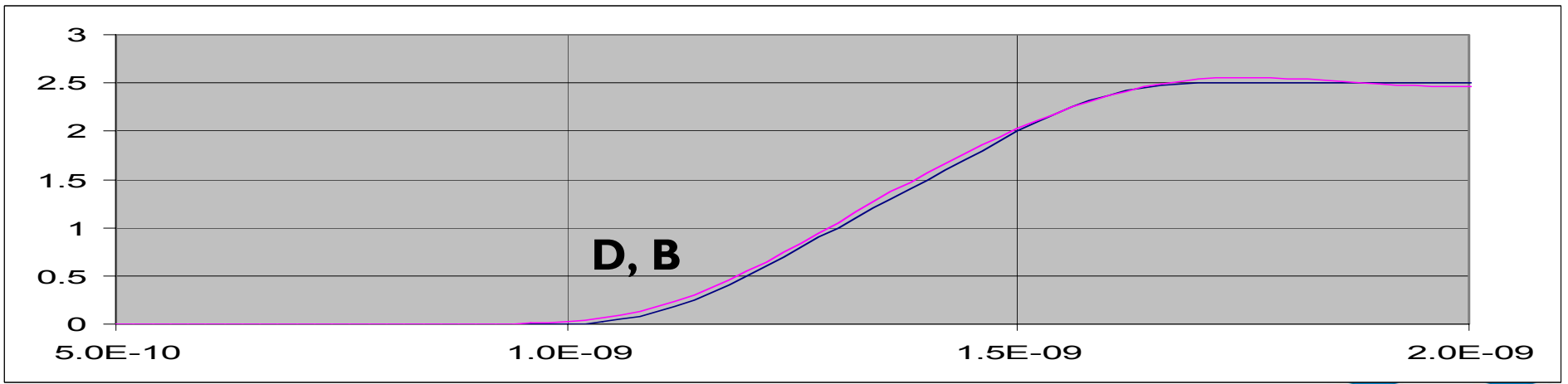
Example 1 – Delayed Rounded Ramps Package Only, No Board

- Assumed measurement based IBIS model:
  - 5 Volt Buffer
  - 50 Ohm pullup, pulldown
  - 4 V-T ideal rounded ramps extracted at the pin (**B**)
  - No clamps
  - C_comp = 5 pF
- Lumped package model
  - L_pkg = 5 nH, C_pkg = 2 pF (50 Ohms, 100 ps)
- V-T tables derived for new IBIS model
  - Tested at pin interface (**D**)

Example 1 - 50 Ohms to Gnd (Lumped Package) with Overshoot





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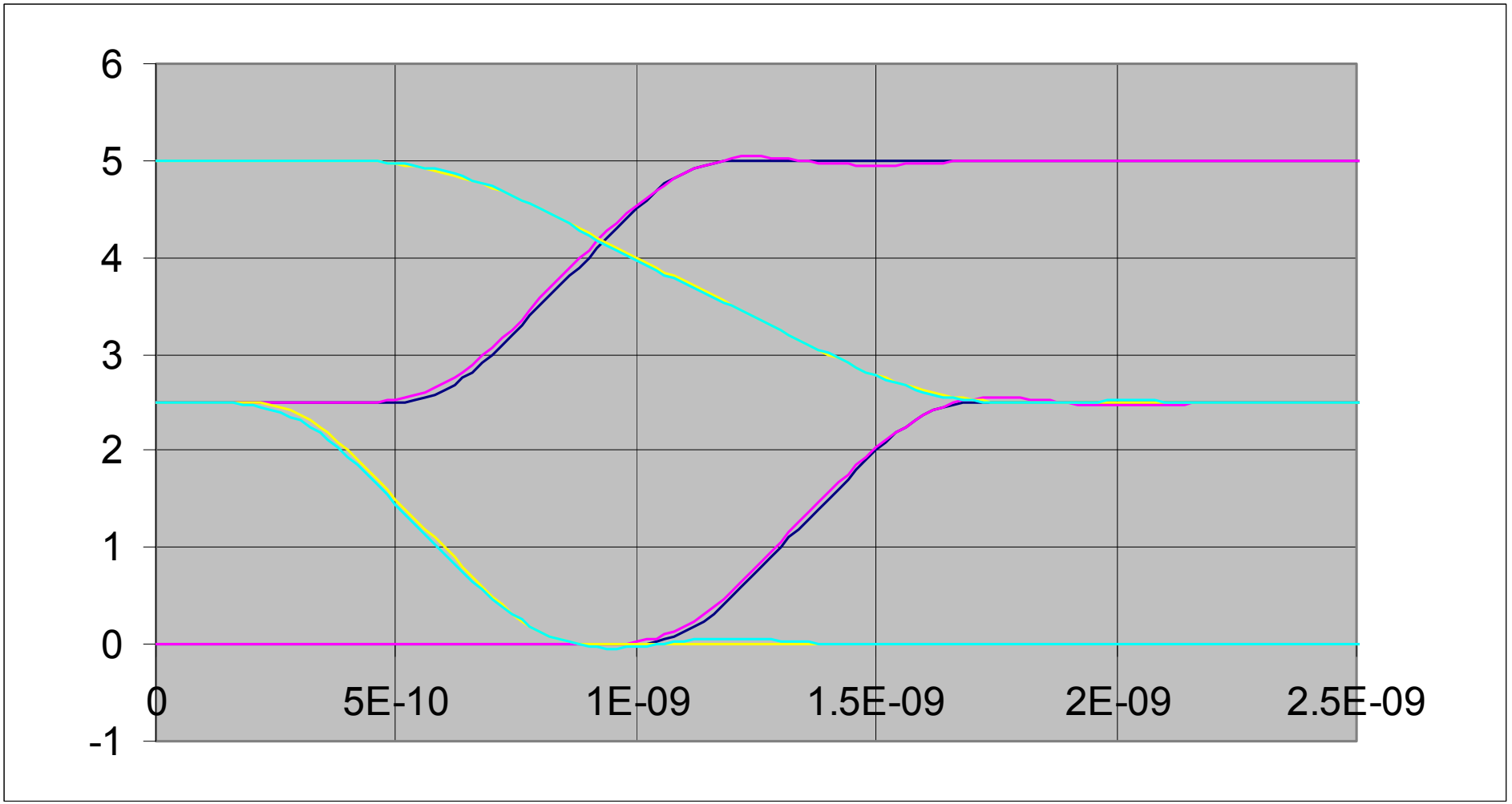
Example 1 – Overlay of B, D for 50 Ohms to Gnd/Vcc Waveforms



Example 2 – Real Device with Test Fixture Board

- Pin D2 V-T data of mounted device measured at test fixture interface
  - C_comp=2.0 pF in model (about 1.8 pF TDA Systems extraction)
- Package/Test Board model from TDA Systems IConnect®:
  - R_pin=0.023 Ohms, L_pin=2.05 nH, C_pin=0.57 pF
  - Z0=79.5 Ohms TD=70 ps (board)
  - Z0=86.5 Ohms TD=34 ps (board)
  - Z0=49.8 Ohms TD=55.8 ps (50 Ohm extension)
- HSpice B-element used to simulate BI-2.6V buffers
- Graphs later show OVERLAYING **B, D** simulations of all corners and V-T tables (50 ohms to ground/Vcc for rising and falling edges)

Example 2 - Package/Board Extraction

- Pin D2 V-T data of mounted device measured at test fixture interface
  - C_comp=2.0 pF in model (about 1.8 pF TDA Systems extraction)
- Package/Test Board model from TDA Systems IConnect®:
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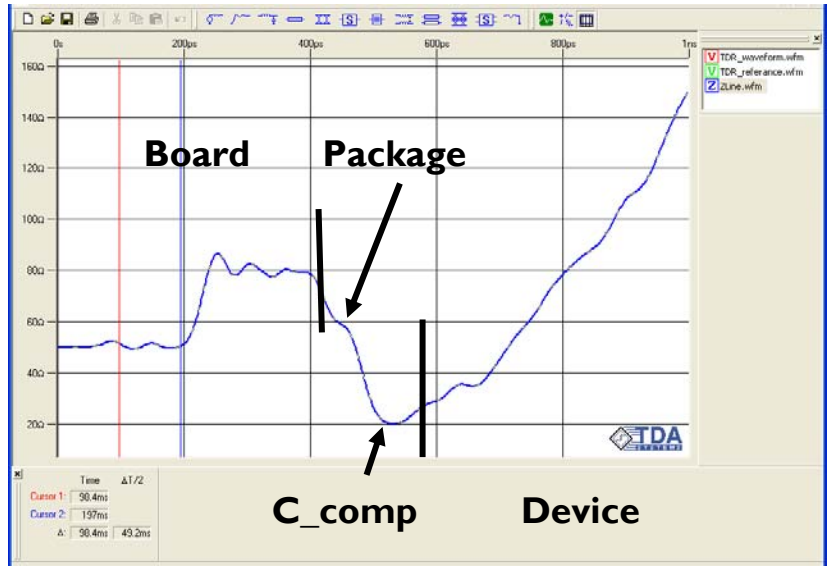


```
•subckt Single_Line_2 port1 port2 gnd_
t1  port1  gnd_  1  gnd_ Z0=49.8 TD=55.8p
t2  1  gnd_  2  gnd_ Z0=86.5 TD=34p
t3  2  gnd_  3  gnd_ Z0=79.5 TD=70p
t4  3  gnd_  4  gnd_ Z0=57.3 TD=32.9p
t5  4  gnd_  5  gnd_ Z0=20.2 TD=36.1p
t6  5  gnd_  port2  gnd_ Z0=114 TD=198p
.ends
```


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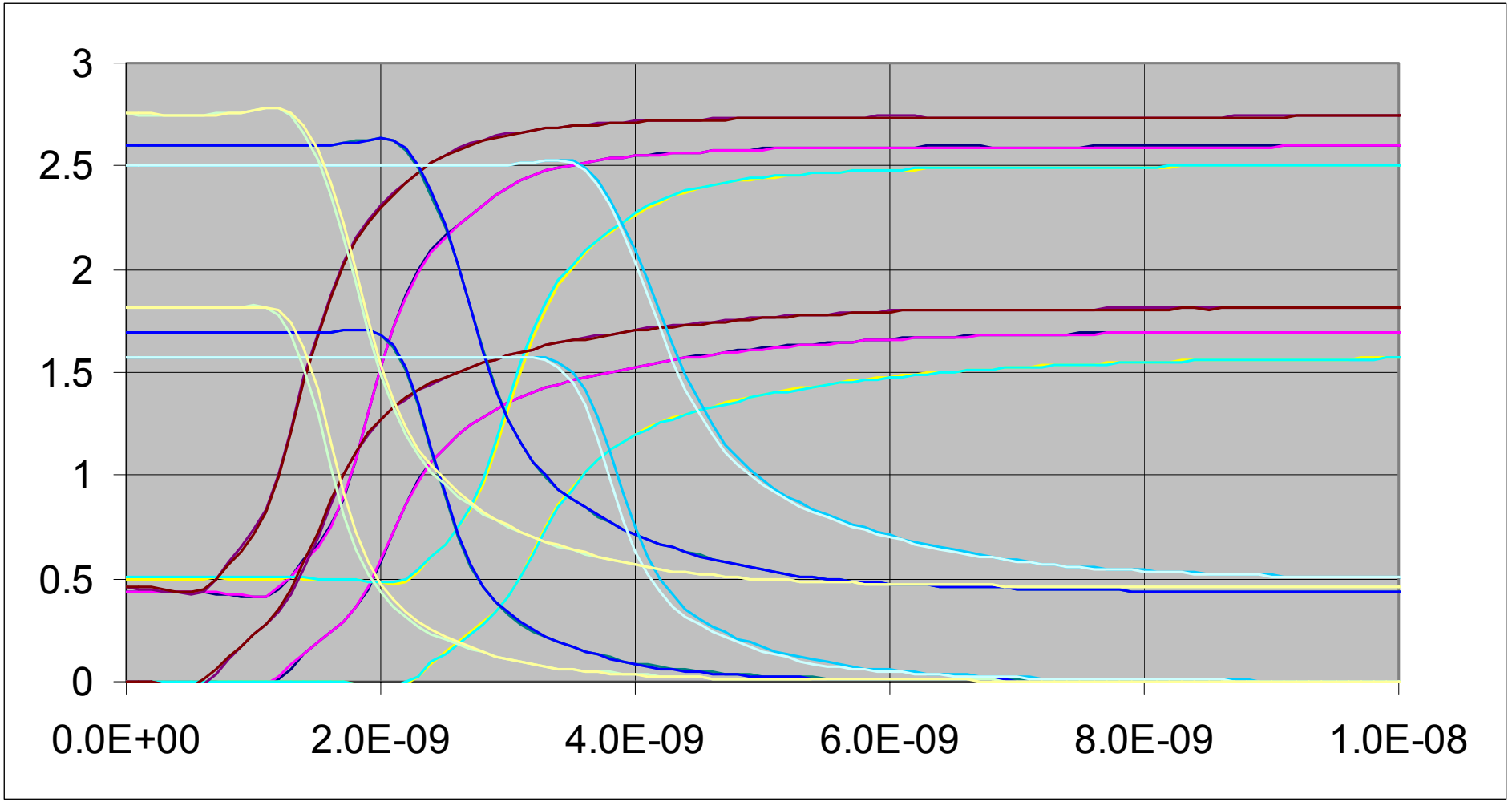
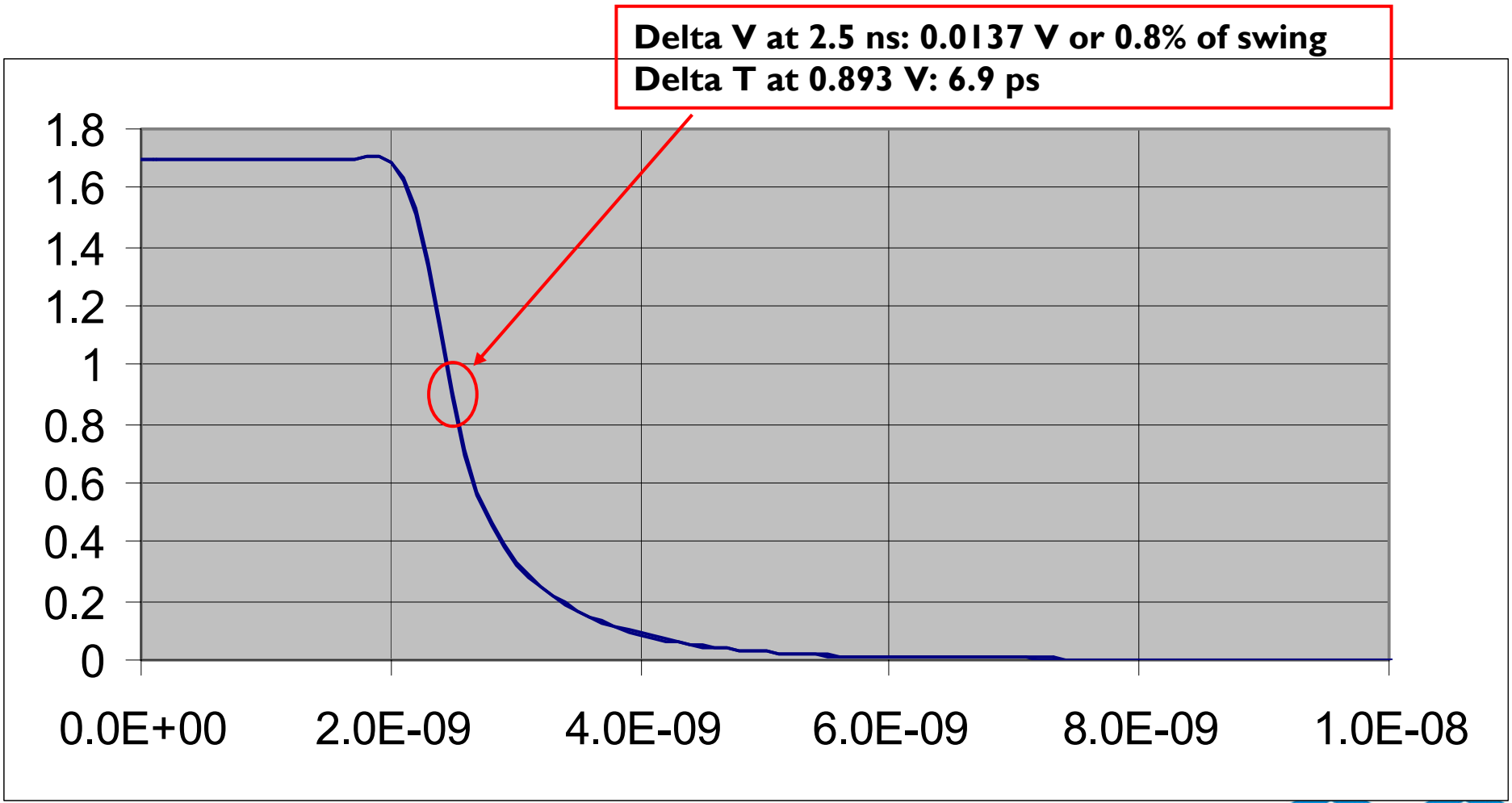
BI-2.6V – B, D Overlaying V-T Model Simulations (min/typ/max)



Typ Column Overlaying B, D Falling Waveform Match



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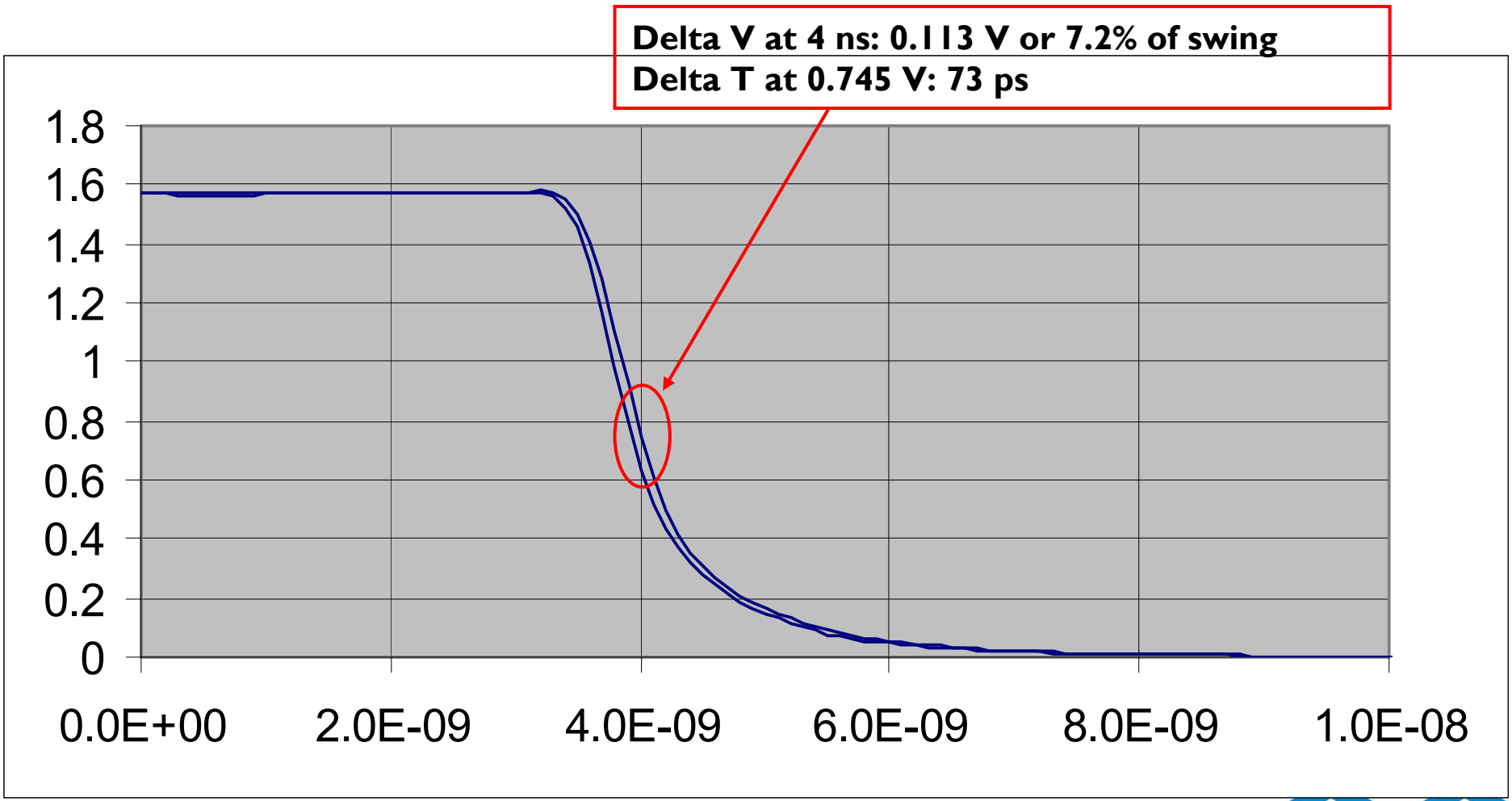
Min Column B, D
Falling Waveform Mismatch



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Column Mismatch Refinement Ideas

- Combine the time axis
  - With 1000 points, just put the min column with same time points shifted by 73 ps (NA's every other point for each column)
  - Or interpolate new corner data to typ time axis
  - Or interleave independently derived typ/min/max axis
- Or just improve the approximation
  - Use three column data point averages for overall average inverse linear transform
  - Or do three column linear regression for closer overall transformation

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Additional Observations

- Delta should work with any EDA tool with:
  - IBIS waveform algorithm that reproduces test fixture responses
  - Time step control for simulation and output (resolution, interpolation)
  - Ability to process complex packages
- Other possible "formal" approaches
  - Optimization, feedback methods, FFT/Inverse-FFT methods, de-convolution, …
  - Potential numerical artifacts and other errors
- NOT EXACT, but an EXCELLENT APPROXIMATION
  - Might not capture some detail (e.g., overshoot, glitches)
  - Preserves waveform shapes
  - Adjusts for slew & delay effects (not just scaling or delay)
  - Self checking process

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Summary and Conclusion

- Delta package simulation and time axis inverse linear transform (scale & delay) of typ column measurement data produces accurate die V-T tables
  - Each V-T table handled independently
  - Used for complex packages (device package plus measurement board test fixture)
  - Easy to program directly or with spread sheets
  - Typ data based time axis change gives "good" results for min and max columns
  - Min/max column time axis matching can be improved
- Examples show good correlation

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