[Driver Schedule]
Model Initialization

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My (stated/unstated) Driver Schedule Assumptions (in BIRD35.3)

- Under [Model], the model assumptions must prevail
  - Works for single transition and one cycle (Rising and Falling)
  - FULL CYCLE for [Driver Schedule]
    - Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly
    - x1 or NA x2 or NA x3 or NA x4 or NA
    - Full cycle => down-up (d-u), (u-d), (d-u-d-u), (u-d-u-d) sequencing for "slow" clock (no over-clocking considered or allowed)
    - 16 possibilities, but 5 [x || NA] table variations with 8 total variations considering numerical ordering, finite durations
  - Follows top-level [Model] "Polarity" Non-Inverting and Inverting modes ("phasing") in transparent manner
  - Everything is relative to Rise or Fall edges of "Master Clock"
- Therefore known initial state (High or Low) allowing single switch and one cycle simulation

Initial States (should be implemented for full capability)

R_on	R_off	F_on	F_off	Non-Invert	Inverting
xr	NA	xf	NA	Low	High
NA	xr	NA	xf	High	Low
x1	x2	NA	NA	Low	Low
x2	x1	NA	NA	High	High
NA	NA	x1	x2	High	High
NA	NA	x2	x1	Low	Low
xr1	xr2	xf2	xf1	Low	Low
xr2	xr1	xf1	xf2	High	High

Illegal Cases

R_on	R_off	F_on	F_off	Reason
NA	NA	NA	NA	unknown initial state
xr	NA	NA	xf	u-u sequencing
NA	xr	xf	NA	d-d sequencing
xr1	xr2	xf1	xf2	u-d-d-u sequencing
xr2	xr1	xf2	xf1	d-u-u-d sequencing

And just 1 or 3 numerical entries (sequencing)