The Benefits of Multi-Lingual Extensions to IBIS

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Agenda

- Simulation Limitations
- Advanced Modeling Capabilities
- Modeling Alternatives:
  - Altera Stratix GX High-Speed Serial Interface (HSSI)
- Conclusions

Simulation Limitations

- Model availability remains an issue
  - Proprietary models and languages limit industry mass adoption
- IBIS has major limitations; customers can't use it exclusively
  - Non-extensible syntax
  - Unable to model today's buffer technology
    - Adaptive drivers and receivers
  - Limitations in modeling power supply dynamics
- SPICE has issues as well
  - Too slow for analyzing entire design!!
  - Models often encrypted to proprietary formats
  - Vendors reluctant to provide the IP often found in SPICE models
- Additional engine limitations exist

Advanced Modeling Capability

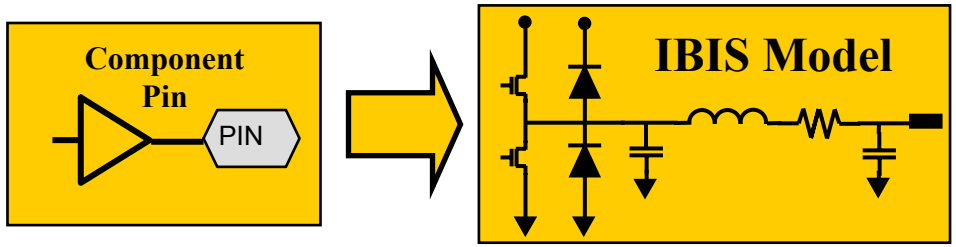
- Allow customers to use models in any possible industry standard format
  - There are different model formats and languages in use today for high-speed design
    - IBIS
    - SPICE
      - HSPICE, Eldo, PSpice, …
    - VHDL-AMS (IC level)
- By providing support for more than one, improve probability of finding a model
- Use the right model for the job at hand

Extensions to IBIS

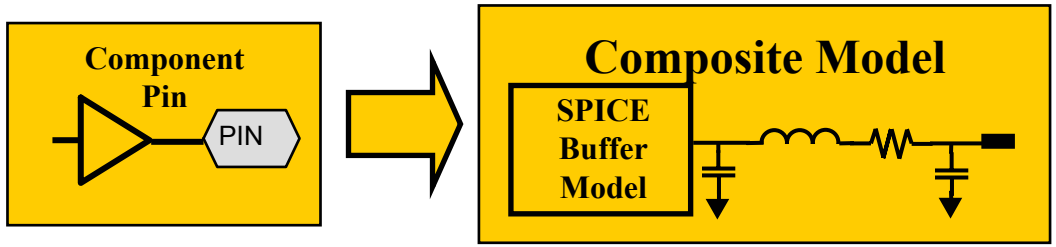
- **Allow IBIS models to reference external models through keywords**
  - **Standard language extensions**
    - **SPICE**
    - **VHDL-AMS**
  - **IBIS extensions**
    - **[External Model]**
    - **[External Circuit]**
    - **[Circuit Call]**
    - **[Node Declaration]**

I/O Buffer Examples

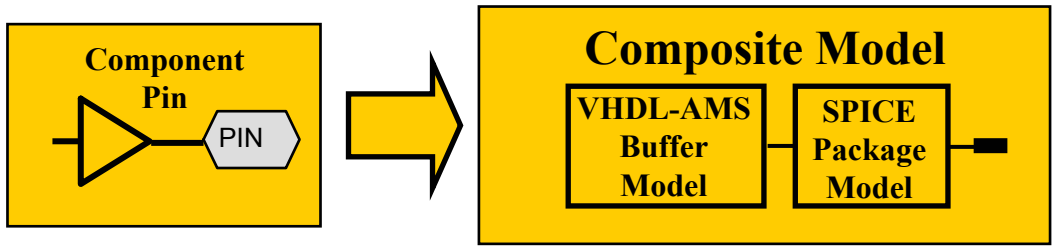
- **IBIS only**



- **IBIS Parasitics with SPICE Buffer**



- **SPICE Parasitics with VHDL-AMS buffer**



Multi-Lingual Simulation

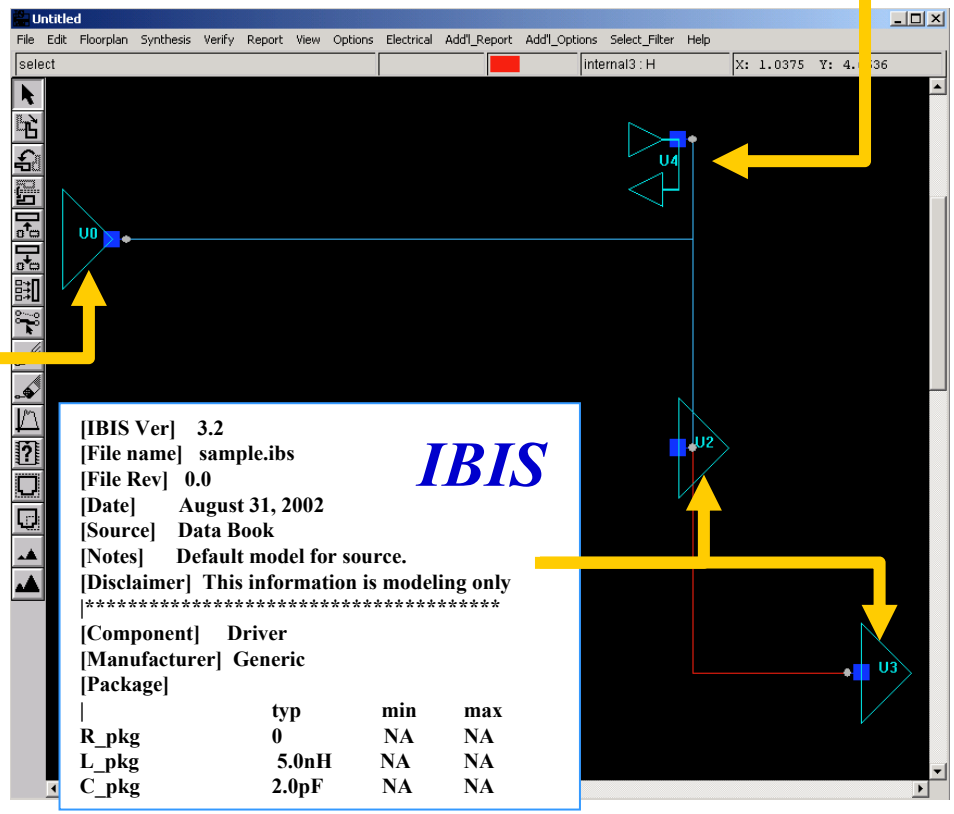
- **Mix and match driver model formats on a single net**

```
entity ibis_tx_cmos is
generic (
      c_comp:real:=7.0e-12;
      vpudata:real_vector:=( -5.250000e+00, … ,7.500000e+00);
      ipudata:real_vector:=( 3.555770e-01, … ,-1.356870e-01);
            … same for vpd, ipd, vpc,ipc, vgc, igc
```

VHDL-AMS

```
R_I$277 VCC out1 1.55K
C_I$272 ibias N$238 28.3P
M_I$46 N$240 ibias 0 0 NFET L=1.52U W=7.85U M=40
M_I$283 out2 out2b VCC VCC PFET L=0.5U W=4U M=1
.MODEL NFET NMOS (RSH=17 KP=1.34M
+ GAMMA=0.919 PHI=0.707 LAMBDA=0.1M RD=52.88
+ RS=52.55 CBD=4.79P CBS=5.73P PB=1
+ CGSO=3.17P CGDO=2.04P CGBO=4.01P MJ=0.189 )
...
```

SPICE



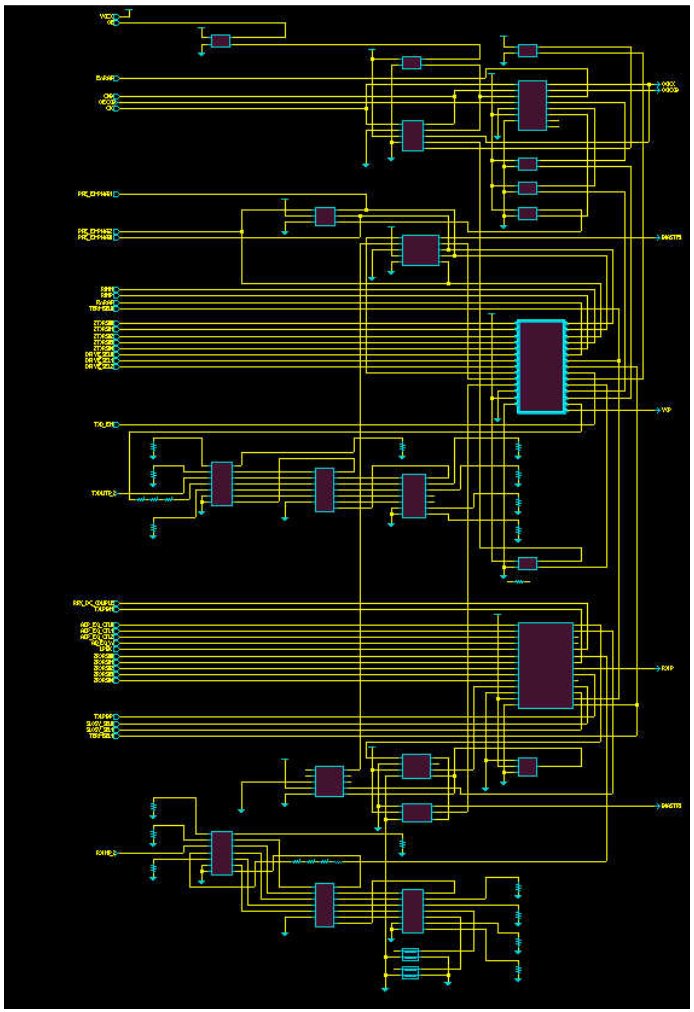
IBIS

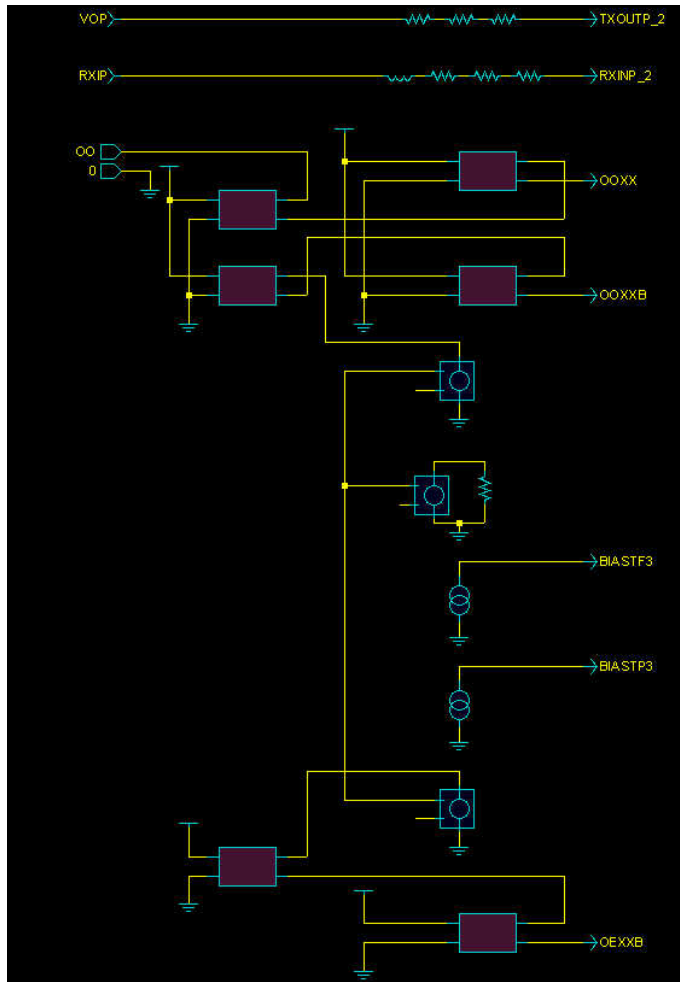
```
[IBIS Ver]    3.2
[File name]   sample.ibs
[File Rev]    0.0
[Date]        August 31, 2002
[Source]      Data Book
[Notes]       Default model for source.
[Disclaimer]  This information is modeling only
|*************************************
[Component]   Driver
[Manufacturer] Generic
[Package]
|              typ      min     max
R_pkg          0        NA      NA
L_pkg          5.0nH    NA      NA
C_pkg          2.0pF    NA      NA
```

Modeling Alternatives: Starting Point

- Altera Stratix GX High-Speed Serial Interface (HSSI)
  - SPICE transistor level model
  - Single circuit for transceiver
  - Selectable parameters for Driver pre-emphasis levels, Driver output voltage amplitude, Driver impedance, Receiver equalization level, Receiver impedance, Trace length and loss
- 3” lossy differential pair trace model from driver pins to receiver pins
- Circuit as delivered took 21 minutes (real time) to simulate in Eldo (SPICE)

Original Transceiver Model





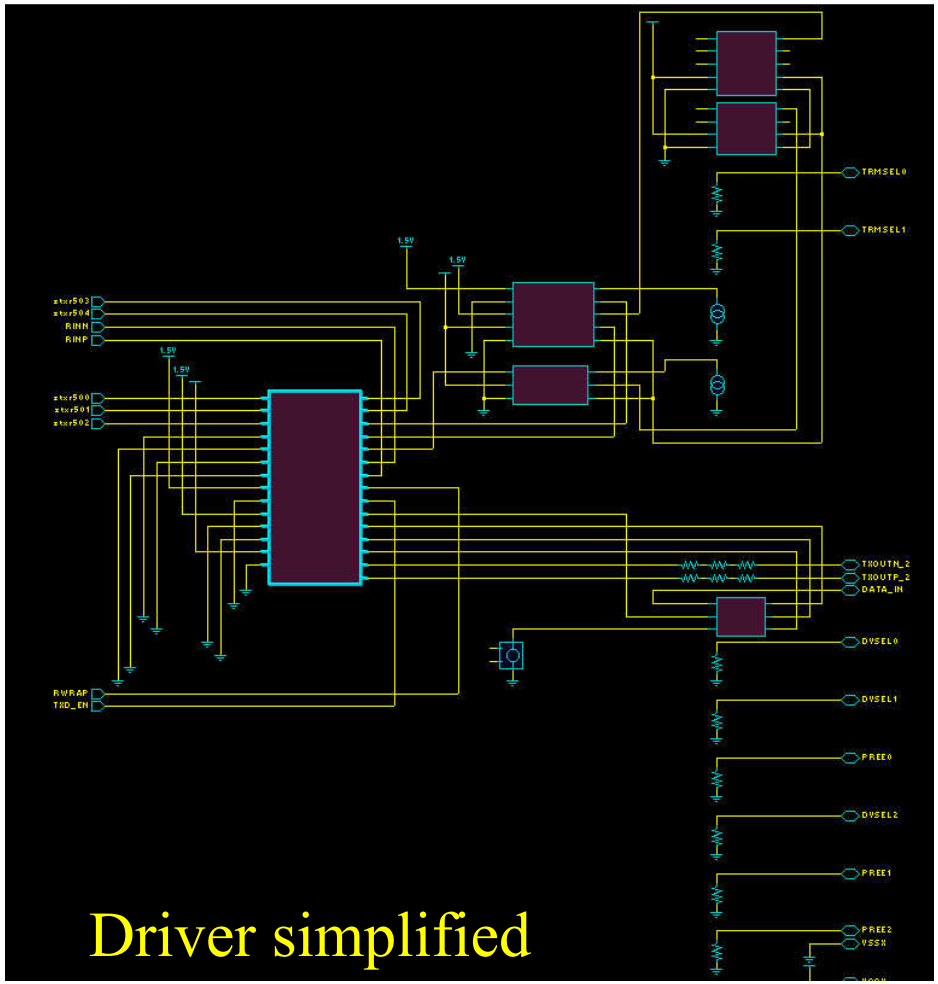
Multi-page schematic created with SpiceVision PRO from Concept Engineering

Issues with SPICE Models

- **Can't simulate Driver separate from receiver**
  - **Probably simulating extra nodes that are irrelevant**
- **Subcircuits encrypted (Eldo)**
- **Global nodes (.global in SPICE)**
  - **Possible conflict with models from another source**
- **Scale option = 1u**
  - **Another possible conflict with other models**

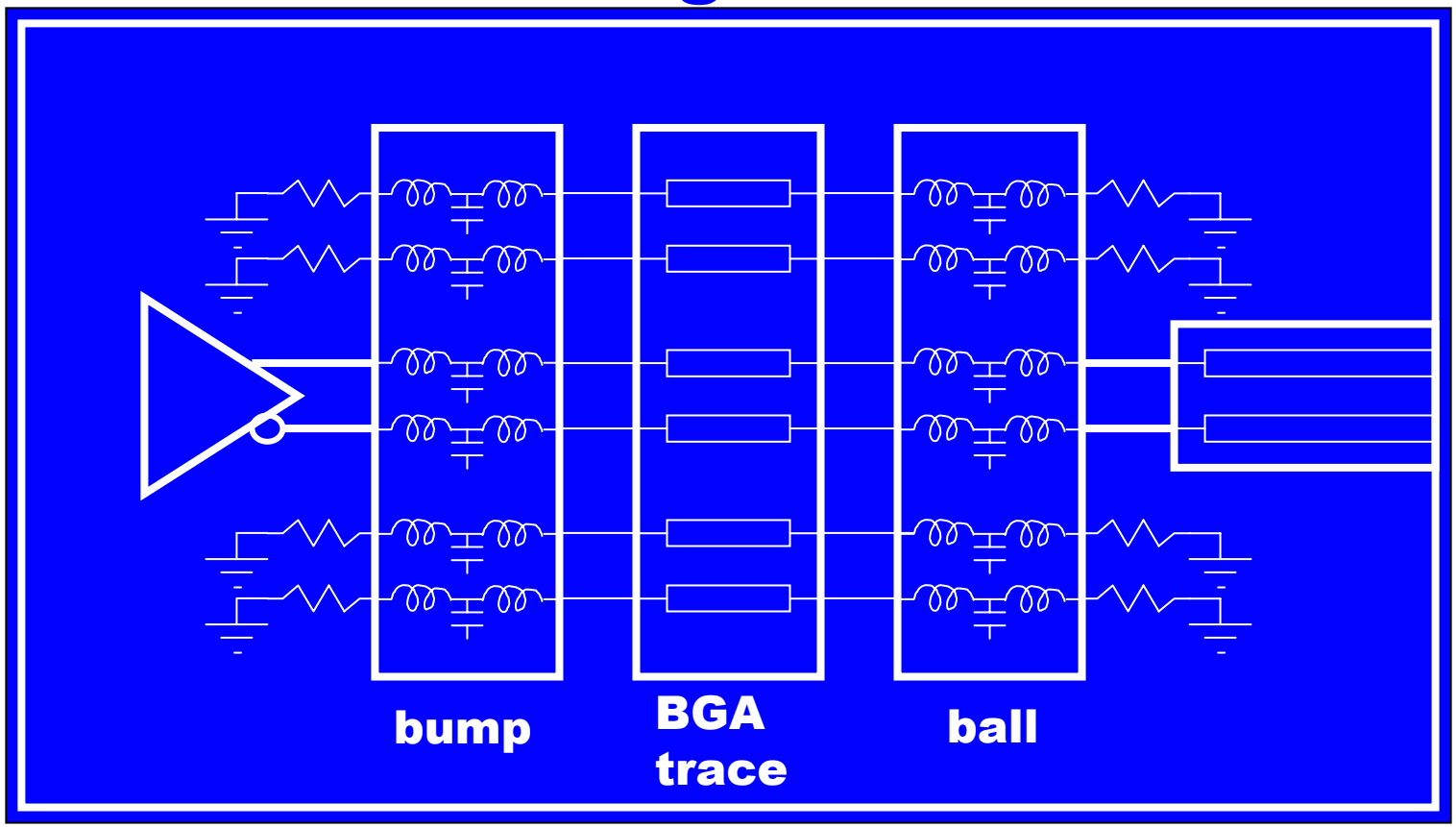
* These are common issues with SPICE models *

Transceiver Model Reduction



- **Driver and Receiver sections separated**
  - **Allows instantiation of driver and receiver IBIS 4.1 models on separate parts for design verification**
- **Driver section reduced**
  - **Data and pre-emphasis signal generation simplified with controlled-source logic**
- **Simulation time reduced to 12 minutes real time – 57% of original time**

Package Model

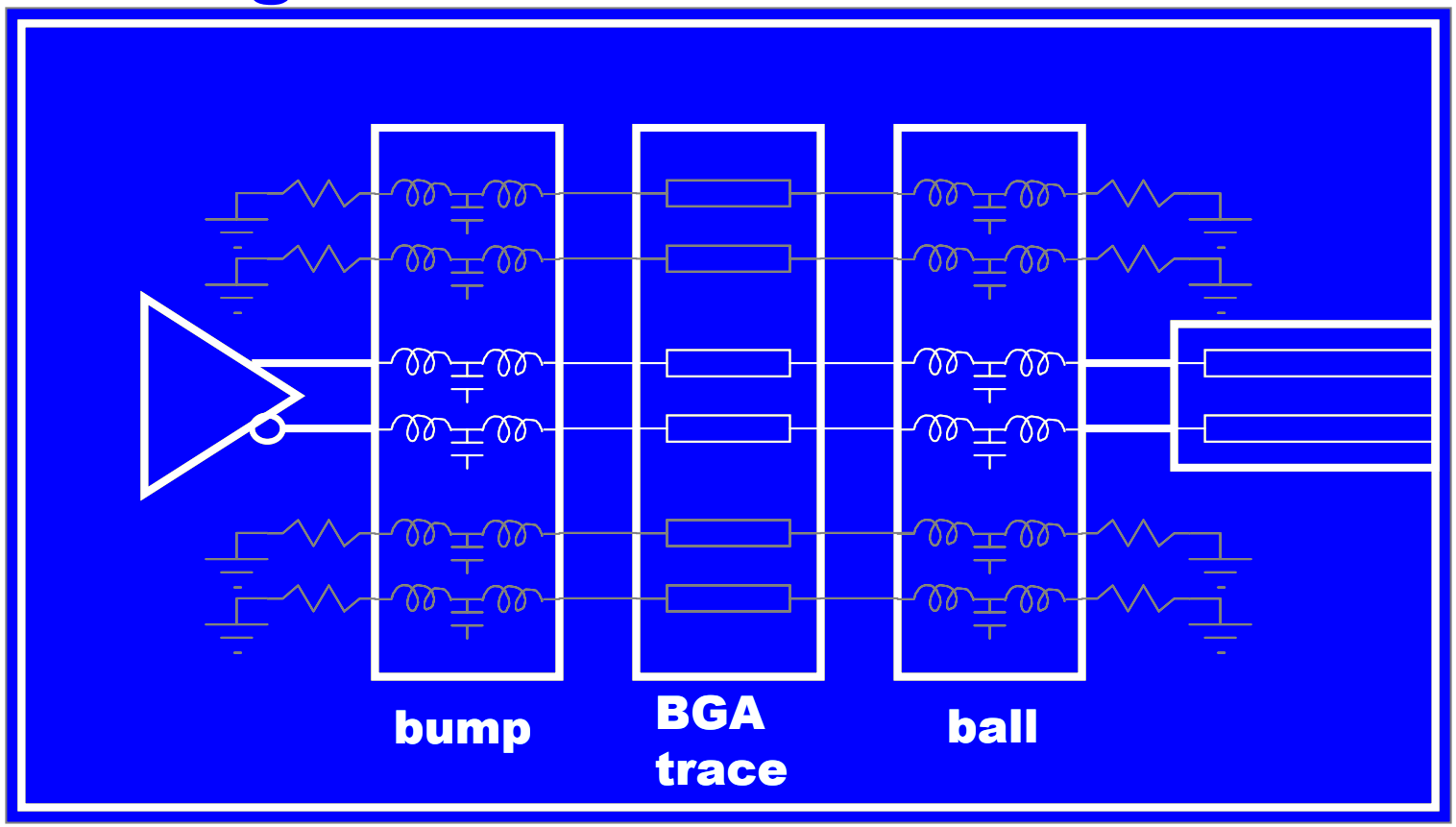


- Complex package model
  - 3 differential pairs fully coupled
  - 3 cascaded sections

Package Model Reduction

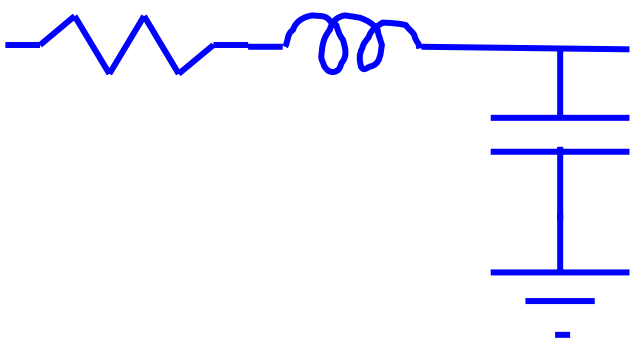
- **Element elimination**
- **Simple IBIS RLC parameters**
- **S-parameter model**

Package Model Element Elimination



- Reduced simulation time by about 10%
- Changed results beyond acceptable error

Simple IBIS RLC Parameters



$L = T_d * Z$

$C = T_d / Z$

T_d measured from original simulation is 83ps (Tr ~ 200ps)

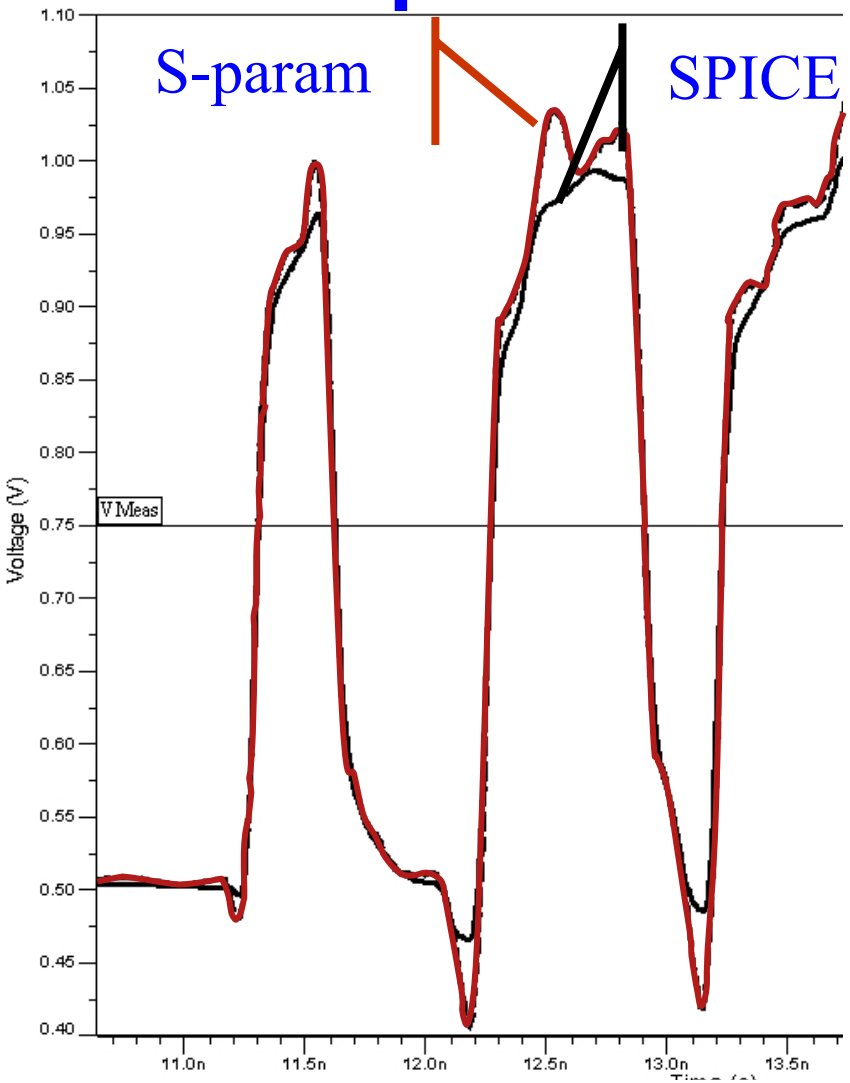
Assume Z_0 is 50Ω

$L = 4.15nH$

$C = 1.66pF$

- **Can't be more accurate than reduced element model**
- **Should provide much faster simulation time**
- **Reduced simulation time by 25%**
- **Reduced overshoot**
  - **Assumed impedance of 50 Ohms was better than original SPICE model**

S-parameter Package Model

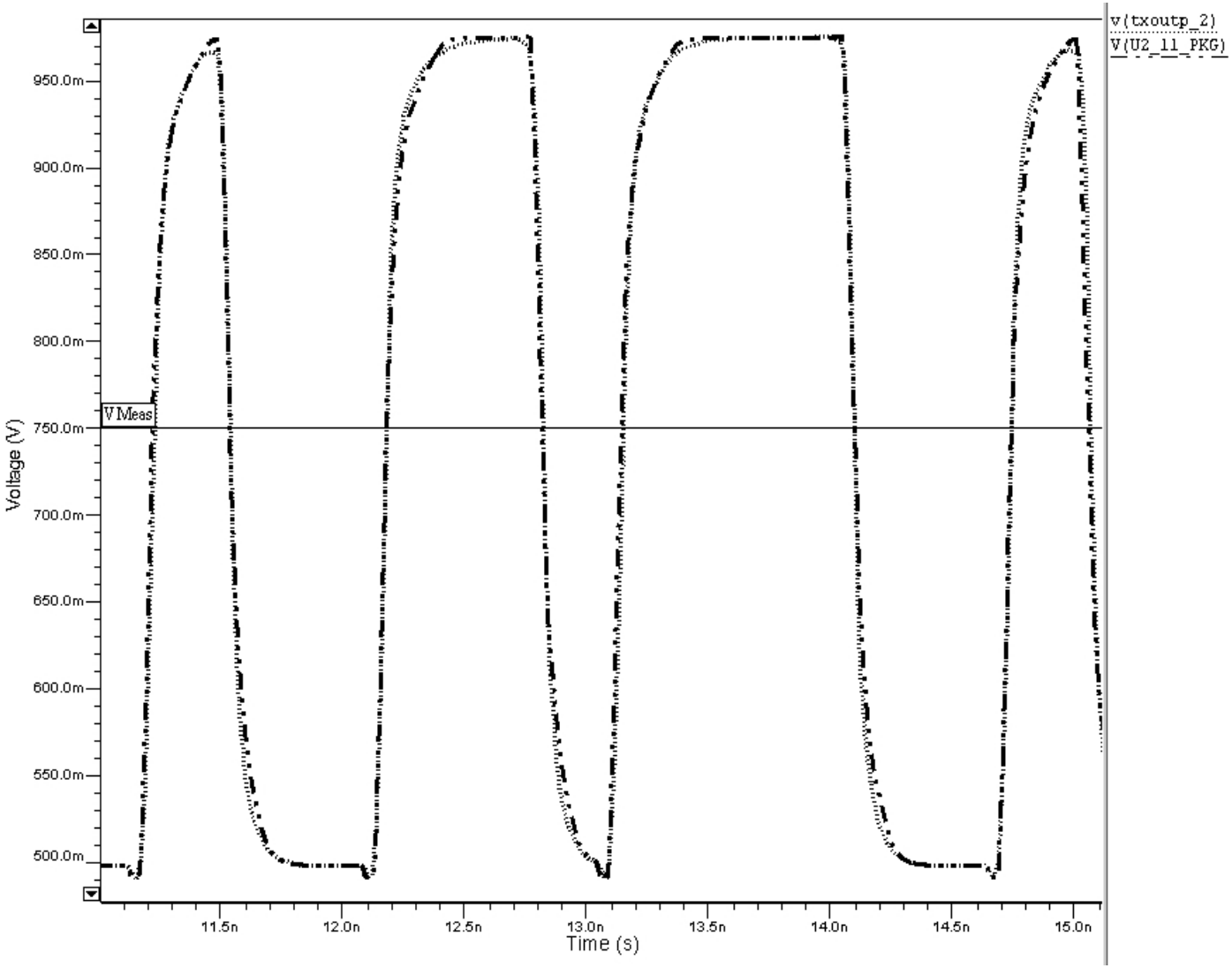


- **S-parameter set created by SPICE simulation of original package model**
  - **Frequency steps of 100MHz from 100MHz up to 10GHz**
- **Simulation time reduced by 25% from full package model simulation**
- **S-parameters have other issues**
  - **Usually no DC information**
  - **Possible non-causal or non-passive results**

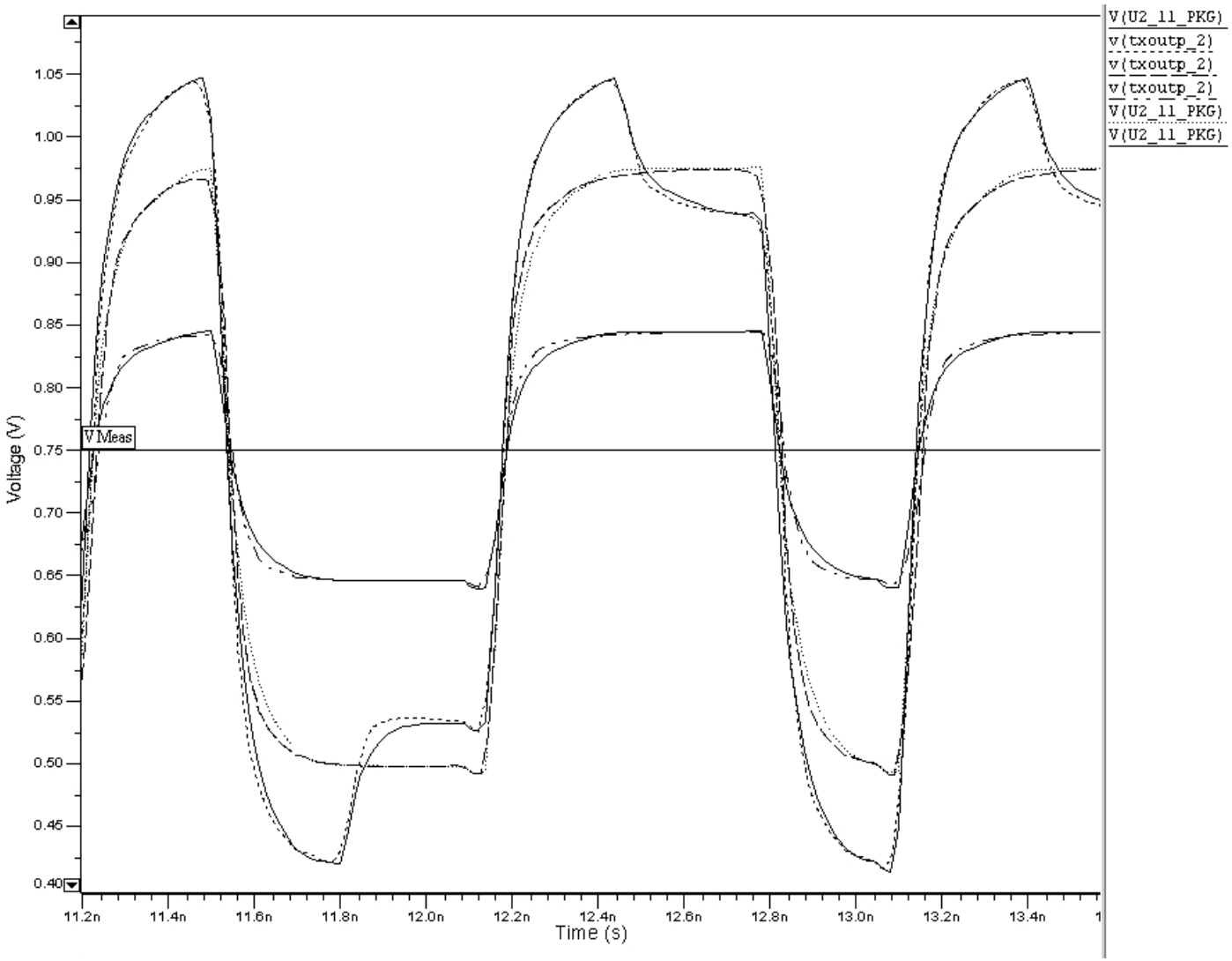
Behavioral Modeling

- ***Functionality and accuracy must be maintained!***
- **Majority of simulation time is spent solving the 1000's of nodes in the transistor level transmitter and receiver models**
- **This time could be greatly reduced by using behavioral models such as VHDL-AMS**

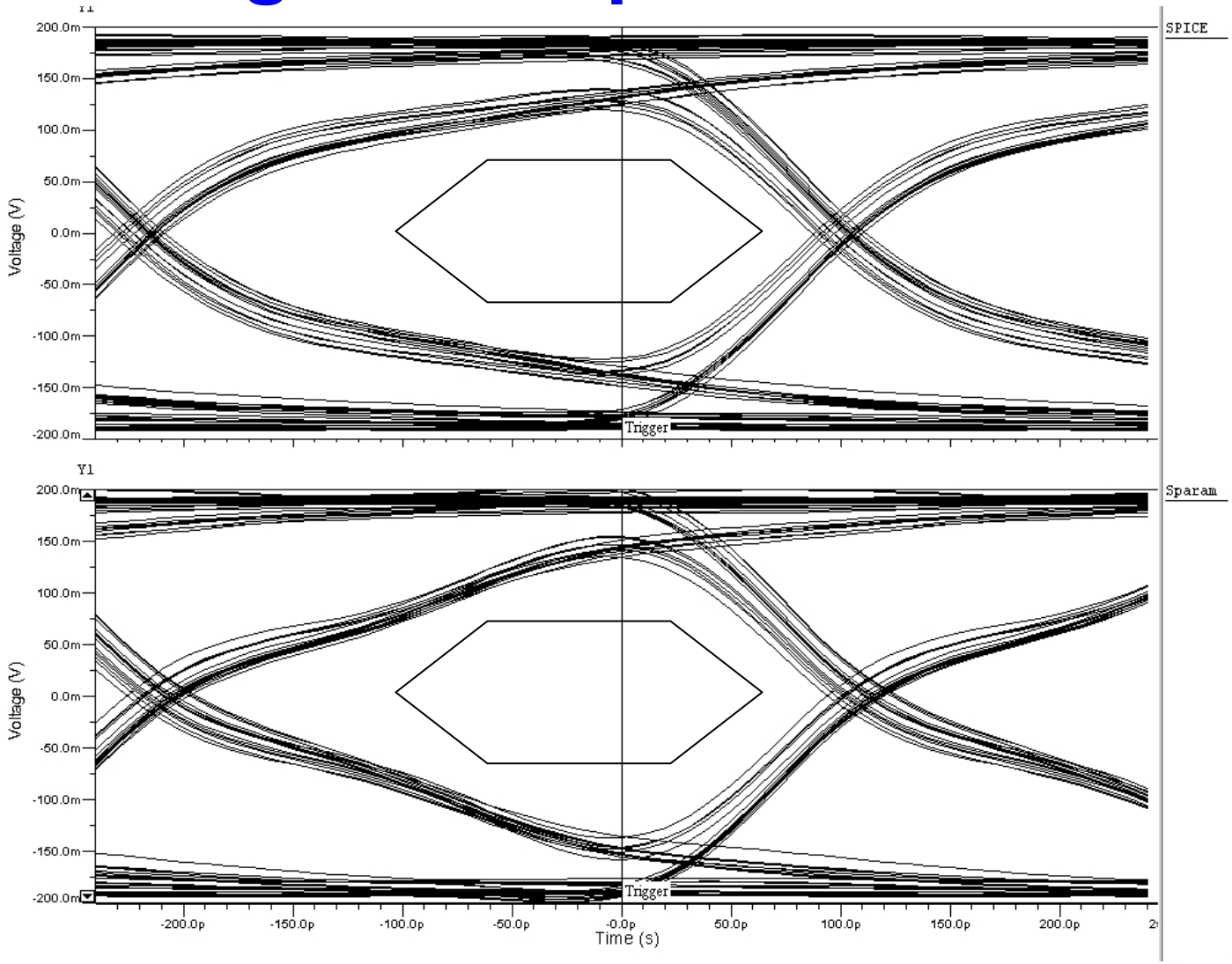
VHDL-AMS Model Correlation



VHDL-AMS Model Functionality



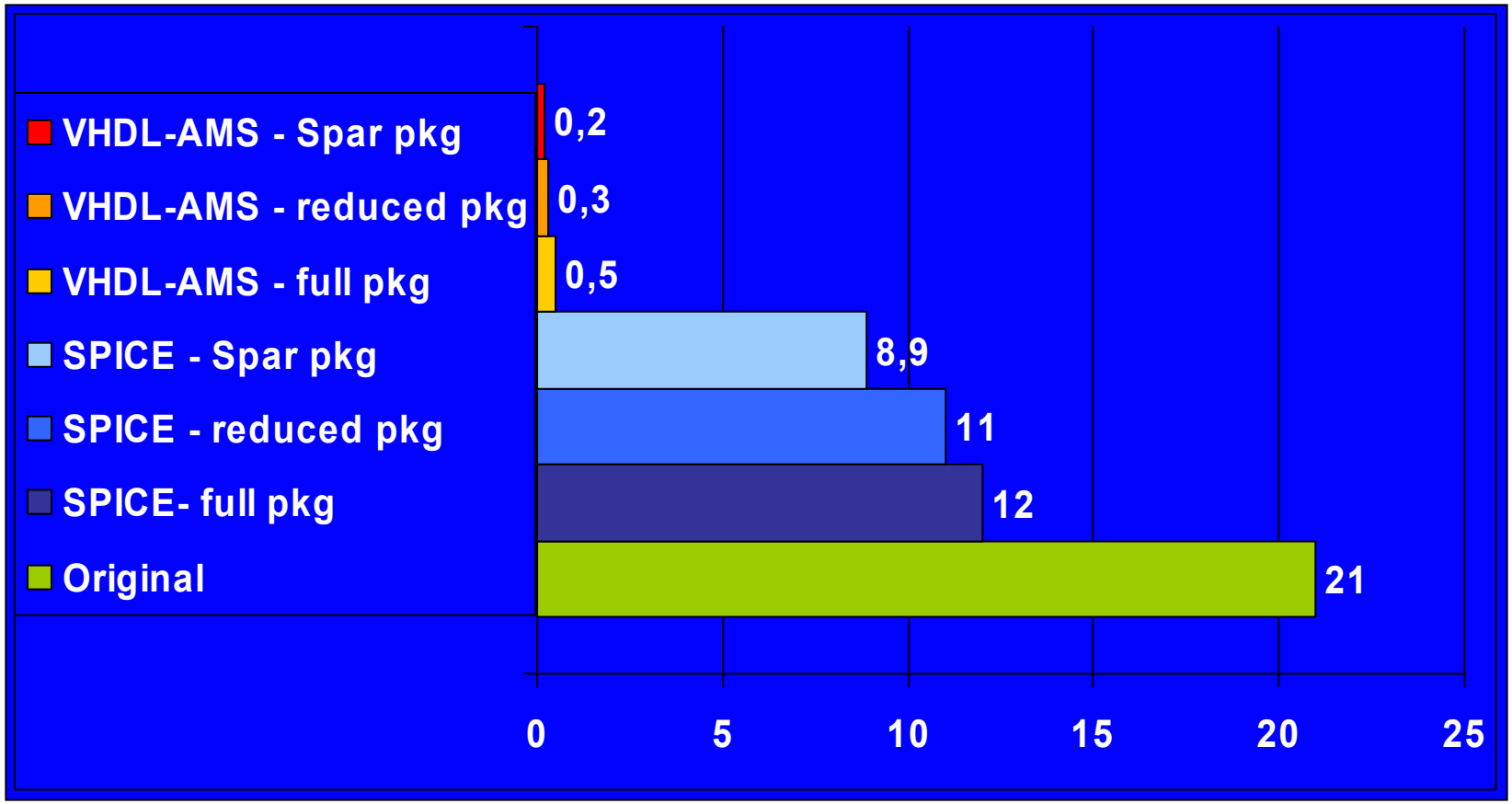
Signal Comparison at the Receiver



SPICE package

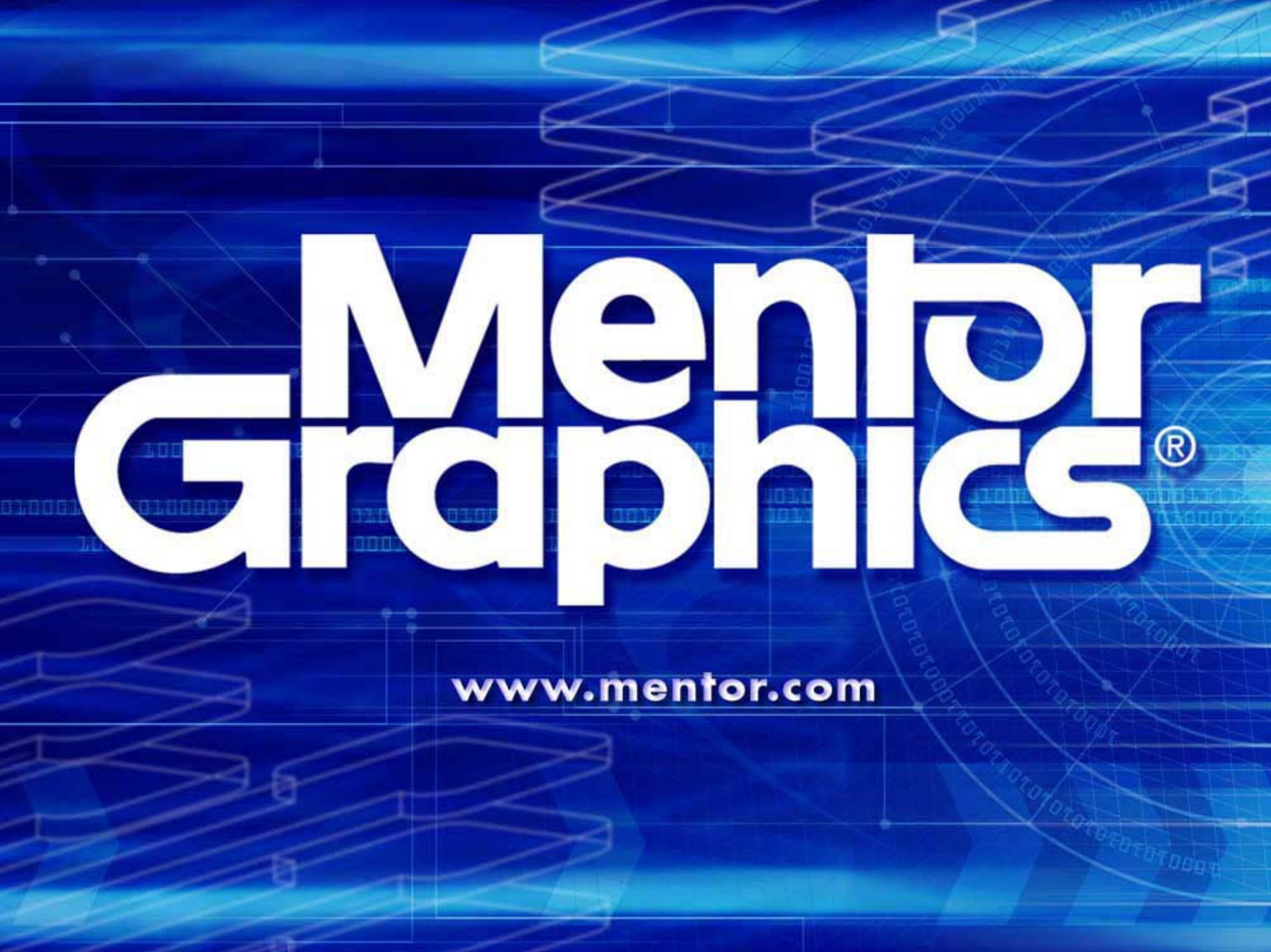
S-param package

Simulation Time Reduction



Conclusions

- The SPICE model can be reduced to save simulation time
- The package model can be translated to other formats to save some simulation time, but doesn't justify the change in results.
- Using a behavioral model of the driver and receiver drastically decreases simulation time to less than 1/10 and maintains fidelity to the original results
- Extensions to IBIS and Multi-Lingual Simulator provide flexibility and performance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