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Use of IBIS models at Alcatel

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Topics

- Managing IBIS models
- Verifying IBIS models
- Short-cuts for model creation
- Extracting design information from models
- IBIS models in ASIC design cycle
- Conclusion

Managing Models

- Common file system for CAD tools and Web server
- Web based interface
  - to upload, cretae and edit models
  - to verify models
  - to extract design information
- Both buffer and component libraries
- IBIS parser written in Perl

IBIS Web Tools

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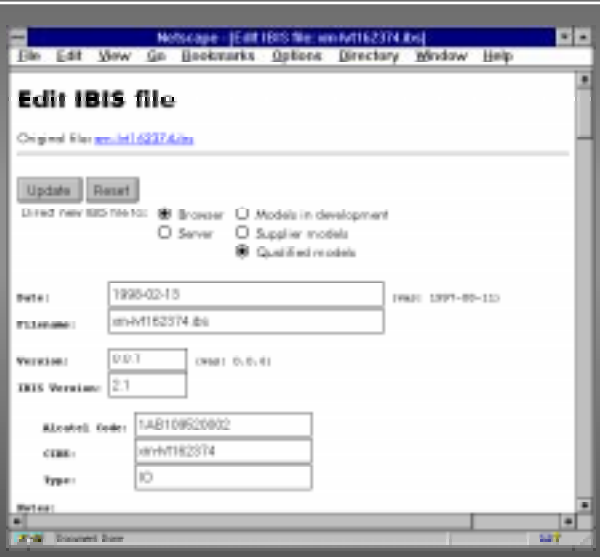
Editor 1/2



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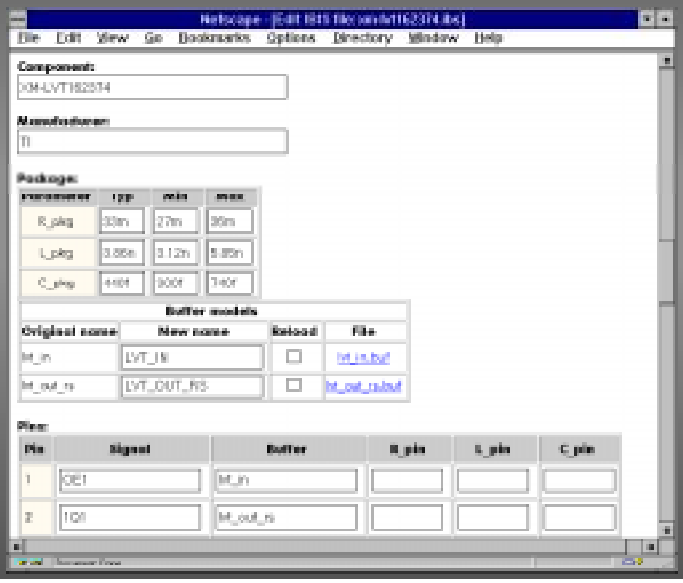
Editor 2/2



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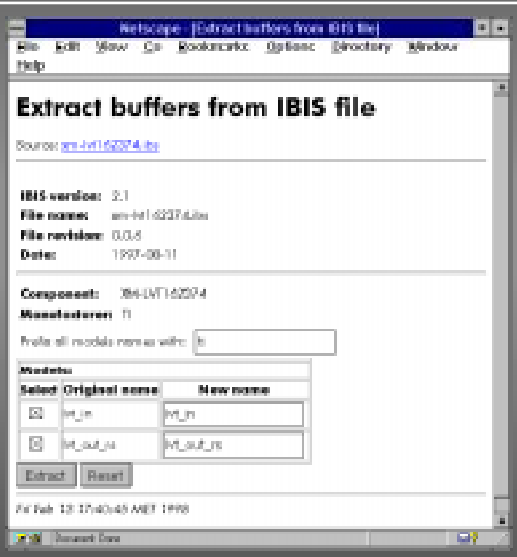
Extract buffers



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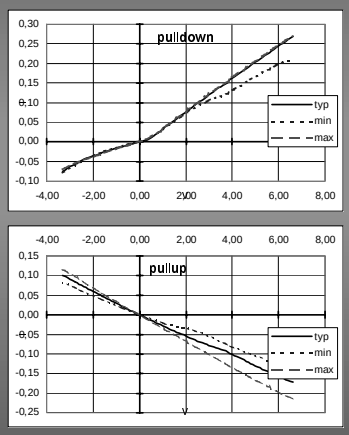
Verifying Models

- ibischk2 + additional checks
- Component header information
- Calculate attributes
- Visual inspection of curves
- No simulations!
- No measurements!

Graphical datasheet

- No good tool graphical tool to visualise the model.
- Experiments with Excel and Visual Basic.
- Add clamp curves together, or with pullup or pulldown, to get real response!
- Filter out superfluous data like huge clamping currents.



Short-cuts for model creation

- What do you do if you can't get a model?
  - Extract pin list from CAD symbol
  - Figure out buffer types from datasheet
  - Use a buffer from a similar component...
  - take a guess at Vcc, Icc and Trise
- In many situations, results obtained with these models are good enough.
- Not recommended for novices.

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IBIS BufferMaker

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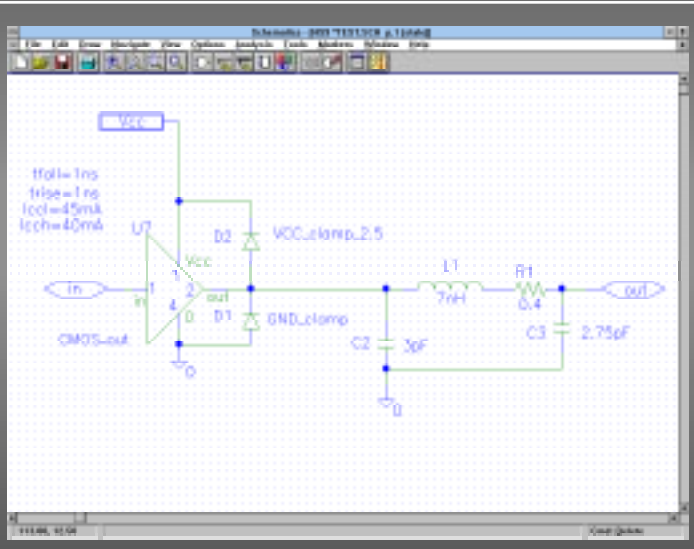
Generic behavioral model



Extracting design information

- Simulation can be time consuming.
- Condense information of IBIS file for use in design rules:
  - Output impedance *(what value series resistor?)*
  - short-circuit current
  - clamping diodes *(can I interface from 5V to 3V directly?)*
  - critical length *(when do I need to terminate?)*
  - Pull-up and bus-hold inputs.
- Example: crosstalk rules

Attributes

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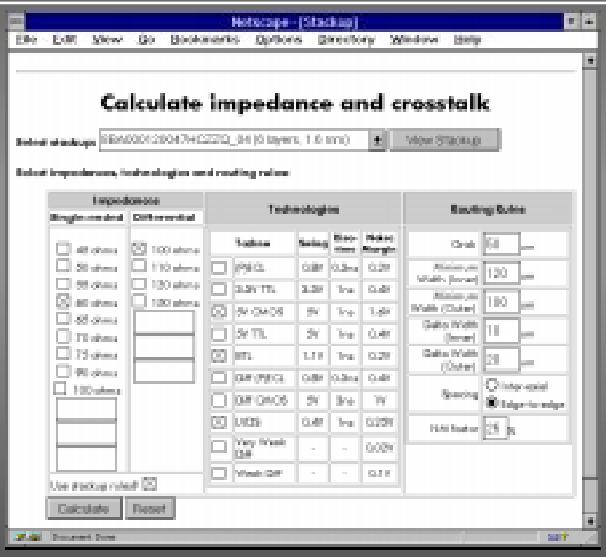
Crosstalk: info



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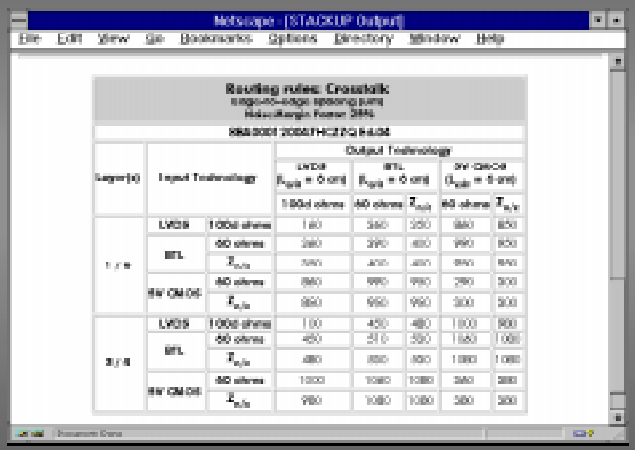
Crosstalk: rules



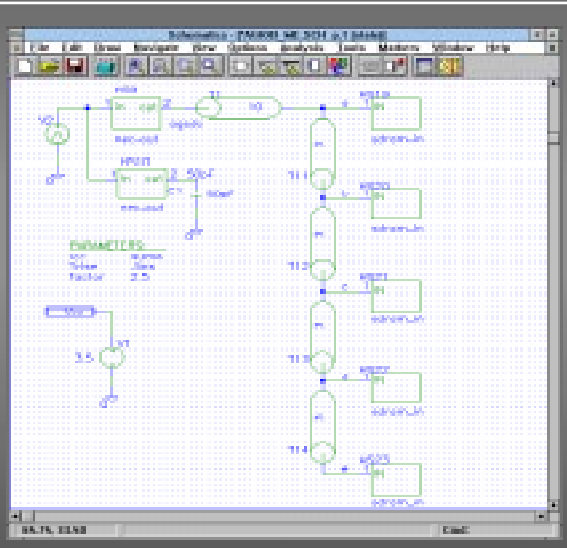
ASIC support

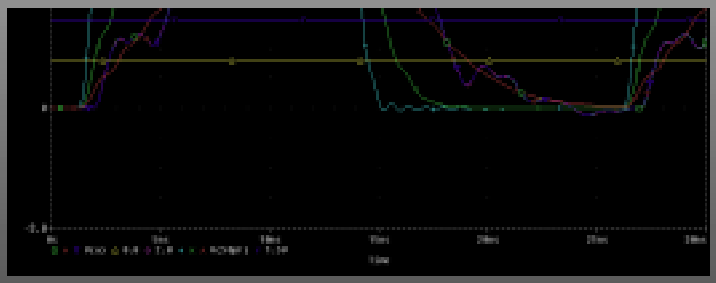
- Alcatel contract with its Asic suppliers specifies that an IBIS library must be available, but reality is different.
- IBIS standard and tools not intended for library files
  - pin information less important
  - differential buffers cannot be treated independently of pins
- IBIS Package models not readily available. Extra support needed from IBIS community?

ASIC design cycle (2/2)

- IBIS Library used to choose buffer strengths
- Difficult to allocate timing budget
  - Impossible isolate on-chip and on-board timings.
  - ASIC simulators require a fixed C_{load} to represent the actual load, which of course is not capacitive!
  - What voltage level for timing measurements? Vt or Vih/Vil?
- IBIS models not suited to ground bounce simulation. Can anything be done?

Buffer Strength (1/2)



Buffer Strength (2/2)

Propagation Time