ECALS/JEITA

新電元

To be model of Circuit Simulation

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IBIS SUMMIT at Santa Clara

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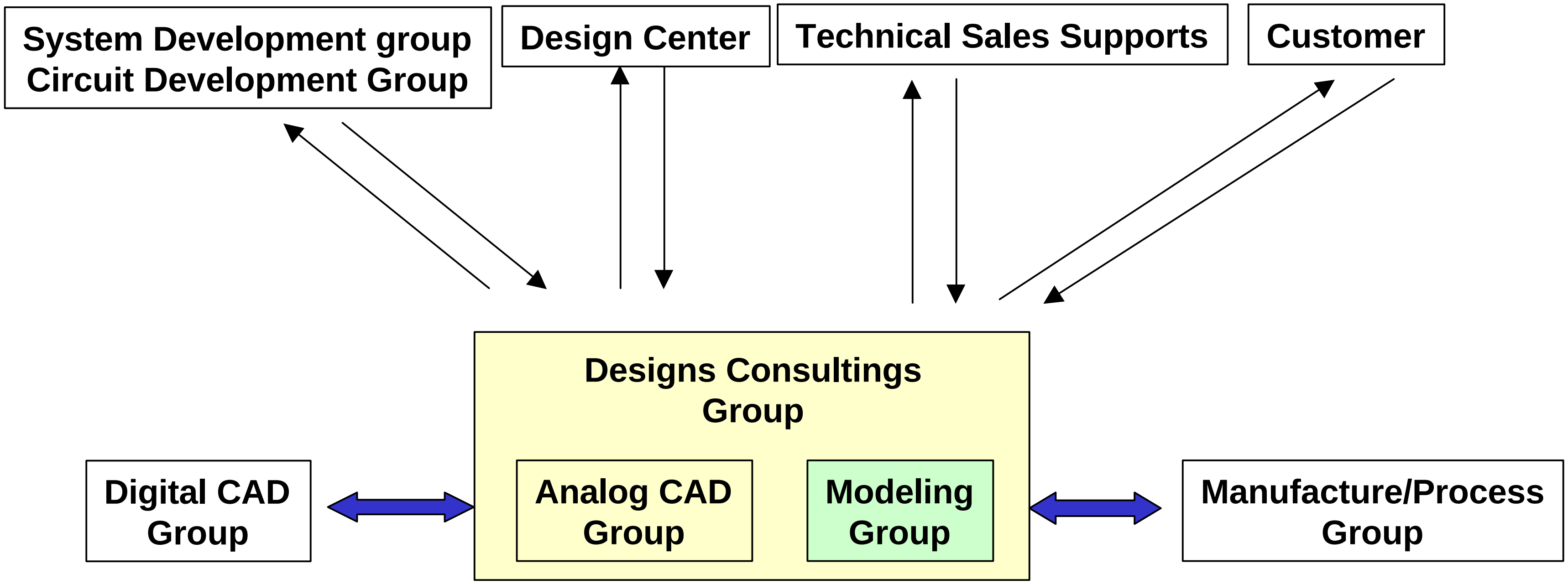
To be model



Time to Market

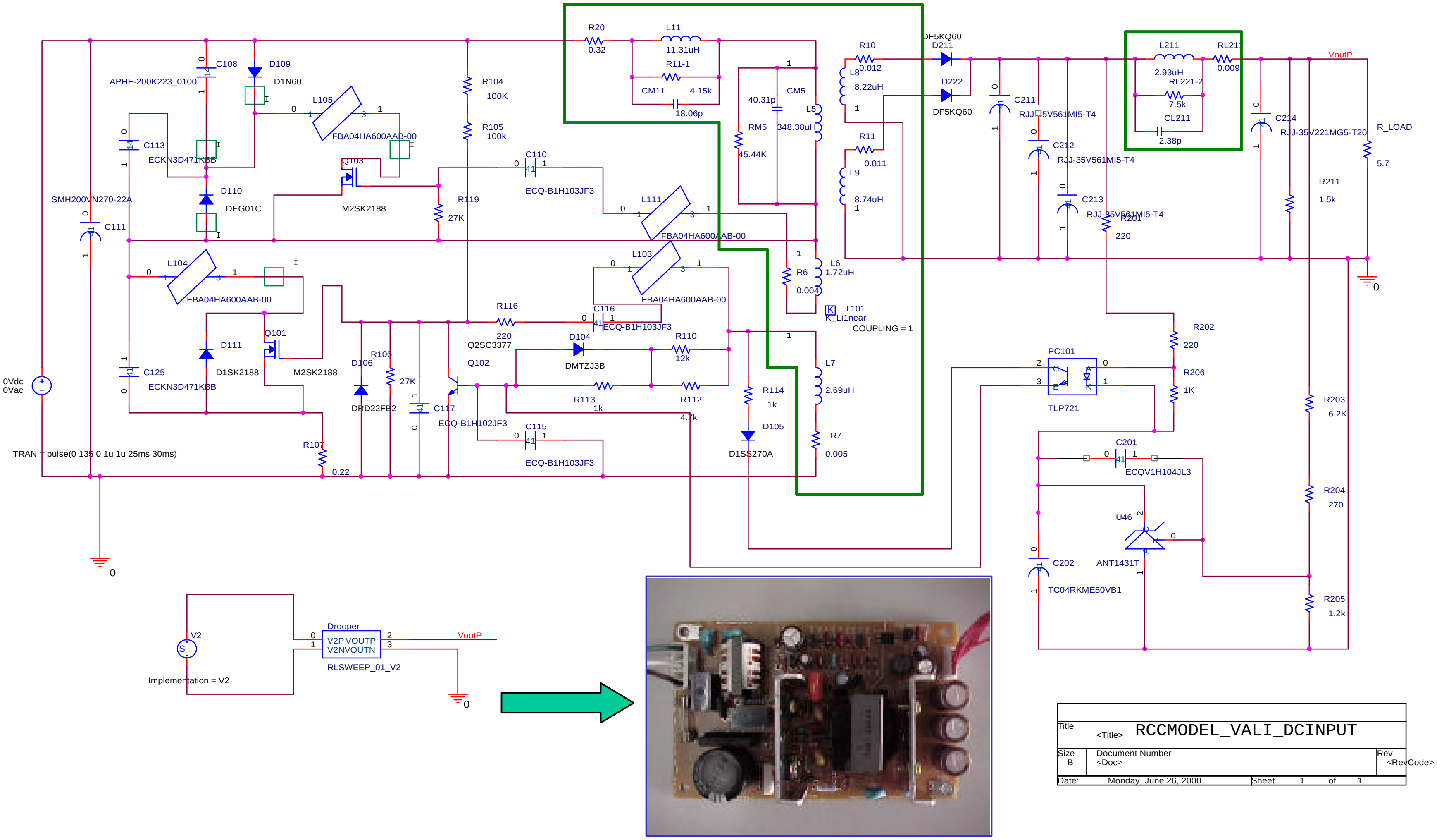
?Circuit Simulation(Thermal Model,Noise Model)

?Easiness of obtaining EDA MODEL,Design Kit and Development of Device Modeling Technology

Unified design environment (Digital,Analog,High frequency) *including EDA MODEL*

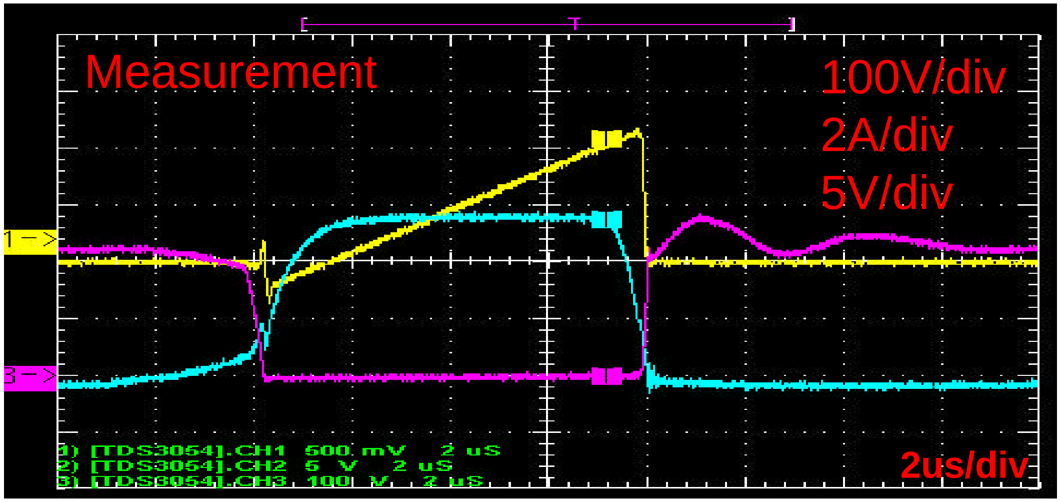
As is model

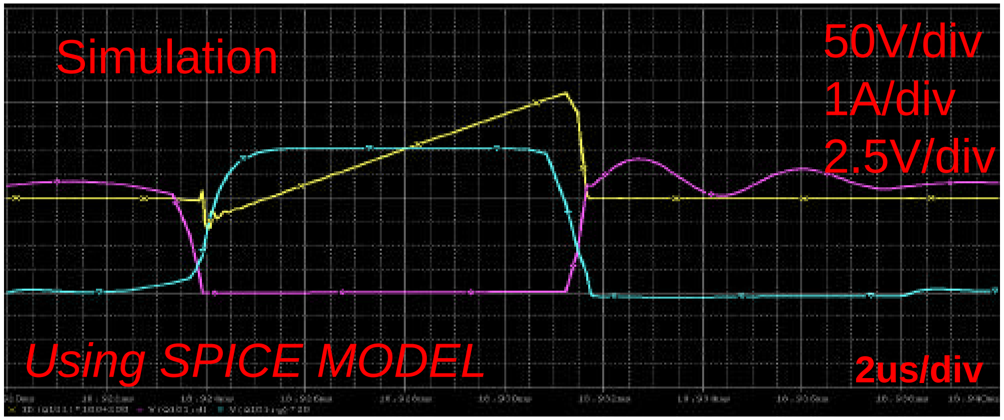
Circuit Simulation(SPICE MODEL) ?Trial Product



Comparison of shapes of waves

Vds, Id, Vgs(Q101)





An analytical consequence is good. *but it took circuit designer a lot of time to obtain EDA MODEL(SPICE MODEL).*

Proposal

Unified design environment (Digital,Analog,High frequency)
including EDA MODEL

Expansion of Electronic parts of IBIS and IBIS-X

Example

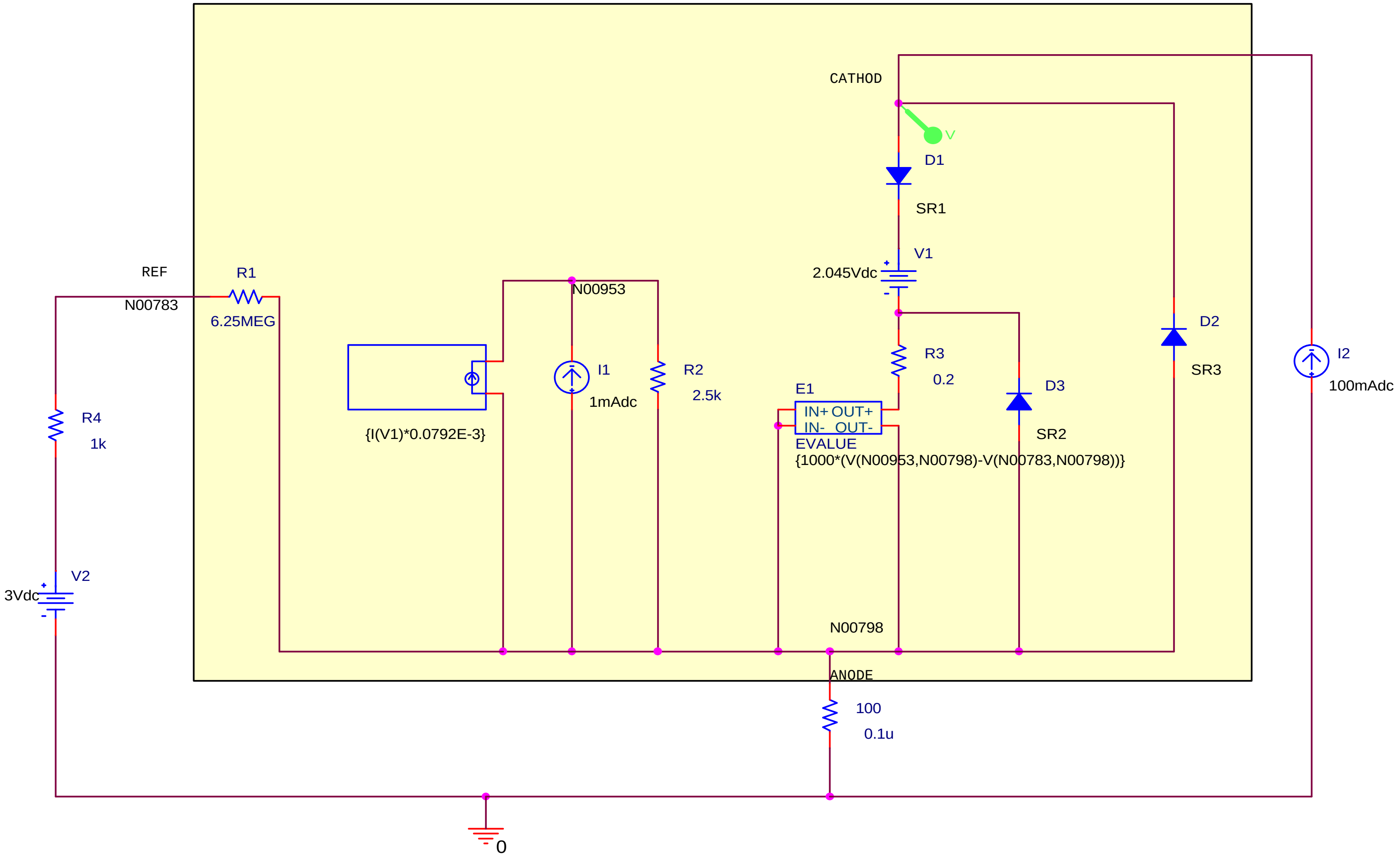
Analog IC
Photocoupler

SPICE MODEL
(Equivalent circuit)

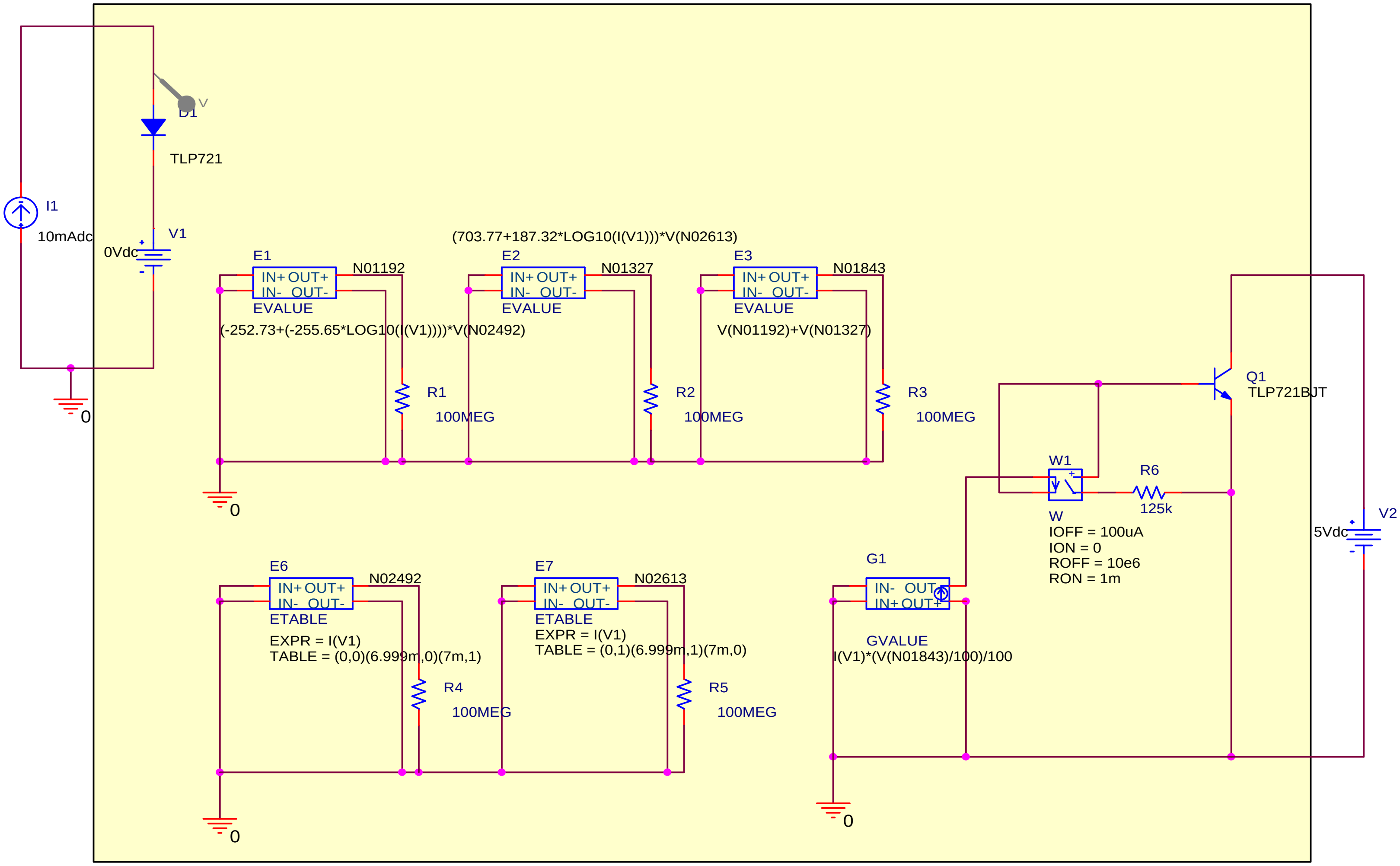
Analog IC
Photocoupler

IBIS-X
(Using Macro language)

Example:
Analog IC(Shunt Regulator): SPICE MODEL(Equivalent circuit)



Example:
Photocoupler : SPICE MODEL(Equivalent circuit)



We want to aim at the unified design environment (Digital,Analog,High frequency) *including EDA MODEL* and the environment of easiness obtaining *EDA MODEL*.