A BIRD 75 Multi-lingual Example

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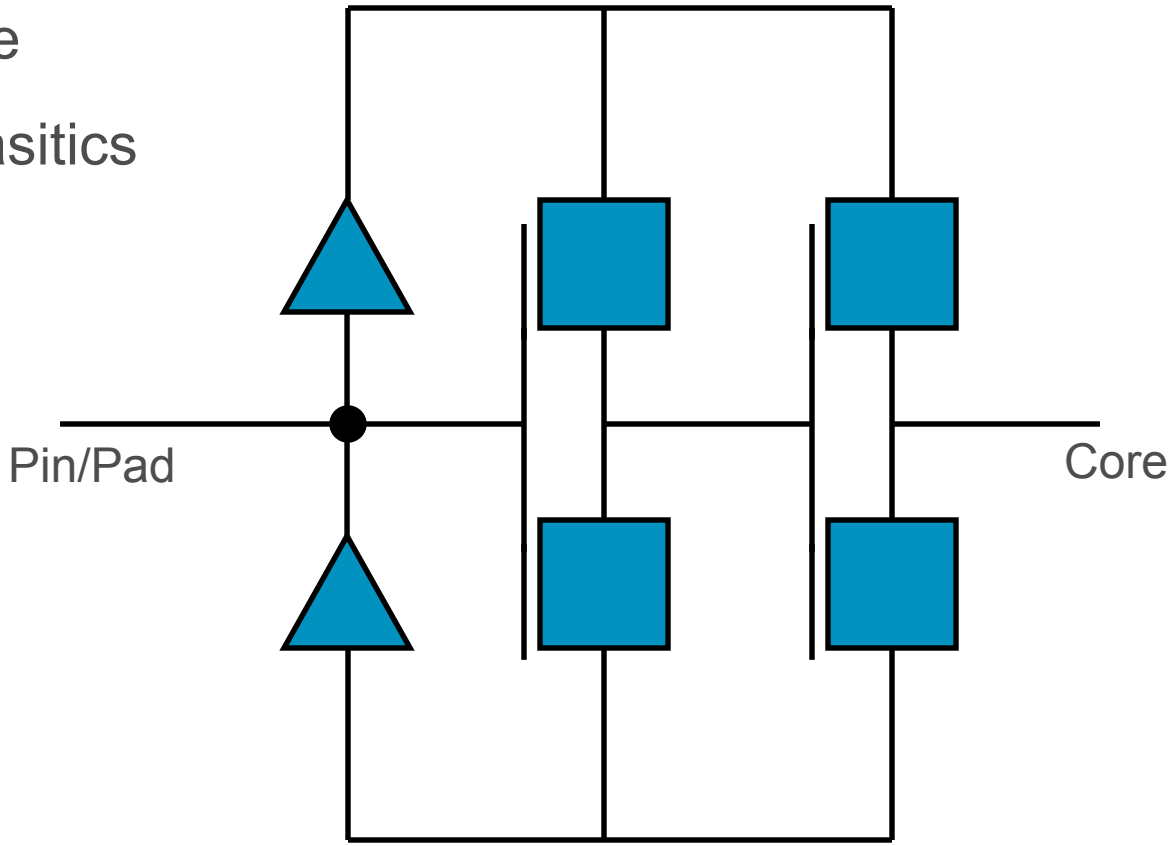
Multi-Lingual Example

- Simple receiver
- SPICE
- VHDL-AMS
- Calling in IBIS 4.x File

Simple Receiver

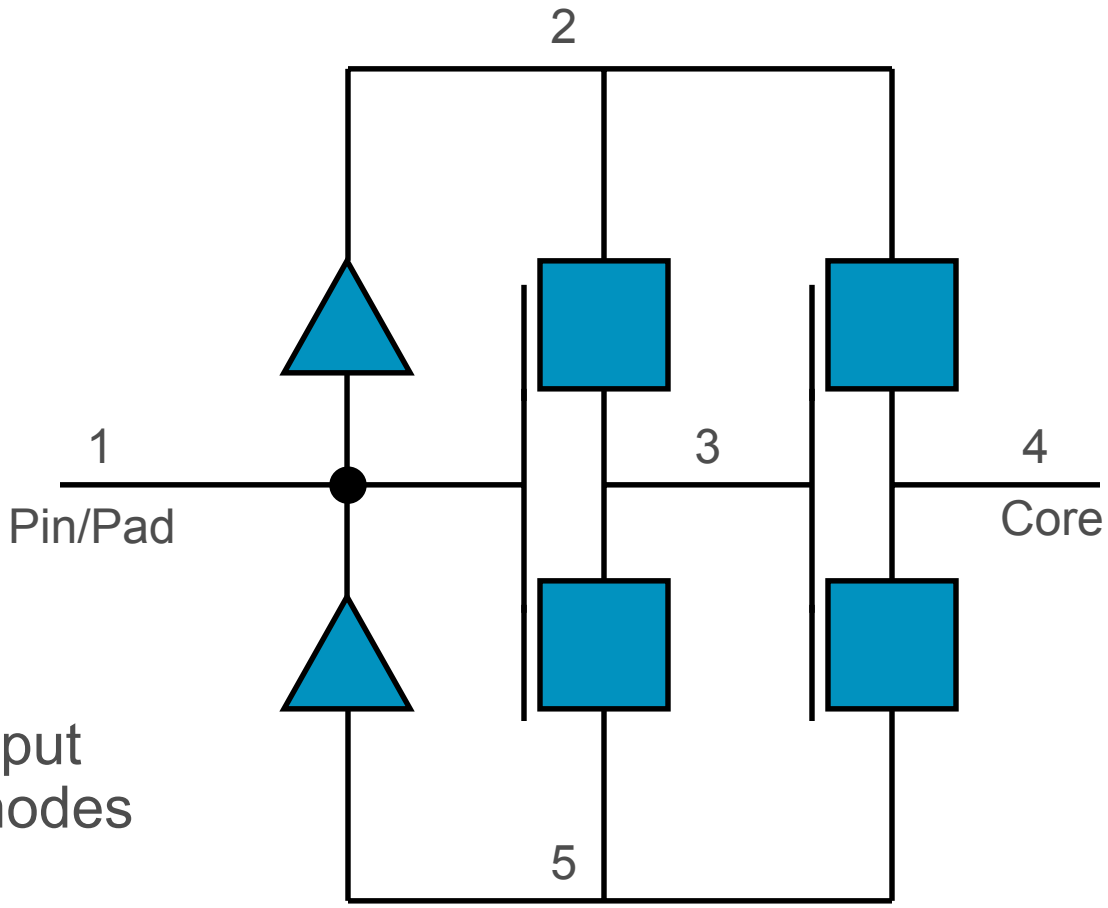
- Pair of clamp diodes
- Input capacitance
- No package parasitics



Simple Receiver in SPICE

```
.subckt Rcvr 1 2 4 5
D1 1 2 DD
D2 5 1 DD
M1 1 3 2 2 P
M2 1 3 5 5 N
M3 3 4 2 2 P
M4 3 4 5 5 N
.model DD d Cj0 2p
.model N nmos
.model P pmos
.ends
```

Analog input and output
KCL and KVL at all nodes



Simple Receiver in VHDL-AMS

```
Library IEEE;
use IEEE.math_real.all;
use IEEE.std_logic_1164.all;
library IEEE_proposed;
use IEEE_proposed.electrical_systems.all;
use IEEE_proposed.energy_systems.all;

entity Rcvr is
  generic(
     TempC : real := 25.0;
     cap : capacitance :=2.0e-12;
     Vinh :voltage :=2.0;
     Vinl : voltage :=0.8);
  port (terminal v_pad, v_pwr, v_gnd :
  electrical;
        signal core : out std_logic);
end entity Rcvr;
```

KCL and KVL only at analog nodes

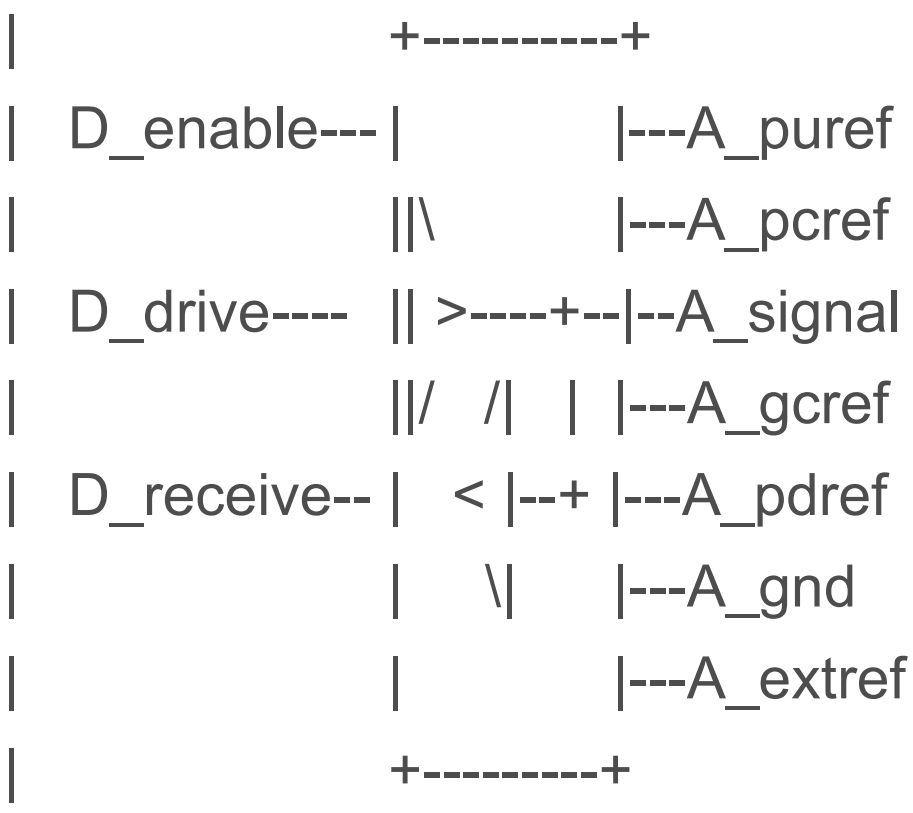
Simple Receiver in VHDL-AMS

```
architecture linear of Rcvr is
  constant vt : real := K*(TempC + 273.0)/Q;
  constant isat : current := 1.0e-15;
  constant delay1 :time :=3.5 ps;

  quantity v_cap across i_cap through v_pad to v_gnd;
  quantity v_gc across i_gc through v_gnd to v_pad;
  quantity v_pc across i_pc through v_pad to v_pwr;

begin
```

Simple Receiver in VHDL-AMS

```
process (v_cap'above(Vinh), V_cap'above(Vinl)) is
   begin
      if  v_cap'above(Vinh) then
         core <= '1' after delay1;
      elsif not v_cap'above(Vinl) then
         core <= '0' after delay1;
      else
         core <= 'X' after delay1;
      end if;
end process;

i_cap==cap*v_cap'dot;
i_gc == isat*(exp(v_gc/vt) - 1.0);
i_pc == isat*(exp(v_pc/vt) - 1.0);
end architecture linear;
```

Calling the External Model



Calling the SPICE Model

```
[Model] ExBufferSPICE
Model_type Input
Vinh = 2.0
VinI = 0.8
[Voltage Range]   3.3     3.0    3.6
|
[External Model]
Language SPICE
Corner    Typ        rcvr_typ.spi  Rcvr
Corner    Min        rcvr_min.spi  Rcvr
Corner    Max        rcvr_max.spi  Rcvr
```

Calling the SPICE Model

```
| List of pin/port names
| in same order as in SPICE
Ports A_signal A_puref core A_pdref
|
| Convert analog core signal to digital core signal
| A_to_D d_port       port1   port2     vlow  vhigh  corner_name
A_to_D   D_receive  core    A_pdref  0.8   2.0     Typ
|
[End External Model]
```

Calling the VHDL-AMS Model


```
[Model] ExBufferAMS
Model_type Input
Vinh = 2.0
VinI = 0.8
[Voltage Range]   3.3     3.0    3.6
|
[External Model]
Language VHDL-AMS
Corner    Typ        rcvr_typ.vhd  Rcvr
Corner    Min        rcvr_min.vhd  Rcvr
Corner    Max        rcvr_max.vhd  Rcvr
```

Calling the VHDL-AMS Model

```
| Parameters are allowed
Parameters TempC cap
|
| List of pin/port names
| in same order as in VHDL-AMS
Ports A_signal A_puref core A_pdref
|
[End External Model]
```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