The Case Study of Board Simulation

Atsuji Ito ito.atsuji@jp.panasonic.com
Matsushita Electric Industrial Co., Ltd.
(Panasonic)

Panasonic digital appliance

- Digital Appliance of Panasonic

http://panasonic.jp/

Agenda

- The Status of JEITA EDA-WG
- The Case Study of Board Simulation in Panasonic
- The Issues of Board Simulation
- Proposal to the IBIS-WG

The Status of JEITA EDA-WG

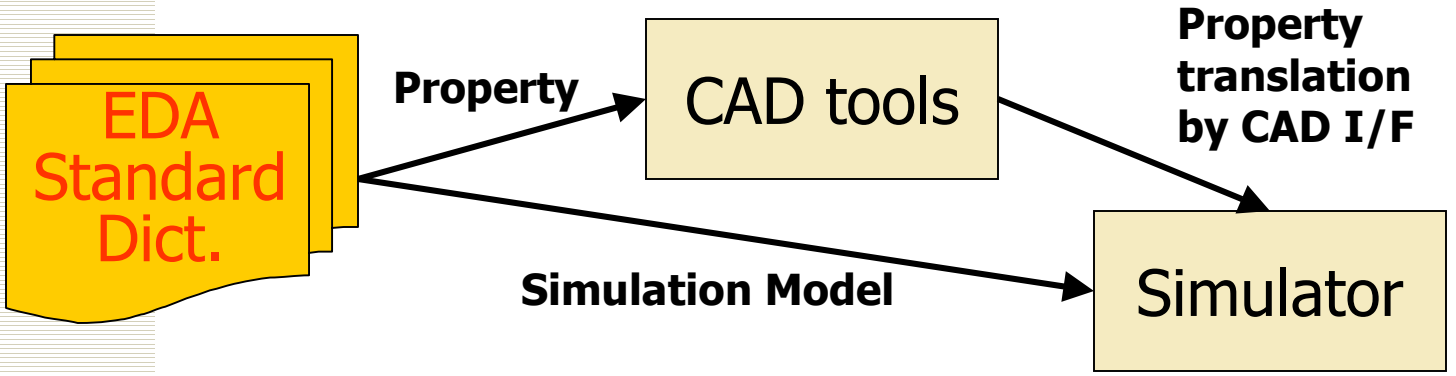
- JEITA is developing "EDA Standard Dictionary"

分類名称	CODE	EDIT	ERSION	VISION	PREFNAME.EN	PREFNAME.JA	SHORTNAME.EN	SHORTNAME.JA
L,C,R,C,Tr			001	01	Model Select	解析情報有無	Model Select	解析情報有無
ICLSI_SPICE			001	01	ICLSI_SPICE Model description file	ICLSI_SPICE モデル記述ファイル	Model file	モデル記述ファイル
ICLSI_SPICE			001	01	ICLSI_SPICE Circuit diagram	ICLSI_SPICE 回路図	Circuit diagram	回路図
ICLSI_SPICE			001	01	ICLSI_SPICE Subcircuit node	ICLSI_SPICE サブサーキットノード	Subcircuit node	サブサーキットノード
ICLSI_SPICE			001	01	ICLSI_SPICE \/I characteristics correlation	ICLSI_SPICE \/I特性グラフ	\/I-character	\/I特性グラフ
ICLSI_SPICE			001	01	ICLSI_SPICE Tr/Tf characteristics correlation	ICLSI_SPICE Tr/Tf特性グラフ	Tr/Tf-character	Tr/T特性グラフ
ICLSI_SPICE			001	01	ICLSI_SPICE Tr/Tf characteristics extraction co	ICLSI_SPICE Tr/Tf特性抽出回路	Tr/Tf-extraction	Tr/T特性抽出回路
ICLSI_SPICE			001	01	ICLSI_SPICE Simulator	ICLSI_SPICE 解析ツール	Simulator	解析ツール
Tr_SPICE			001	01	Tr_SPICE Model description file	Tr_SPICE モデル記述ファイル	Model file	モデル記述ファイル
Tr_SPICE			001	01	Tr_SPICE Circuit diagram	Tr_SPICE 回路図	Circuit diagram	回路図
Tr_SPICE			001	01	Tr_SPICE Subcircuit node	Tr_SPICE サブサーキットノード	Subcircuit node	サブサーキットノード
Tr_SPICE			001	01	Tr_SPICE \/I characteristics correlation	Tr_SPICE \/I特性グラフ	\/I-character	\/I特性グラフ
Tr_SPICE			001	01	Tr_SPICE Simulator	Tr_SPICE 解析ツール	Simulator	解析ツール
ICLSI_IBIS			001	01	ICLSI_IBIS Version	ICLSI_IBIS バージョン	Version	バージョン
ICLSI_IBIS			001	01	ICLSI_IBIS Model description file	ICLSI_IBIS モデル記述ファイル	Model file	モデル記述ファイル
ICLSI_IBIS			001	01	ICLSI_IBIS \/I characteristics correlation	ICLSI_IBIS \/I特性グラフ	\/I-character	\/I特性グラフ
ICLSI_IBIS			001	01	ICLSI_IBIS Tr/Tf characteristics correlation	ICLSI_IBIS Tr/Tf特性グラフ	Tr/Tf-character	Tr/T特性グラフ
ICLSI_IBIS			001	01	ICLSI_IBIS Log file	ICLSI_IBIS モデル記述チェックファイル	Log file	モデル記述チェックファイル
LCR_SPICE			001	01	LCR_SPICE Model description file	LCR_SPICE モデル記述ファイル	Model file	モデル記述ファイル
LCR_SPICE			001	01	LCR_SPICE Circuit diagram	LCR_SPICE 回路図	Circuit diagram	回路図
LCR_SPICE			001	01	LCR_SPICE Subcircuit node	LCR_SPICE サブサーキットノード	Subcircuit node	サブサーキットノード
LCR_SPICE			001	01	LCR_SPICE Frequency characteristics	LCR_SPICE 特性グラフ	F-character	特性グラフ
LCR_SPICE			001	01	LCR_SPICE Simulator	LCR_SPICE 解析ツール	Simulator	解析ツール
LCR_Sパラメータ			001	01	LCR_S Parameter Model description file	LCR_Sパラメータ モデル記述ファイル	Model file	モデル記述ファイル
LCR_Sパラメータ			001	01	LCR_S Parameter Frequency range	LCR_Sパラメータ 周波数範囲	Frequency range	周波数範囲
LCR_Sパラメータ			001	01	LCR_S Parameter Measurement condition	LCR_Sパラメータ 測定条件	Measurement	測定条件
LCR_Sパラメータ			001	01	LCR_S Parameter Frequency characteristics	LCR_Sパラメータ 特性グラフ	F-character	特性グラフ
LCR_Sパラメータ			001	01	LCR_S Parameter Simulator	LCR_Sパラメータ 解析ツール	Simulator	解析ツール

  - Model circuit diagram, subcircuit node information,characteristics graph, verified simulator, ...

The Status of JEITA EDA-WG

- Purpose of the"EDA Standard Dictionary"
  - One category of ECALS dictionary(for EDI)
  - Useful information for the components selection
  - In order to perform simulation smoothly

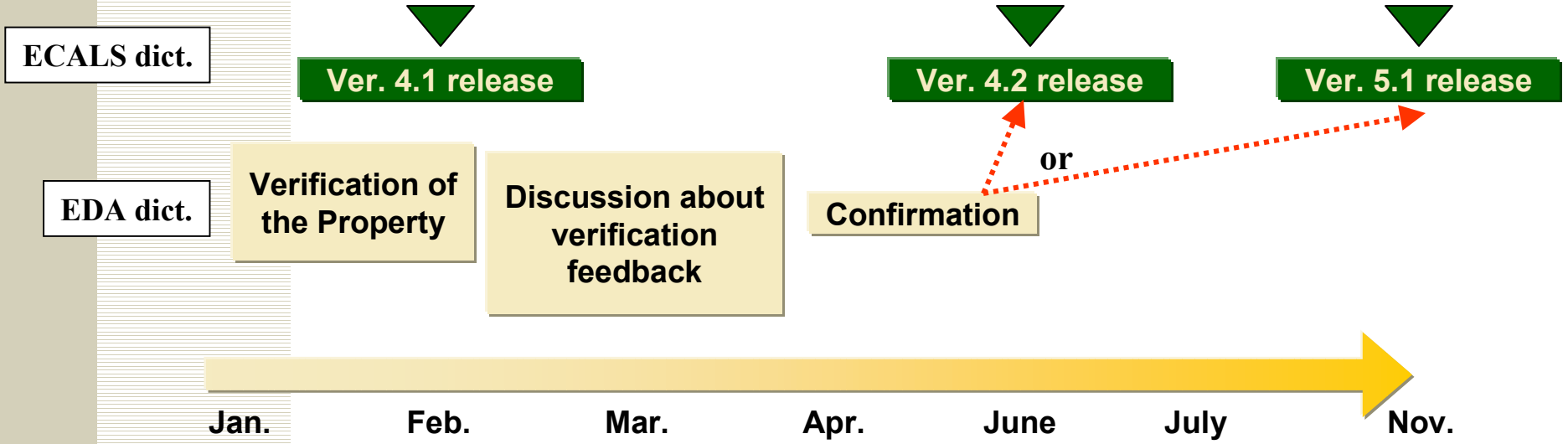


The Status of JEITA EDA-WG

- "EDA Standard Dictionary" is in a verification stage
  - KYOCERA, Murata Manufacturing, TDK provided sample dictionaries
  - Appliance maker evaluated and verified those dictionaries
  - Feedback from appliance maker will be discussed at the EDA-WG

The Status of JEITA EDA-WG

"EDA Standard Dictionary" Development Schedule



Agenda

- The Status of JEITA EDA-WG
- The Case Study of Board Simulation in Panasonic
- The Issues of Board Simulation
- Proposal to the IBIS-WG

The Case Study of Board Simulation

- Using Board Simulation for the Digital HDTV design
  - Aim ： Improvement of the picture quality
    Reduction of trial design
    Cost down

  - Approach:
    - Direct connection of the digital picture stream data between the digital boards
      - Remove DAC/ADC from the board to board connection
    - Placement and route optimization of the LSI and RAMs
      - Smaller area, reduction of the trial
    - Improvement of the LSI

BSデジタル放送の美しさをそのまま再現。「デジタル直結処理回路」

BSデジタルチューナーからのデジタル信号を変換することなく映像処理し、広帯域化することで、BSデジタル放送の美しい高画質映像を鮮明に再現します。

(http://panasonic.jp/tv/products/hi_vision/feature/picture.html)

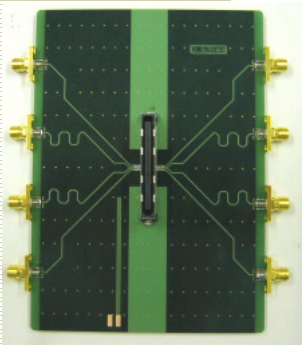
The Case Study of Board Simulation

Summary of the simulation(1)

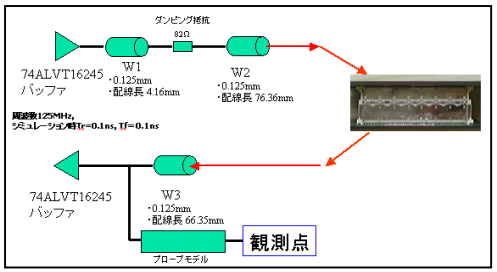
– Direct connection of the digital picture stream data

Next challenge

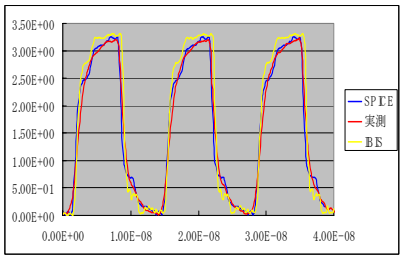
Extraction and Evaluation of the connector model → **Floor Plan simulation by SPICE, IBIS** → **Evaluation of the simulation results** → **Layout Simulation**



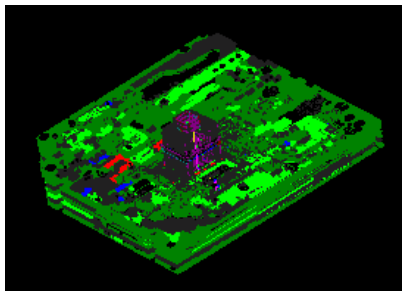
• **Extraction of the SPICE model**



• **Evaluation of the design condition (trace length, impedance, series resistor, …)**
• **Crosstalk(connector pin assignment)**



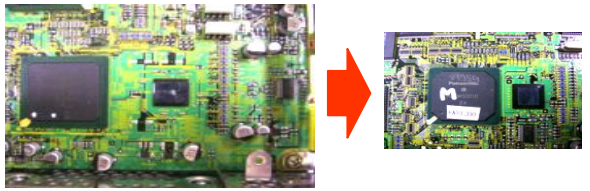
• **Evaluation of the accuracy**



• **Power/GND Analysis**

The Case Study of Board Simulation

- Summary of the simulation(2)
  - Placement and route optimization of the LSI and RAMs



- Optimization of the trace impedance
- Examination of the driver abilities
- Termination
- Crosstalk
- Signal Integrity

- 4 layers Rambus
- 6 layers smaller area (Achieve 60%)

Expansion of the Rambus rules and make Panasonic rules

Agenda

- The Status of JEITA EDA-WG
- The Case Study of Board Simulation in Panasonic
- The Issues of Board Simulation
- Proposal to the IBIS-WG

The Issues of Board Simulation

- Background and issues
  - Transient analysis is useful for the digital appliance
    - SI simulator or SPICE is useful
  - S-parameter model is often supplied for High frequency(RF) components

Higher frequency digital = Using RF components

Time domain ⇔ Frequency domain

Freq. Domain model is not useful!

The Issues of Board Simulation

- Approaches … 2 types of approaches
  - Using RF simulator
    - ○ • S-parameter model can be used directly
    - △ • Time domain module is often option(i.e. more cost)
    - × • IBIS, SPICE models cannot be used for ICs

○ : OK
△ : So so
× : NG

  - Translation S-parameter model to SPICE model
    - ○ • Simulator can be used as it is(i.e. no more cost)
    - ? • Translation accuracy → Evaluation this time!

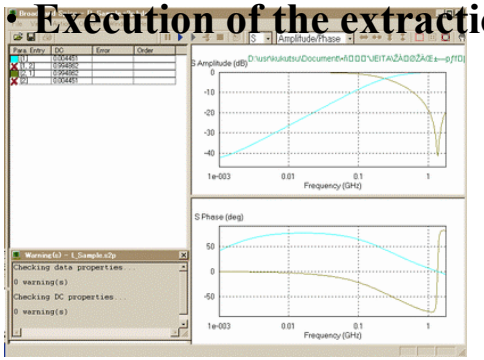
The Issues of Board Simulation

- Description of the translation
  - Translation S-parameter to SPICE model
    - Using BroadBand Spice (Sigrity)

Read and check S-parameter → **Extraction** → **Result Check**

- **Format checking**
- **Calculate DC value**

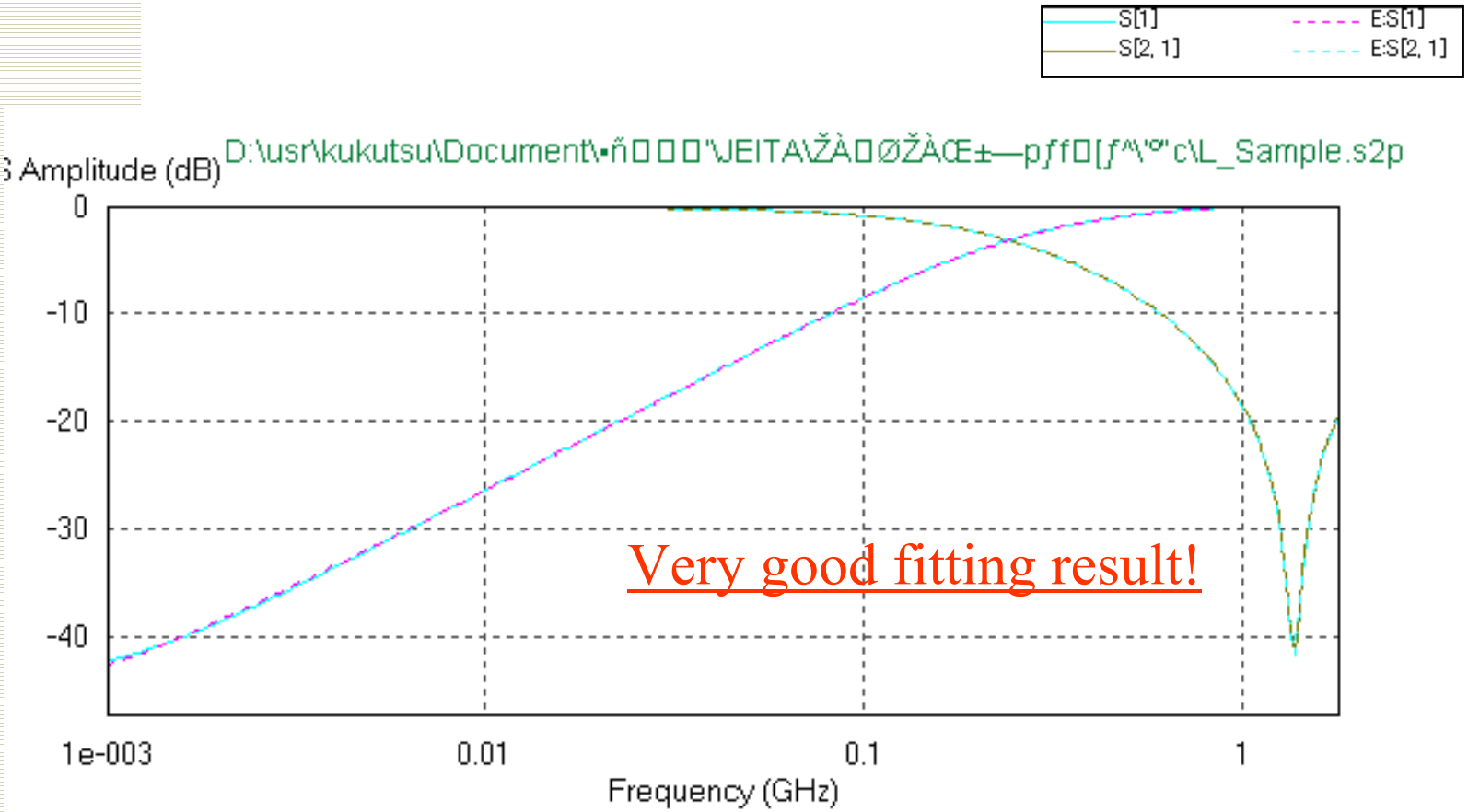
- **Choose types of export model**
- **Execution of the extraction**



- **Check wafeforms**
- **Re-fitting if necessary**

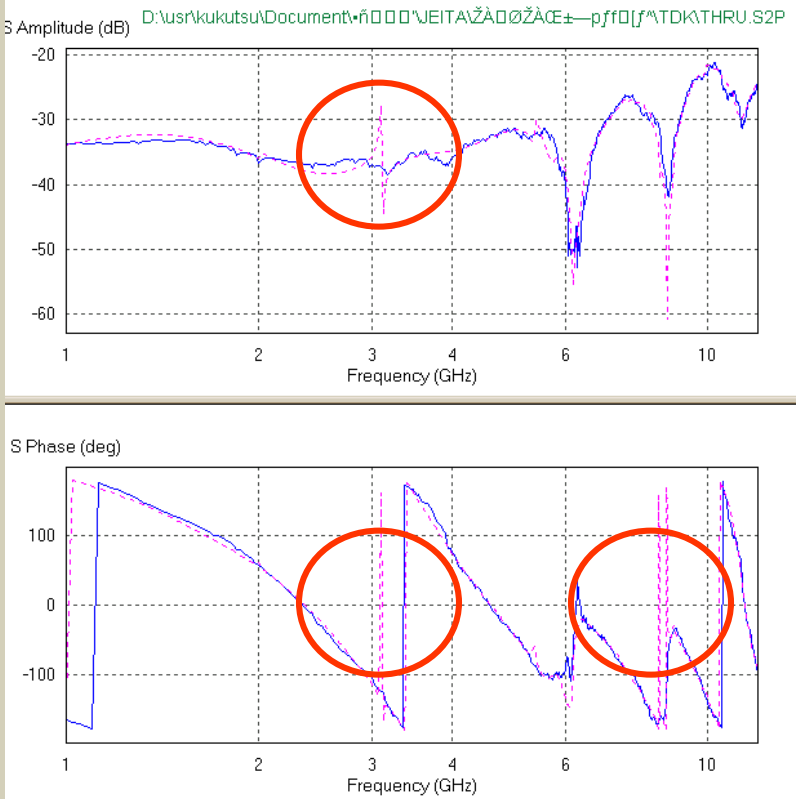
The Issues of Board Simulation

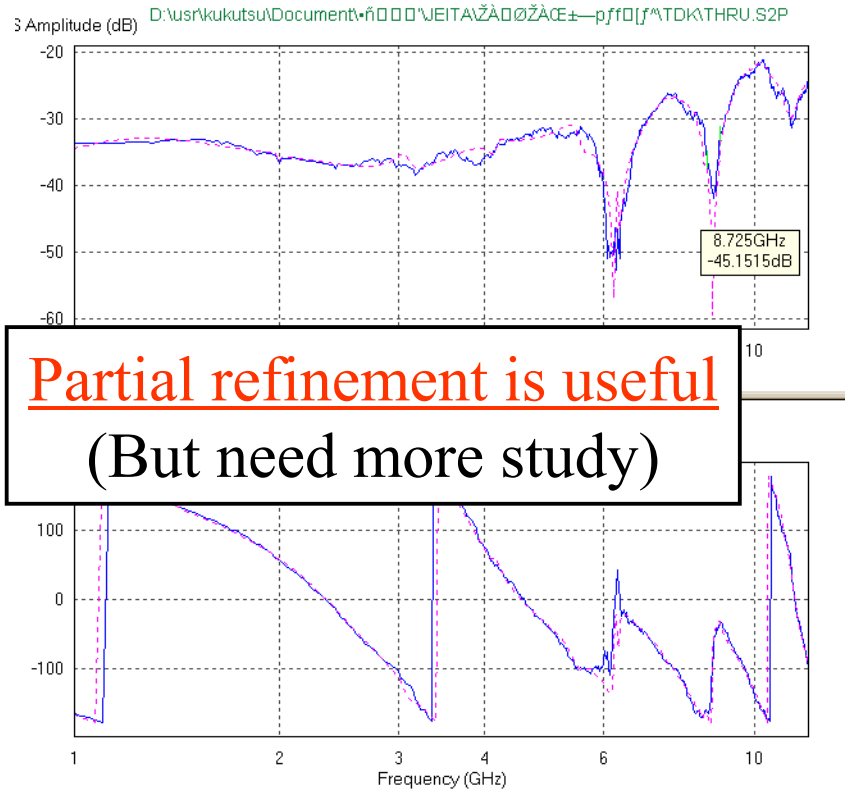
- Extraction result (1)



The Issues of Board Simulation

Refinement example





Partial refinement is useful

(But need more study)

The Issues of Board Simulation

Extraction result … Extracted models

HSPICE native format

```
* This is the subcircuit netlist generated by Broadband SPICE v1.0
* Port Number: 2.
* HSPICE compatible
.subckt L_Sample 1  2  ref
Rd1_1           3  ref  50
Rd1_2           4  ref  1
Vd1             1  3  0
F1              ref   4  Vd1  1.0
G1              ref   4  1  ref        0.02
Rd2_1           5  ref  50
Rd2_2           6  ref  1
Vd2             2  5  0
F2              ref   6  Vd2  1.0
G2              ref   6  2  ref        0.02

G3  ref 3 LAPLACE 4 ref
+ -4.2194949336101296e+016
+ -7.6924500349367864e+005
+ /
+ 8.0538254790796067e+019
+ 1.1053698816035342e+009
+ 1
```

General SPICE format

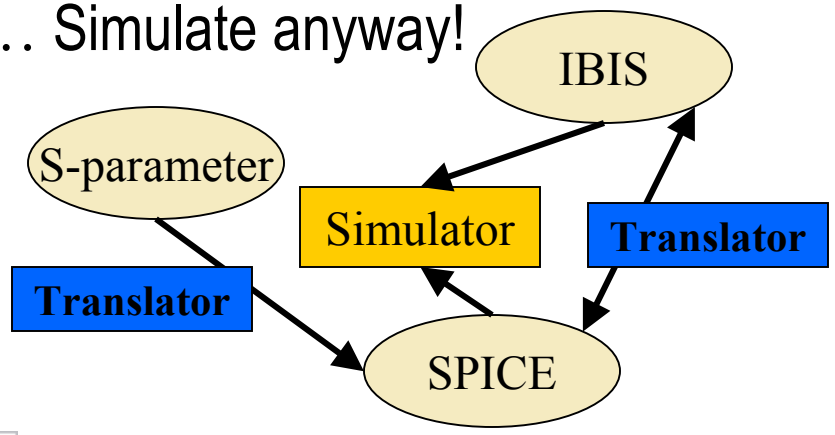
```
* This is the subcircuit netlist generated by Broadband SPICE v1.0
* Port Number: 2.
* SPICE compatible
.subckt L_Sample 1  2  ref
Rd1_1           3  ref  50
Rd1_2           4  ref  1
                        .
                        .
                        .
L2_3_0 n1_1_2 n1_1_par0 2.6196734419533908e-008
C2_3_0 n1_1_par0 n1_1_0 4.7396975379644448e-013
R2_3_0 n1_1_par0 n1_1_0 1.9087178929704005e+003
L1_3_0 p1_1_2 p1_1_ser0 2.6735500391528574e-008
C1_3_0 p1_1_ser0 p1_1_serd0 4.6441845416260152e-013
R1_3_0 p1_1_serd0 p1_1_0 2.9552616902395183e+001

L2_3_1 n1_1_2 n1_1_par1 2.4621677645809129e-007
C2_3_1 n1_1_par1 n1_1_0 6.6348538919814883e-014
R2_3_1 n1_1_par1 n1_1_0 4.8138425989128831e+004
L1_3_1 p1_1_2 p1_1_ser1 2.2790661272104553e-007
C1_3_1 p1_1_ser1 p1_1_serd1 7.1679023177516205e-014
R1_3_1 p1_1_serd1 p1_1_0 7.1356522526650309e+001
```

The Issues of Board Simulation

- Wrap up
  - S-parameter model can be applied for time domain simulation ⇒ Expansion of the simulation case
  - Examination of the accuracy would be necessary
    - S-parameter extracted conditions(frequency range, …)
    - Theoretical limitation
    - Characteristics of the components

The Case Study of Board Simulation

- Next Step
  - Expansion of the Model Extraction Environment
    - Although semiconductor component would be difficult, we would like to increase more types of passive components
  - Construction of the simulation environment which can handle various model format
    - 1st step:Model translation … Simulate anyway!
    - 2nd step: More accuracy



Agenda

- The Status of JEITA EDA-WG
- The Case Study of Board Simulation in Panasonic
- The Issues of Board Simulation
- Proposal to the IBIS-WG

Proposal to the IBIS-WG

- Requirement to the models(more accuracy)
  - More useful 'variation' parameters
    - Min/Max is not for useful because those conditions are not likely on the board.
    - Practical 'variation' conditions, range(number of condition, e.g. typ1, typ2, or ,10degree, 25degree, 40degree, 80degree, …) would be necessary
    - 'variation' parameter of each production lot would be useful

Proposal to the IBIS-WG

- Co-operation between IBIS-WG and JEITA EDA-WG to improve board simulation environment
  - IBIS-WG: LSI, Package, module model accuracy
  - JEITA EDA-WG: Feedback board simulation study result