Data Dependent Buffer Characteristics

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Agenda

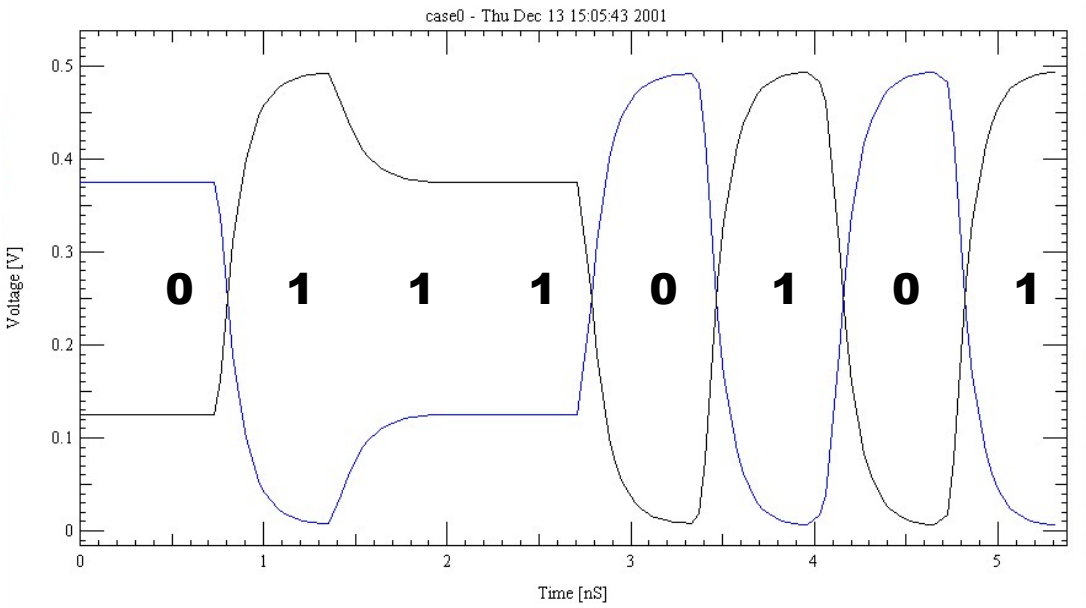
- **Motivation**
- **Pre-emphasis review**
- **SPICE to IBIS conversion example**
  - Original approach
  - Modified Vt curve approach
- **Miscorrelation explained**
  - Fine tuning the IBIS model
- **Summary**

Motivation

- **The need for BIRD75 was questioned by some**
  - Fear: additional features may make IBIS model generation harder and more error prone
- **Previous studies have shown that too many IBIS models are lacking in quality**
  - Suggestions: concentrate more on getting better IBIS models with the existing capabilities of the specification
- **This case study intends provide one example of a practical situation for which the new features of BIRD75 are essential**

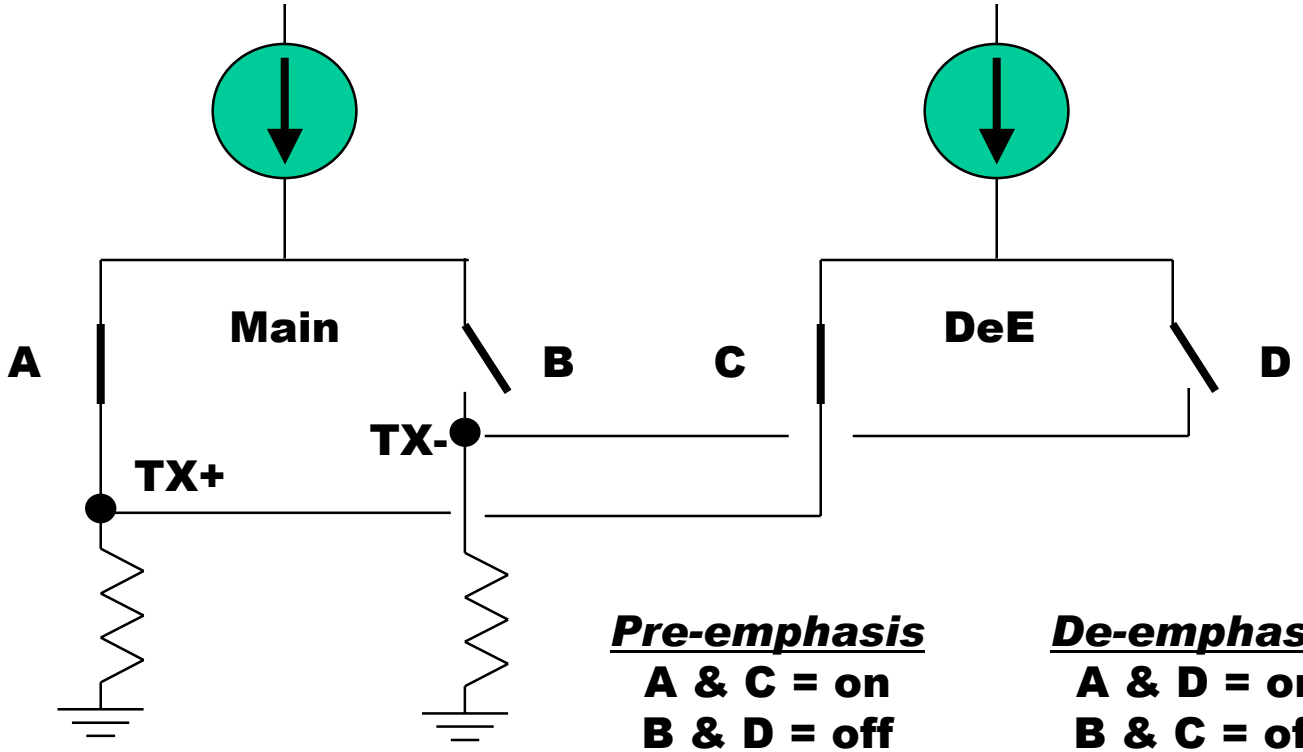
Differential Pre-emphasis design examples

- **Driven strength X at time t (X_t) depends only on X_{t-n}**
- **For S-ATA (optional) & PCI-Express (required), n=1**
  - Strength of bit at time X_t depends only on bit at X_{t-1}
  - Strength increased after bit transition
  - Example: 0111 0101 (both complementary signals shown)



Pre-emphasis / De-emphasis buffer

- Pre-emphasis sums both sources through one “leg”
- De-emphasis “steals” current from non-driving leg
- Total current in system always the same



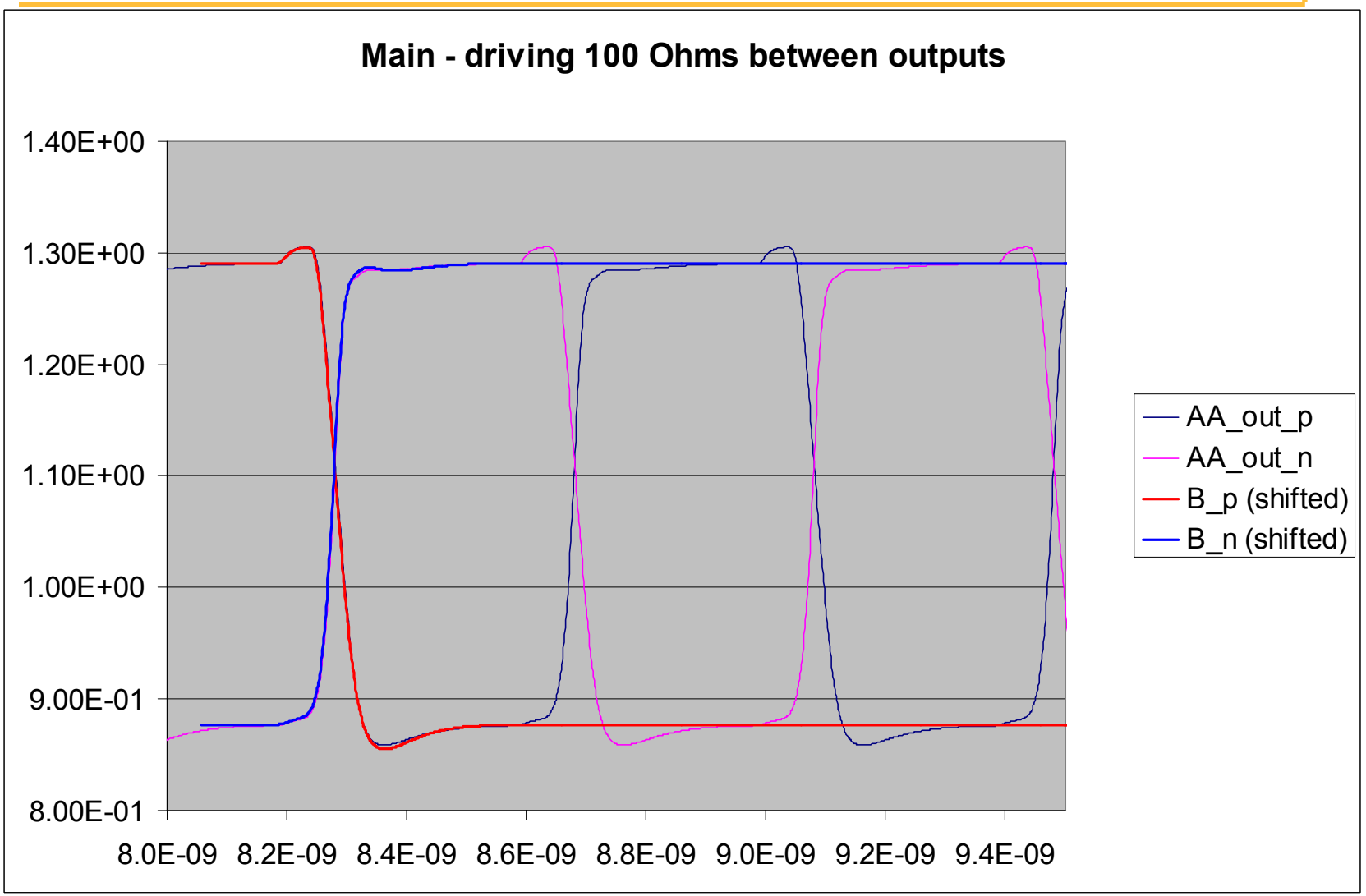
Pre-emphasis
A & C = on
B & D = off

De-emphasis
A & D = on
B & C = off

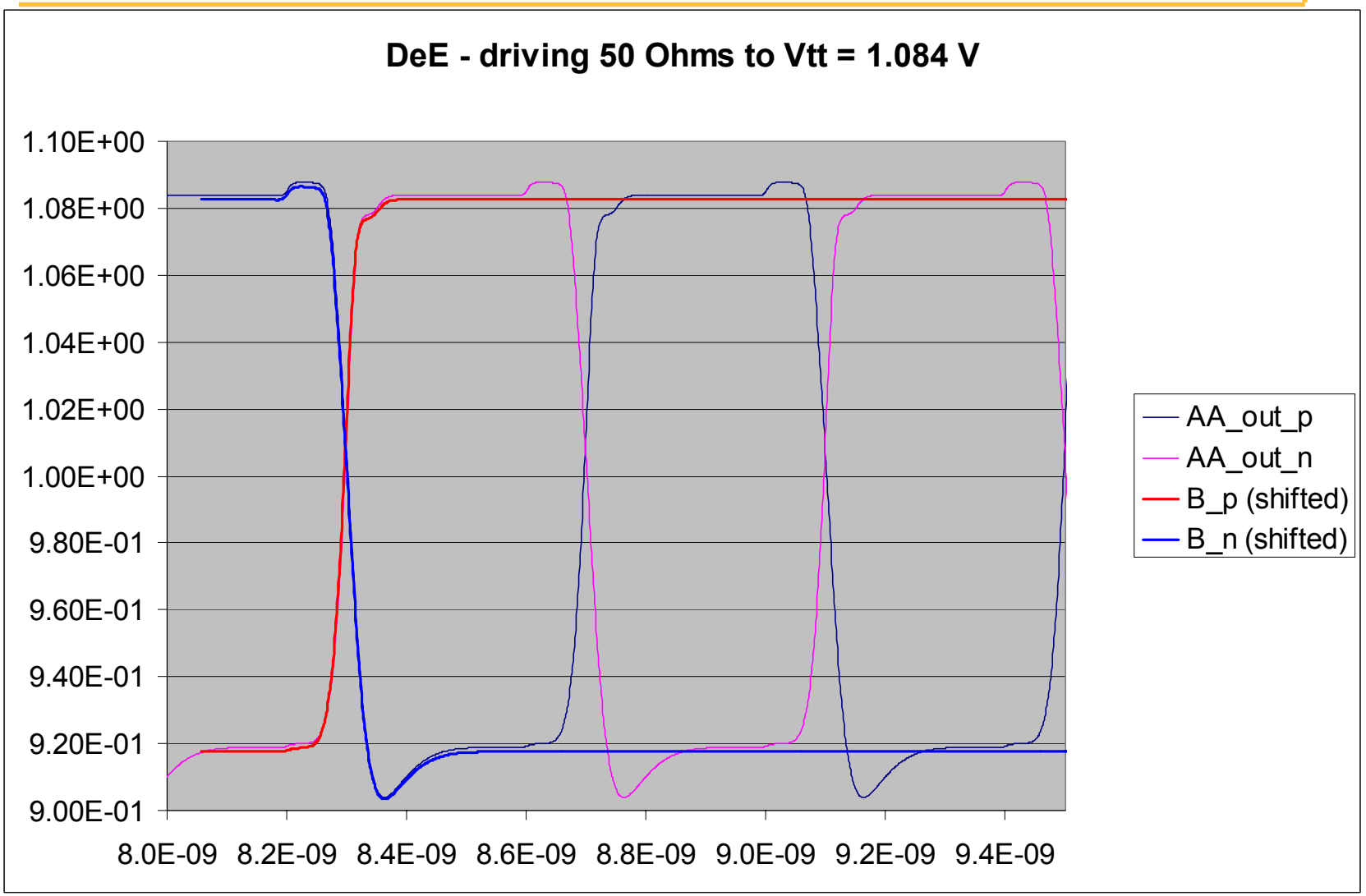
SPICE to IBIS conversion process

- **Separate the Main and De-emphasis (DeE) parts of the buffer and make independent IBIS models for each**
  - generate “common current” IV curves (sweep both outputs with the same voltage simultaneously) assuming that the “differential current” between the pins is negligible
  - determine what the average voltage of the normal signal swing is
  - generate Vt curves with two series 50 Ω resistors between pins with the nodes between the resistors connected to the average voltage of normal signaling
- **Compare Main and DeE IBIS vs. SPICE models separately**
  - the DC levels and edge rates correlated well
  - all features of waveforms are reproduced faithfully
- **Compare complete buffer with SPICE model**
  - falling edge has large undershoot before reaching DC level
  - rising edge creeps up to final DC level
  - edge rate is not matching when coming out of strong bit to weak bit
- **Conclusion: the halves of the buffer do influence each other**

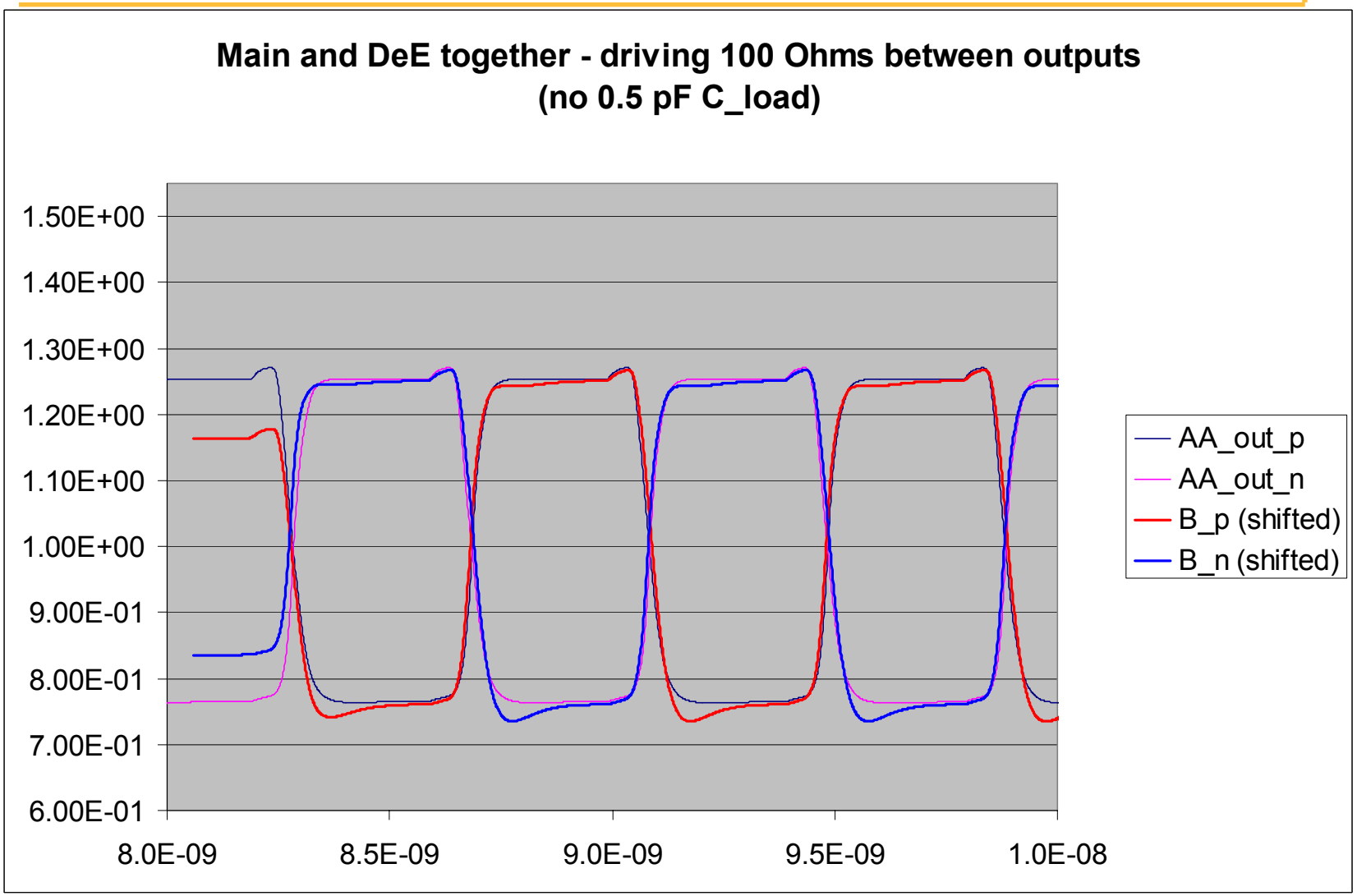
Good match for Main buffer



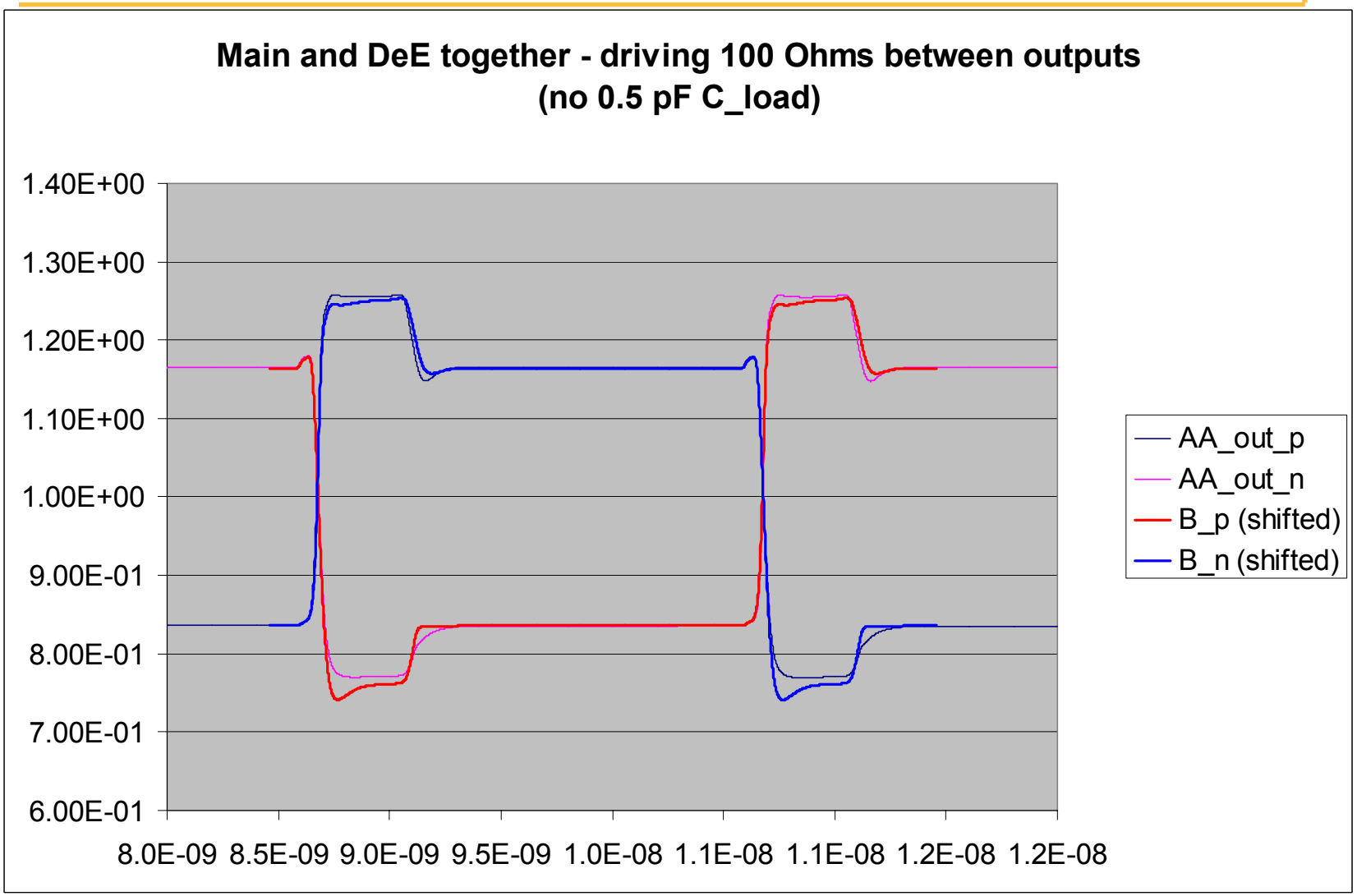
Good match for De-emphasis buffer



Combined model #1 with 1010 pattern



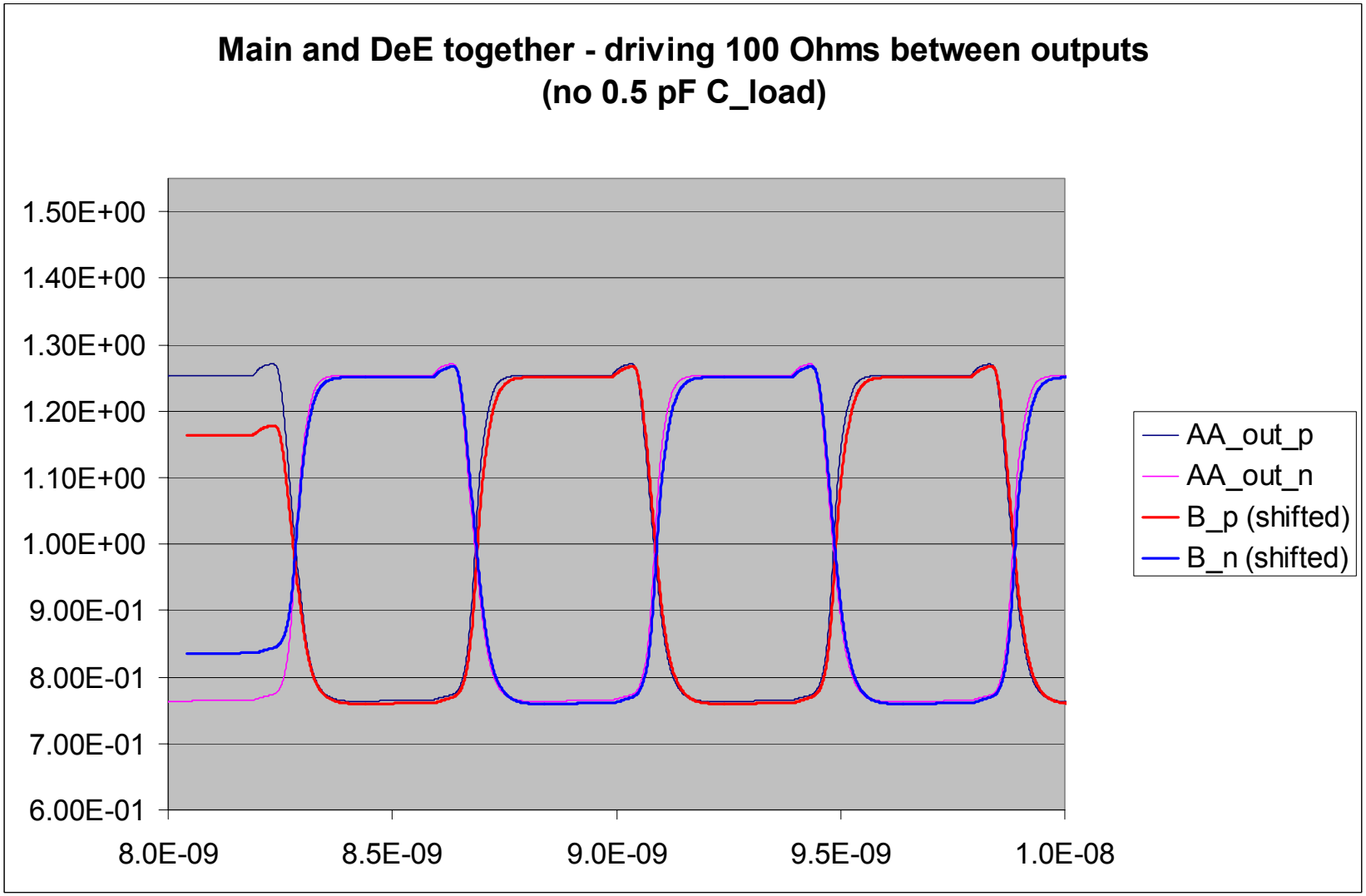
Combined model #1 with 11110000 pattern



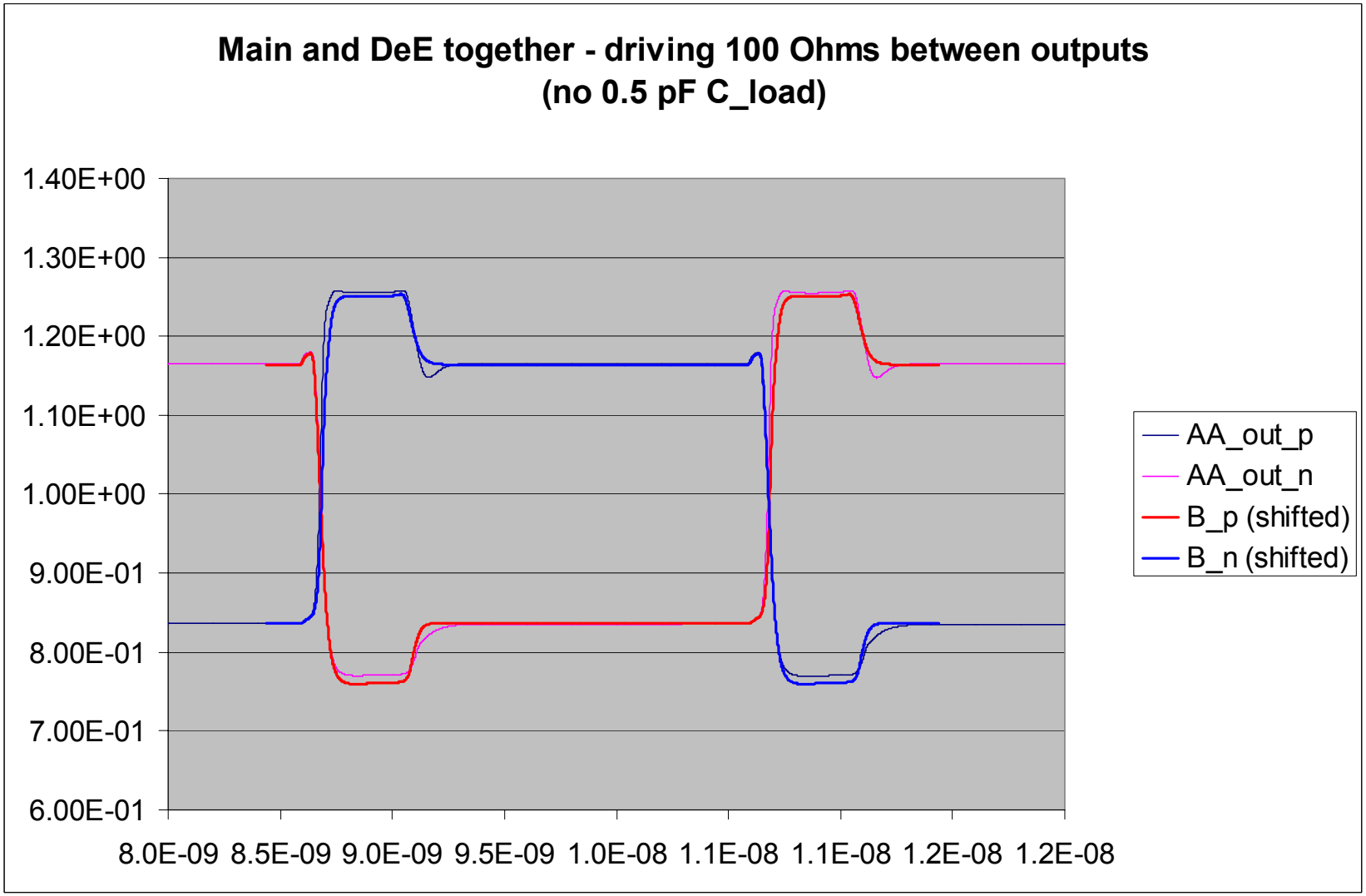
Modified Vt curve extraction process

- **Keep IV curves the same as before**
  - generate “common current” IV curves (sweep both outputs with the same voltage simultaneously) assuming that the “differential current” between the pins is negligible
- **Extract Vt curves using combined buffer to get correct shape**
  - determine what the average voltage of the normal signal swing is
  - generate Vt curves with two series 50 Ω resistors between pins
  - nodes between resistors connected to the average V of normal signaling
- **Use the shape of these Vt curves for Main and DeE buffer, but use IBIS Center to correct the DC levels to match IV curves**
  - this is necessary to ensure that the end points of the Vt curves match the IV curve / load line intersection voltages
- **Conclusion: the shape of the Vt curve obtained from the complete buffer results in waveforms that correlate much better with the original SPICE model**
  - however, the data dependency in the DC levels is still present
  - edge rate still not very accurate when going from strong bit to weak bit

Combined model #2 with 1010 pattern

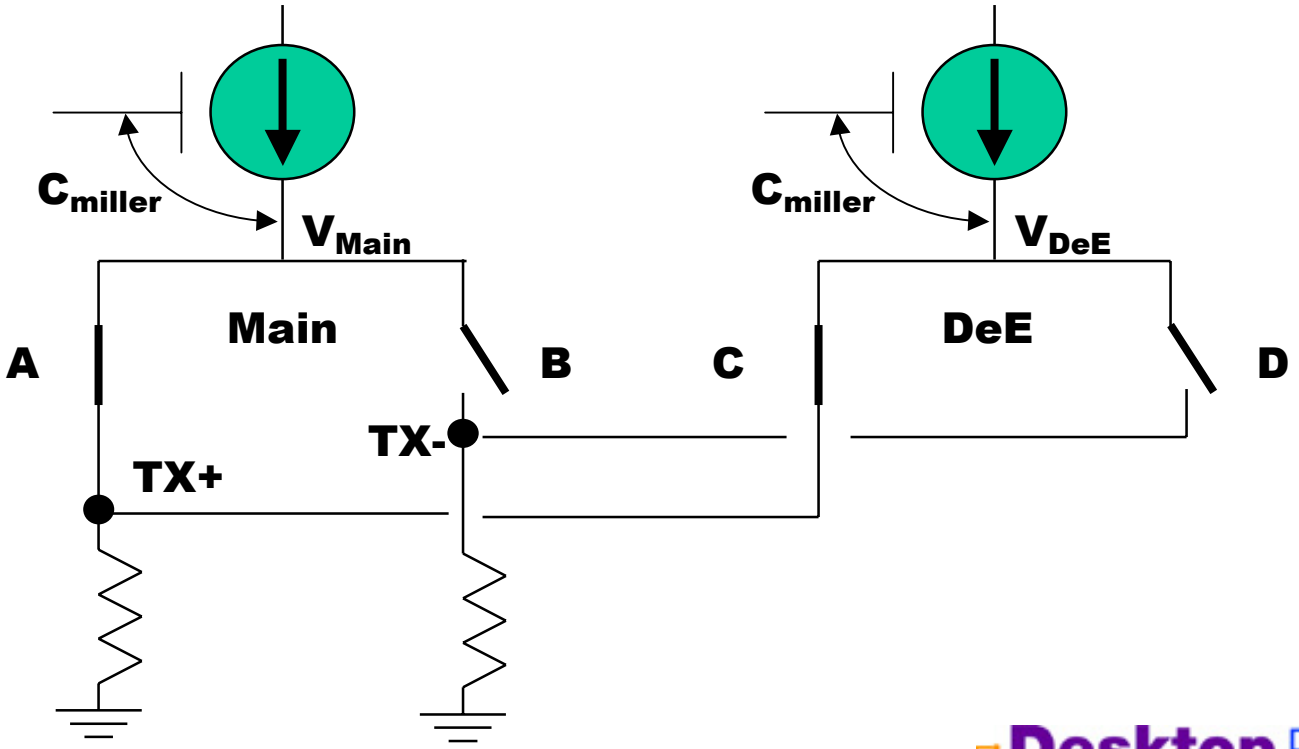


Combined model #2 with 11110000 pattern



Cause of miscorrelation

- Current sources are usually transistors with a DC bias on the gate
- Depending on the mode of operation (i.e. data pattern), V_{Main} and V_{DeE} are not steady, and they move independently
- This variation couples to the bias voltage (gate) of the current sources, modulating the “strength” of the buffers independently
- This effect is worse during transitions, modulating slew rates also



Fine tuning Vt curves

- **Analyzing the miscorrelation, the following was observed**
  - edge mismatches were worst with 11110000 data pattern
  - strong bit to weak bit transition is done by the De-emphasis buffer
  - weak bit to strong bit transition is done by the Main buffer
  - even though both buffers switch together in the 1010 pattern, the Main buffer dominates (it is about 5x the size of DeE)
- **A few experimental simulations showed that**
  - shifting and scaling the rising / falling edges of the Main and DeE buffer independently changes the edge rate and size of the overshoot and notch in the simulated waveforms
- **Combining the observations above, a manual iterative fine tuning of the Vt curves was carried out**
  - the time axis of the Vt curves were scaled using the “rwf_scal” and “fwf_scal” parameters of the HSPICE* B-element
  - the time placements of the rising and falling edges of the Main and DeE buffers were independently shifted left or right using fully parameterized PWL sources as the input stimulus to the B-elements
  - this iterative “optimization” was used to find the best scaling and shifting coefficients for the Vt curves of the IBIS model

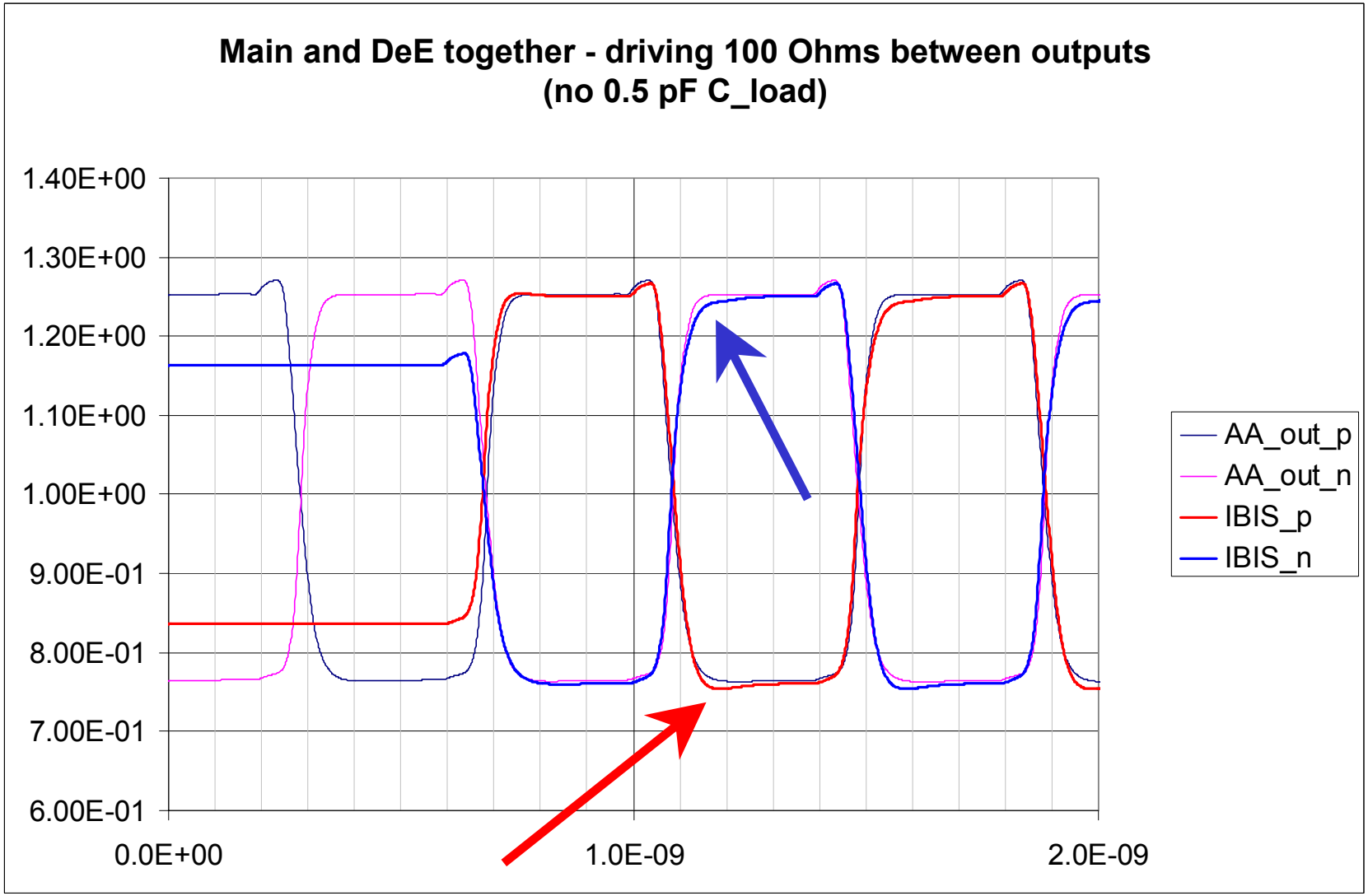
New Vt curves were generated

- **Scaling the horizontal axis to adjust edge rates**
  - .LIS file has three blocks of data for the typ, min., max. corners
  - rising and falling edges are side by side with a common x-axis column
  - in order to be able to scale corners and rise/fall edges independently a duplicate x-axis was generated for each curve
  - after scaling the x-axis they had to be re-sampled so that the rise/fall data could share a common x-axis again (done in Matlab with spline)
- **Shifting edge positions**
  - the y-axis columns were shifted up/down in time to achieve correct edge positions (done in EXCEL*)
- **Making new IBIS file**
  - the new Vt tables were saved off from EXCEL* into the .LIS files without changing the IV curves
  - IBIS Center was used without any data processing to convert the .LIS file to the IBIS format
- **Testing the new IBIS model**
  - the new IBIS model was simulated with the HSPICE* B-element and the output waveform was overlaid with the original Analog Artist* waveforms

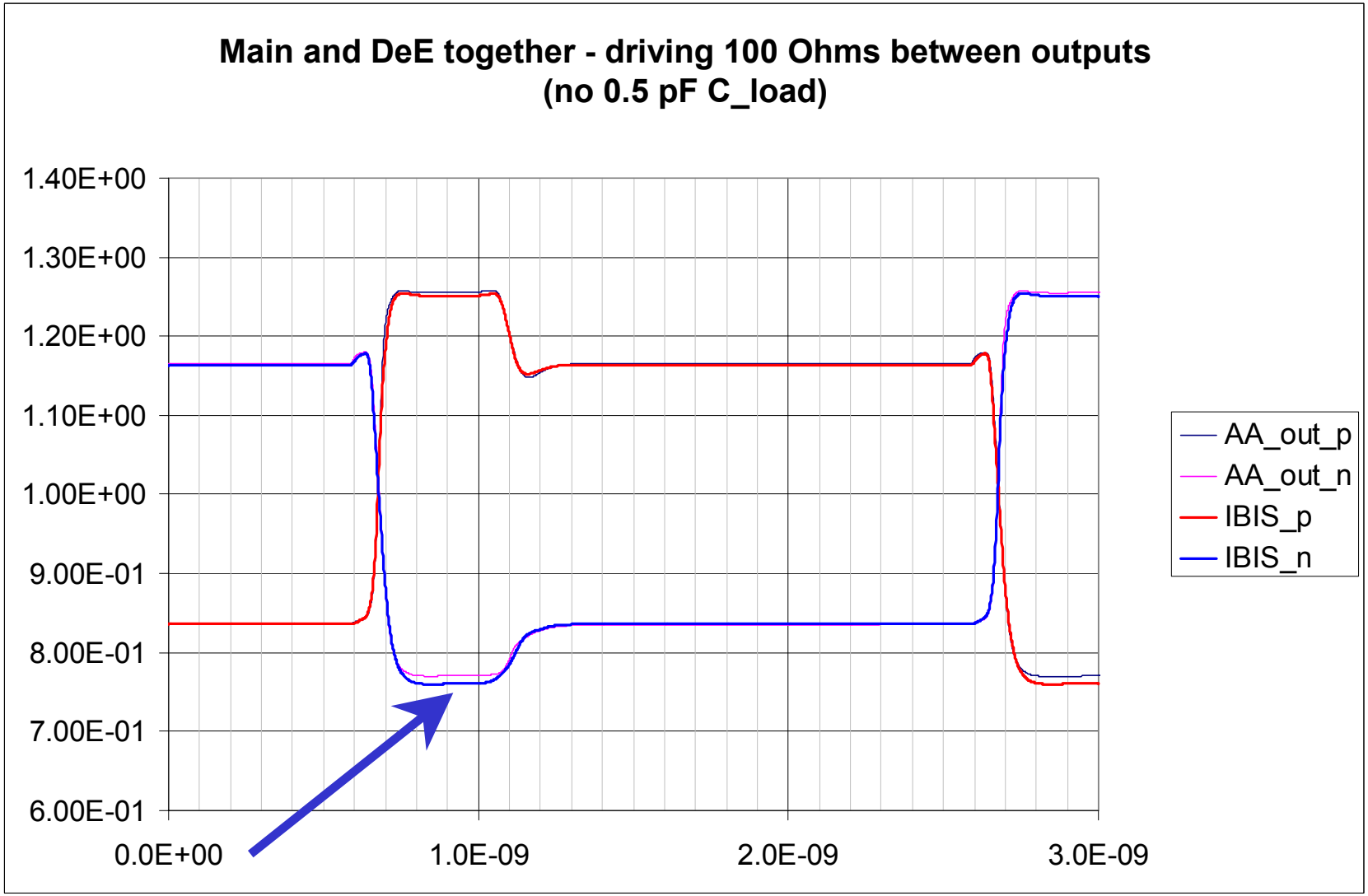
Results

- **The new overlay of the IBIS waveforms show**
  - very good match on both rising and falling edges for 11110000 pattern
  - the bumps, notches and overshoot/undershoot effects are now visible in the IBIS waveforms
  - the edge rates now match in both directions even when transitioning from the strong bit to the weak bit
  - the edge rate for the 1010 pattern is still good, but the rising edge has a somewhat larger rounding effect than before and the slow corner shows a slight shift on the rising edge
  - this is a compromise that had to be made to ensure the above matches and is due to the data dependent modulation of the current source
  - the DC levels of the strong bit is still off on the low side due to the data dependent modulation of the current source
- **These issues are highlighted by the arrows on the following pages**

Combined model #3 with 1010 pattern



Combined model #3 with 11110000 pattern



Summary

- **It has been shown that some buffer types can have data dependent DC and transient characteristics**
  - Voltage level and edge rate modulation
- **It has been shown that conventional IBIS models cannot describe these effects**
  - Tedious manual fine tuning did not solve the problem
- **A few relatively simple logic equations coupled with the analog portions of the IBIS model could solve the problem**
  - The VHDL-AMS or Verilog-AMS extensions to IBIS would make modeling these devices possible