BIRD95:
Power Integrity Validation using HSPICE

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Cisco Systems, Inc

Acknowledgement

- We would like to thank all industry colleagues for their valuable inputs, comments and hard work. Special thanks to Sigrity for their valuable discussions.
- Thanks to Ilyoung Park – Cisco Systems, Inc for all validation simulation results.
- A special acknowledgment to Istvan Novak - SUN and Sergio Camerlo - Cisco, for their support and vision

Agenda

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- History of Power Integrity simulations with IBIS
- Summary of Problems with current IBIS Models in Power Integrity simulations
- BIRD95 Proposal
- Implementation and correlation of BIRD95 using HSPICE
- Conclusions

The Challenge

DesignCon2004 PDN Panel

- **DesignCon2004 PDN Panel:**

  Sergio Camerlo (Cisco Systems, Inc) and Istvan Novak (SUN Microsystems) challenged the EDA / Modeling Industry to solve Power Integrity Analysis through accurate modeling and simulation

- **DesignCon2004 PDN Simulation Panel proceedings and materials**

  http://home.att.net/~istvan.novak/papers.html

Brief History

- Goal: leverage the good work already done by many experts within IBIS and IEC
- BIRD42.3 was revisited in terms of IvsT tables

  Many thanks to all those who had initiated this proposal
- ICEM (Integrated Circuits Electrical Model) – IEC62014-3

  http://www.ic-emc.org

  "..I would be pleased to attend an IBIS committee meeting to illustrate and explain our work…"

  - Etienne SICARD, INSA, Jan25th 2005
- Various discussion continued with IBIS forum.

  3/4/2004, 5/14/2004, 6/8/2004, 7/16/2004, 8/24/2004 etc
- BIRD95 was proposed by Cisco Systems, Inc on Dec13th 2004
- BIRD95.1 was revised Jan28th, 2005

The Proposal – BIRD95

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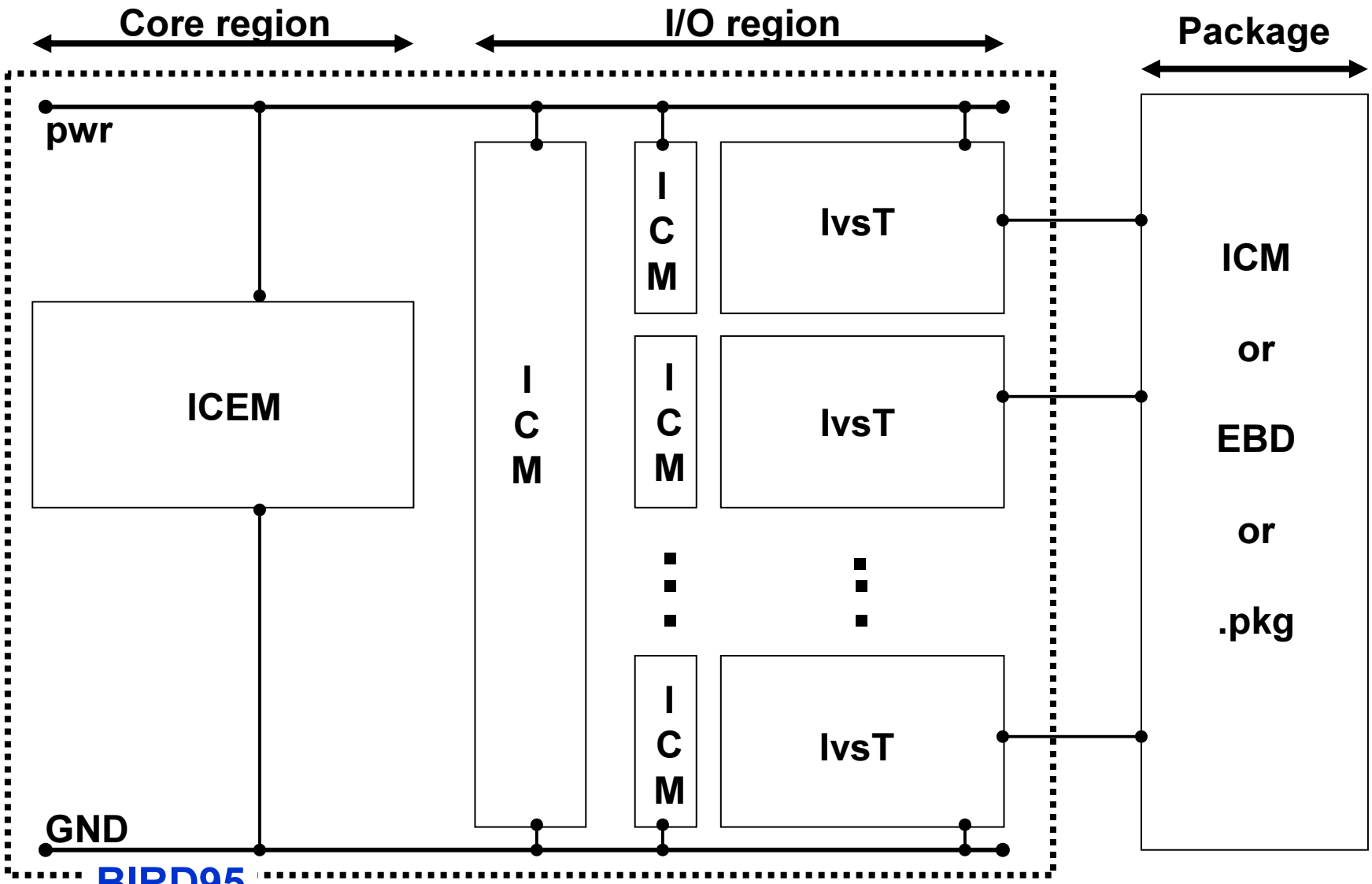
- **BIRD95 - Power Integrity Analysis using IBIS**
- **Task#1**

  Solve the SSN simulation challenge using IvsT
- **Task#2**

  Connect to the Core model using ICEM

Major components of BIRD95



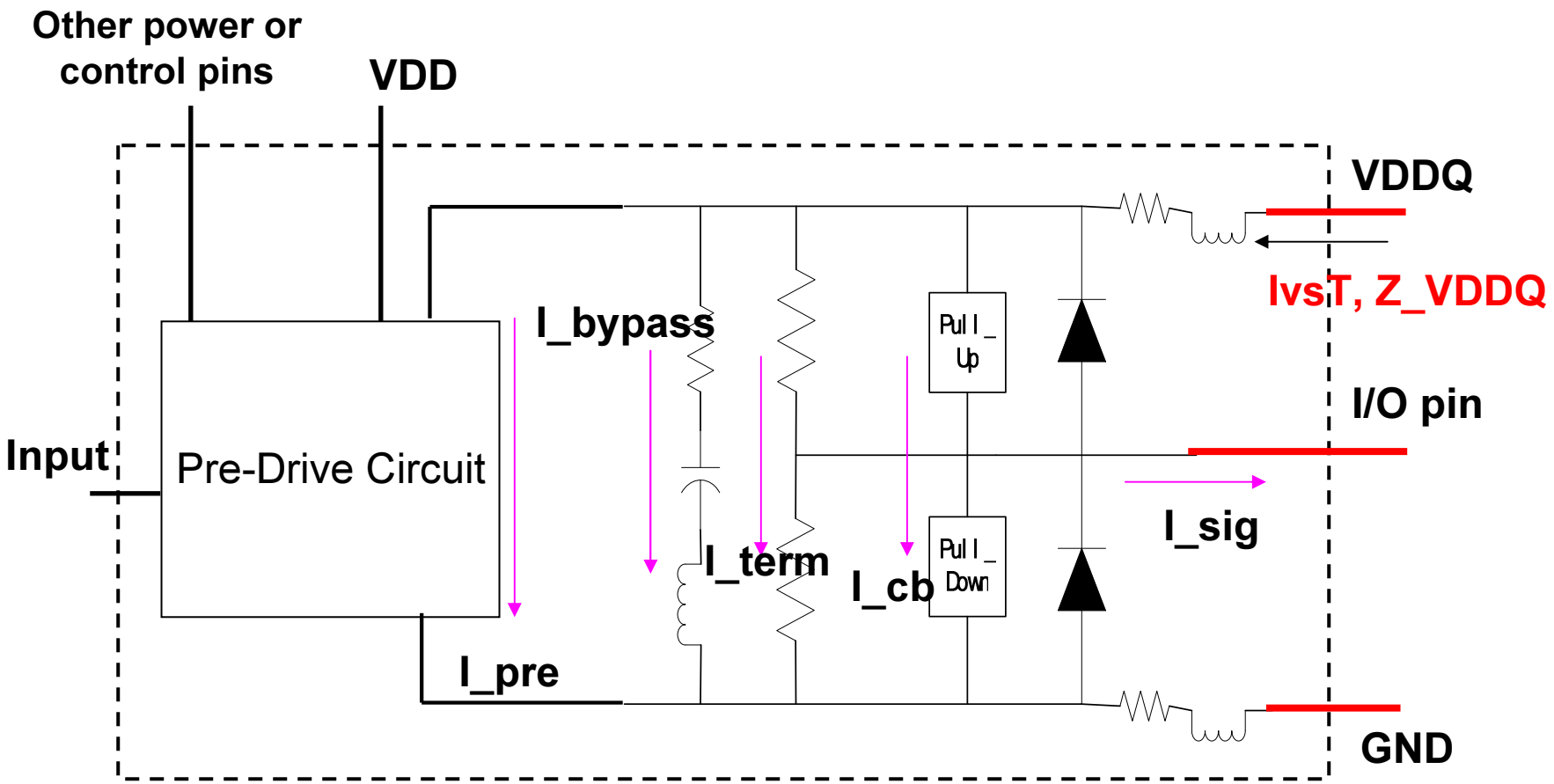
Validation using HSPICE

- **Part-II**

Summary of Problems with Current IBIS Model in Power Integrity simulations

- Pre-drive current is completely ignored
- On-die parasitic capacitance between power and ground is not included
- X-bar current is completely ignored, or not correctly modeled
- Existing IBIS SSN simulation could either over- or under- estimate the power noise

BIRD95 Proposal



Note: Encrypted circuit model could include elements shown in the dashed box (black box). All info in BIRD95 is extracted from this black box through VDDQ, I/O and GND pins. Internal details are not needed.

Definition of IvsT and Z_VDDQ

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- IvsT is the total current from the VDDQ which is connected to ideal DC voltage source
- There are total 6 IvsT tables (3 different I/O loadings associated with rising/falling edges)
- Z_VDDQ is the frequency-dependent impedance derived with the correct DC voltage applied at VDDQ pin and open-load condition
- Z_VDDQ information is proposed to be provided through ICM model

Implementation and Correlation of BIRD95 in HSPICE

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- Simulation description
- Evidence of the problems with current IBIS model (Ideal Power Supply case)
- ***BIRD95*** implementation schematics
- Results with added IvsT (I versus T)
- Results with added IvsT and Z_Vddq

Simulations description

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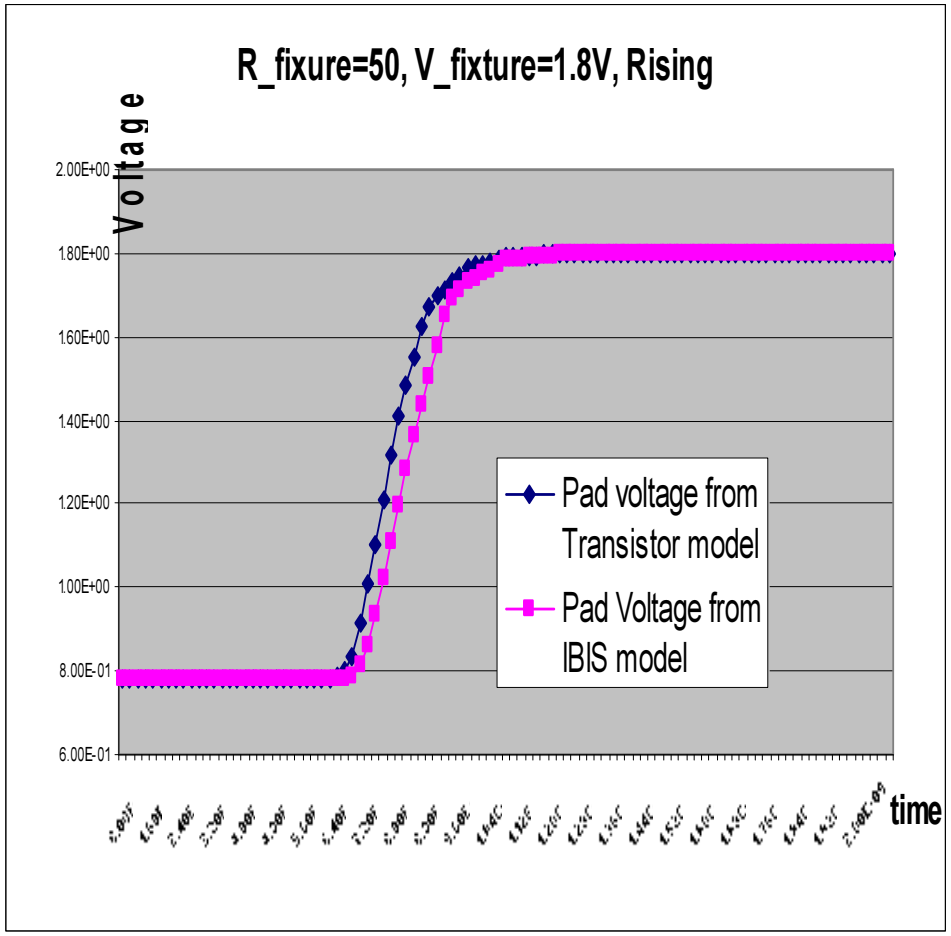
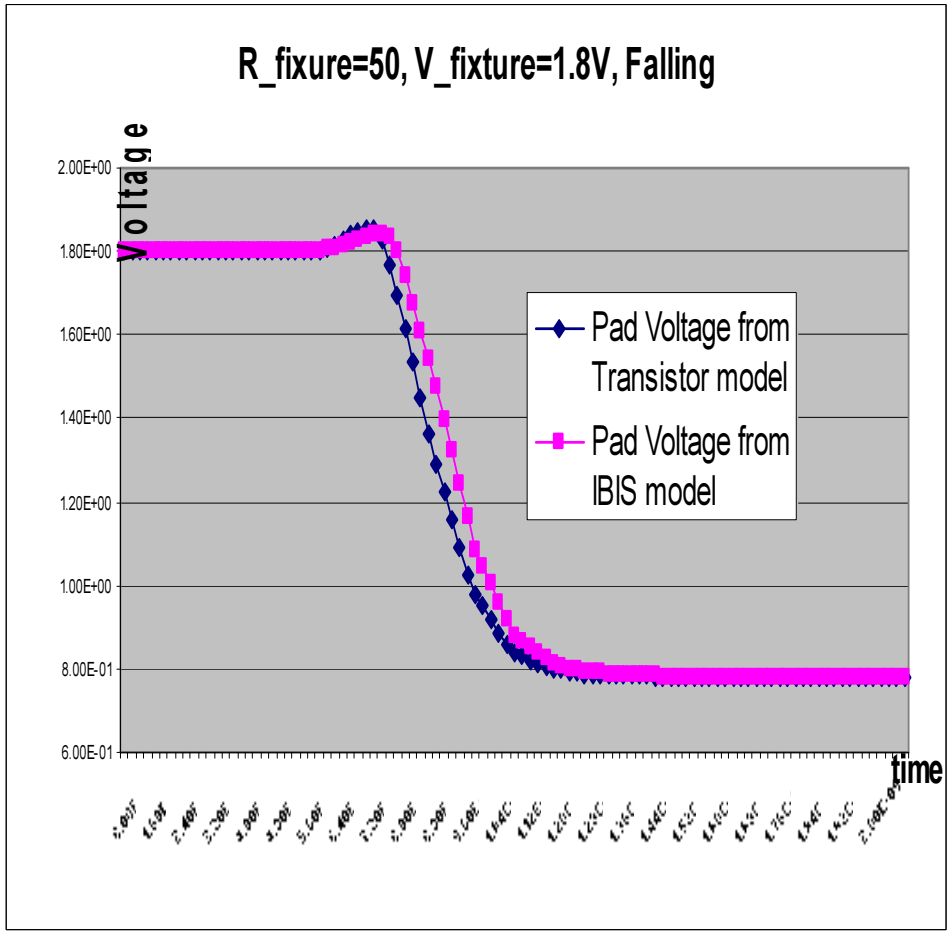
- An impedance-controlled 1.8V HSTL output buffer is used as an example
- IBIS model is extracted from HSPICE transistor model
- Both Ideal and Non-ideal power supply cases are analyzed
- HSPICE B-element is used to simulate the IBIS model
- *BIRD95* IvsT info is implemented with ideal current source in parallel with B-element
- Both cases with and w/o Z_VDDQ are analyzed

Evidence of the Problems with Current IBIS Model: I/O Voltage (Ideal Power Supply)





Evidence of the Problems with Existing IBIS Model: Total Current from Power Pin (Ideal Power Supply) (1)

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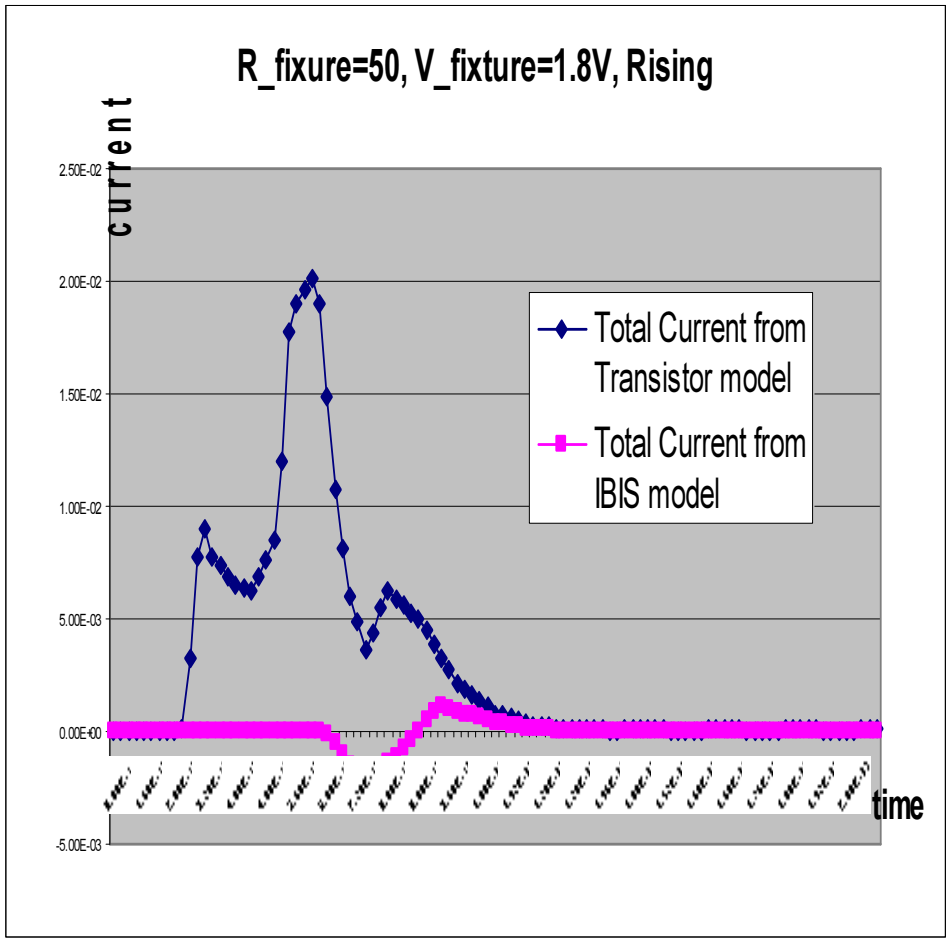

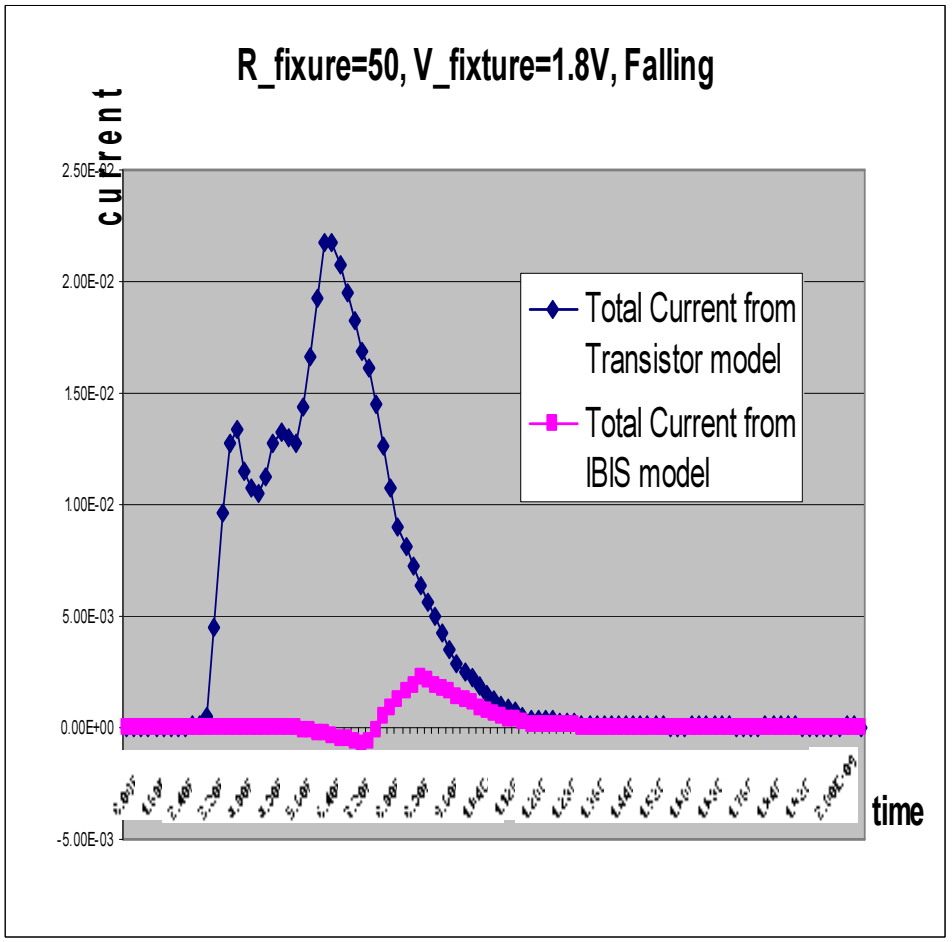

Evidence of the Problems with Existing IBIS Model: Total Current from Power Pin (Ideal Power Supply) (2)

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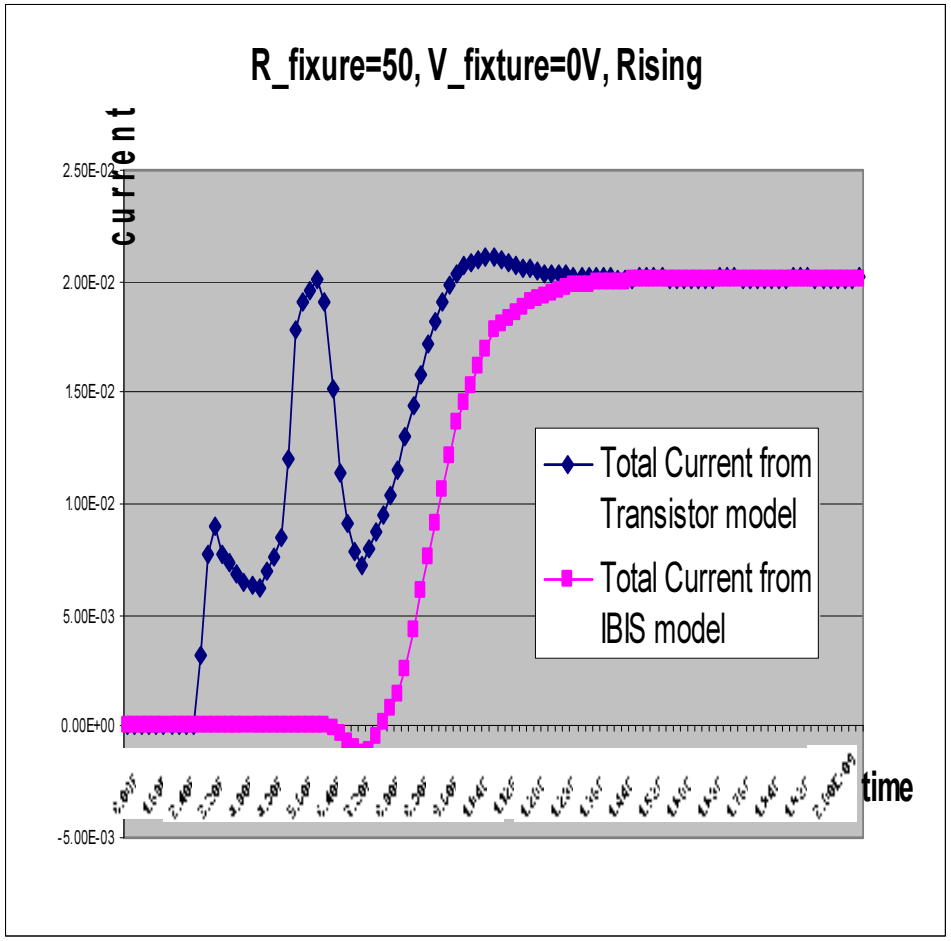
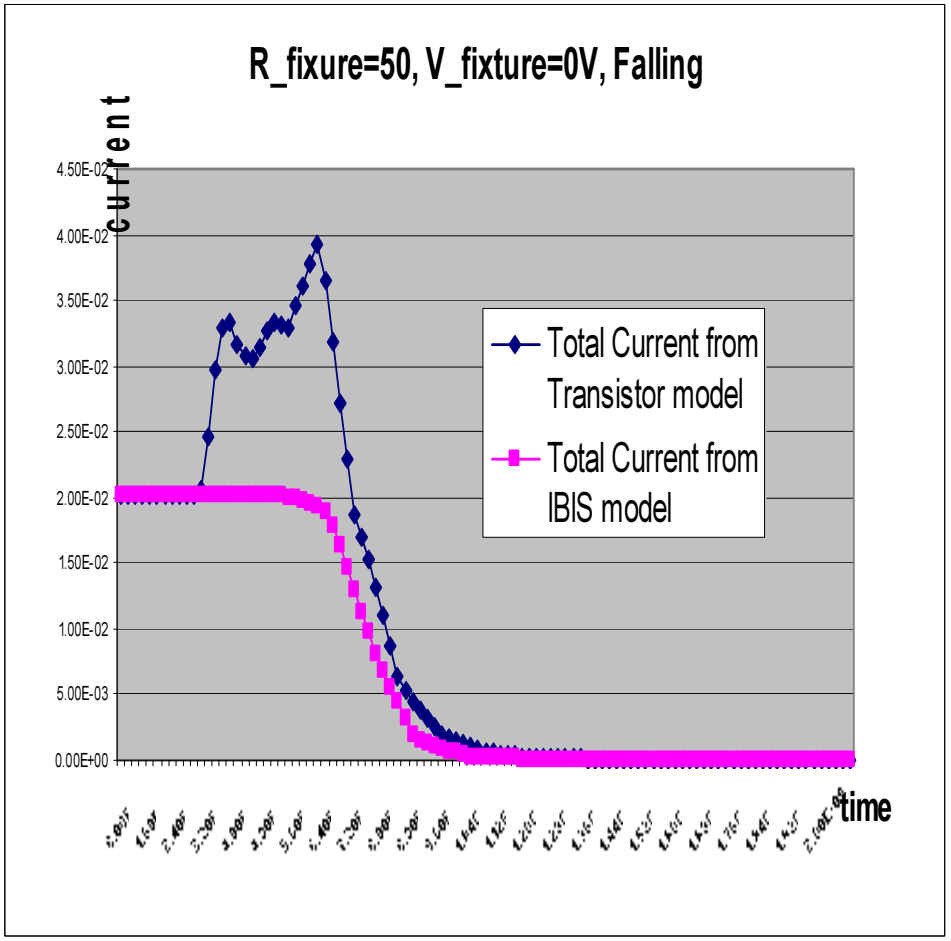
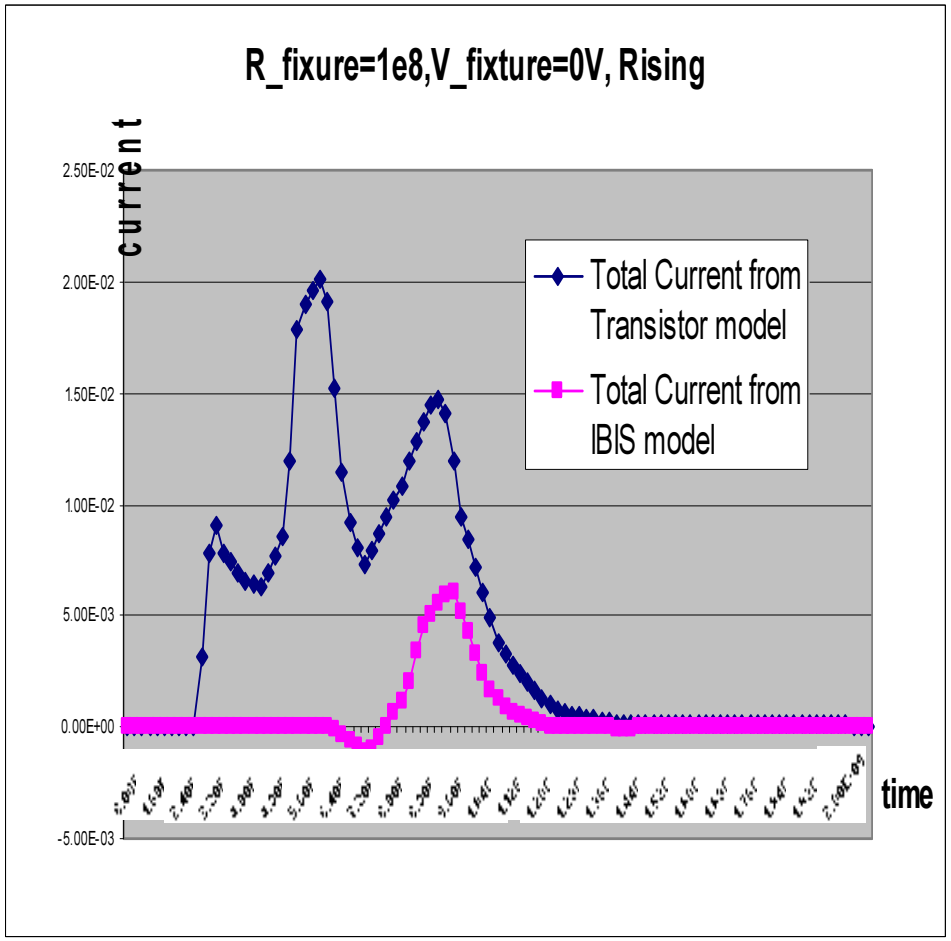
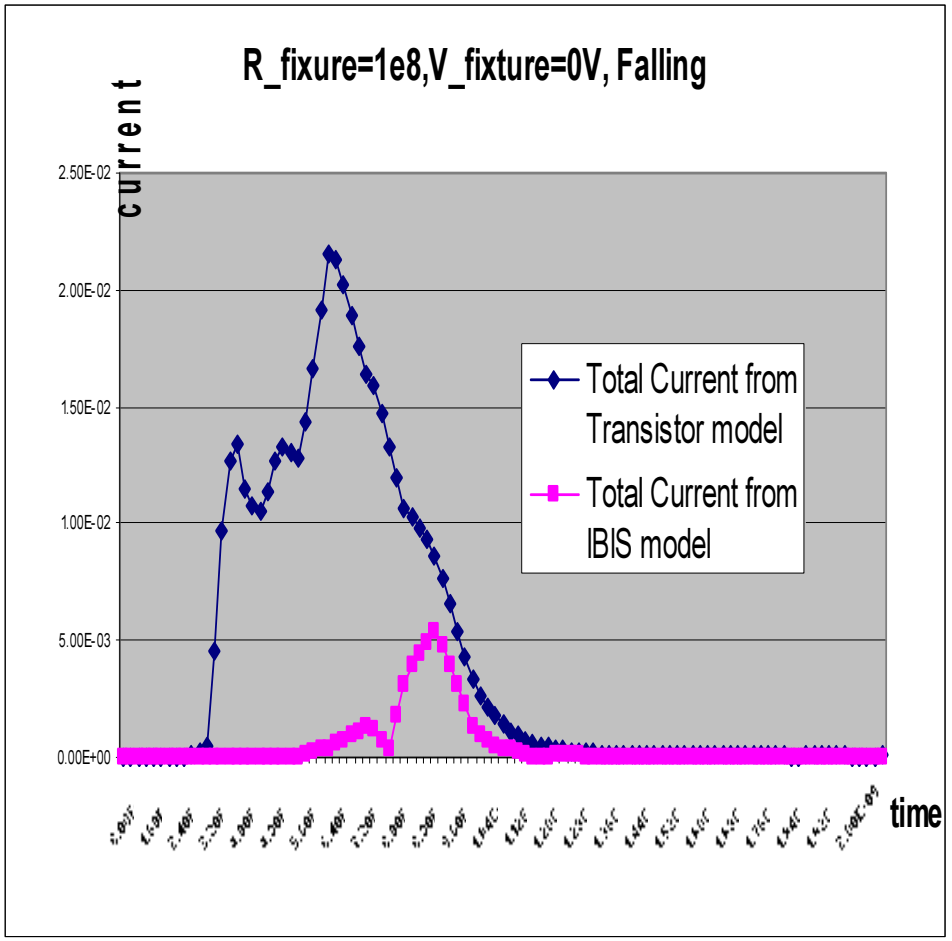


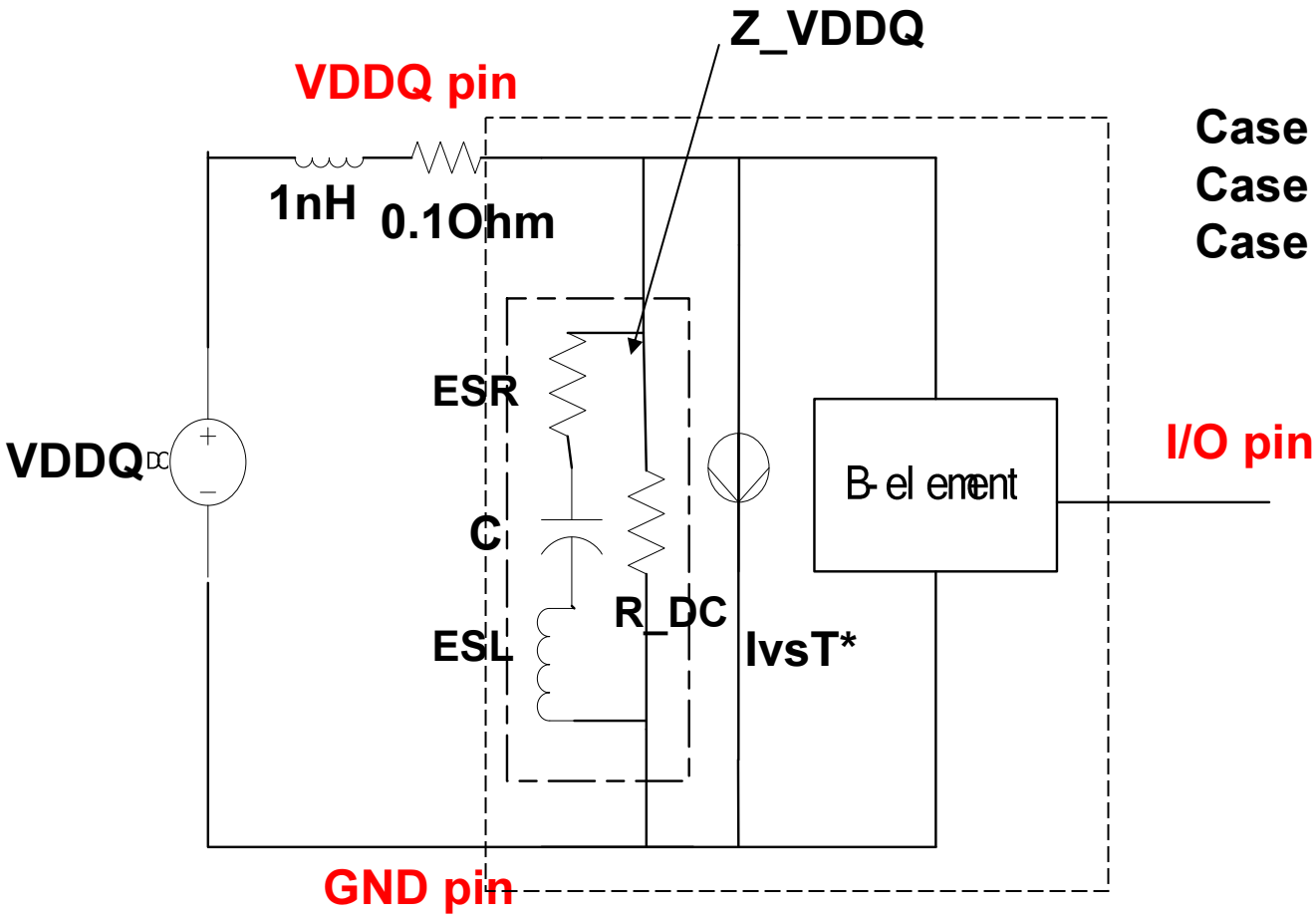


Evidence of the Problems with Existing IBIS Model: Total Current from Power Pin (Ideal Power Supply) (3)





BIRD95 implementation schematics



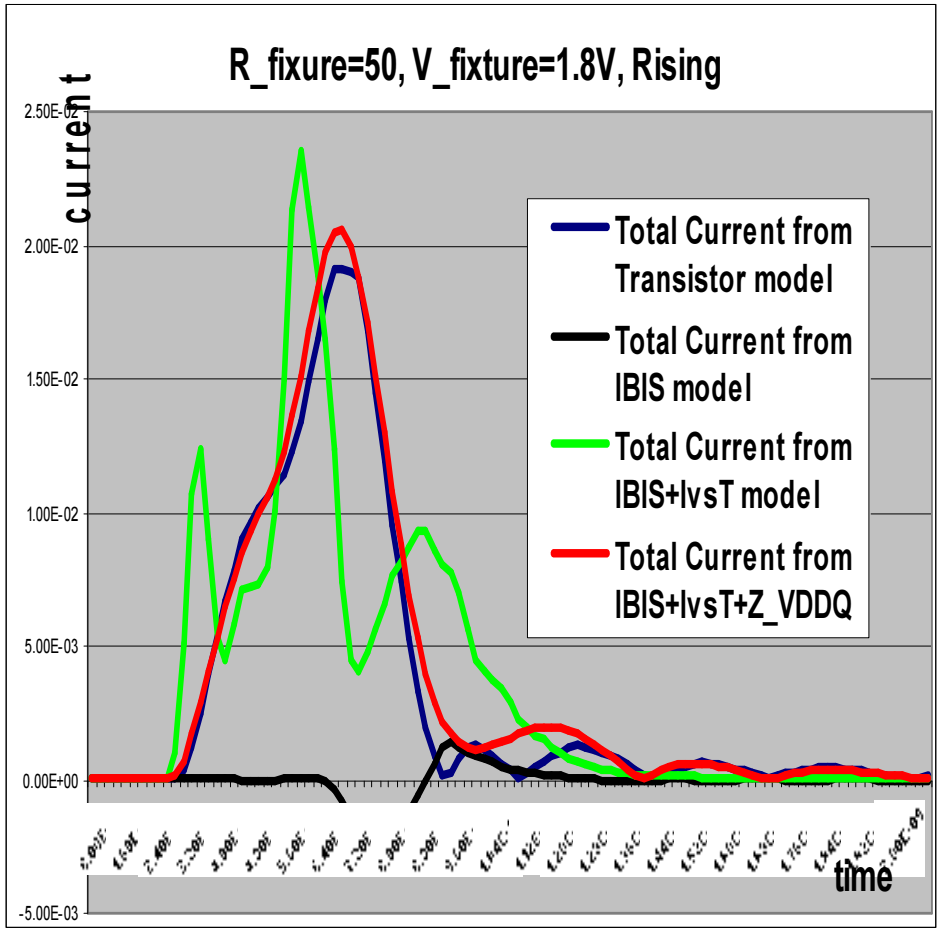
Case 1: B-element only
Case 2: B + IvsT*
Case 3: B+IvsT*+Z_VDDQ

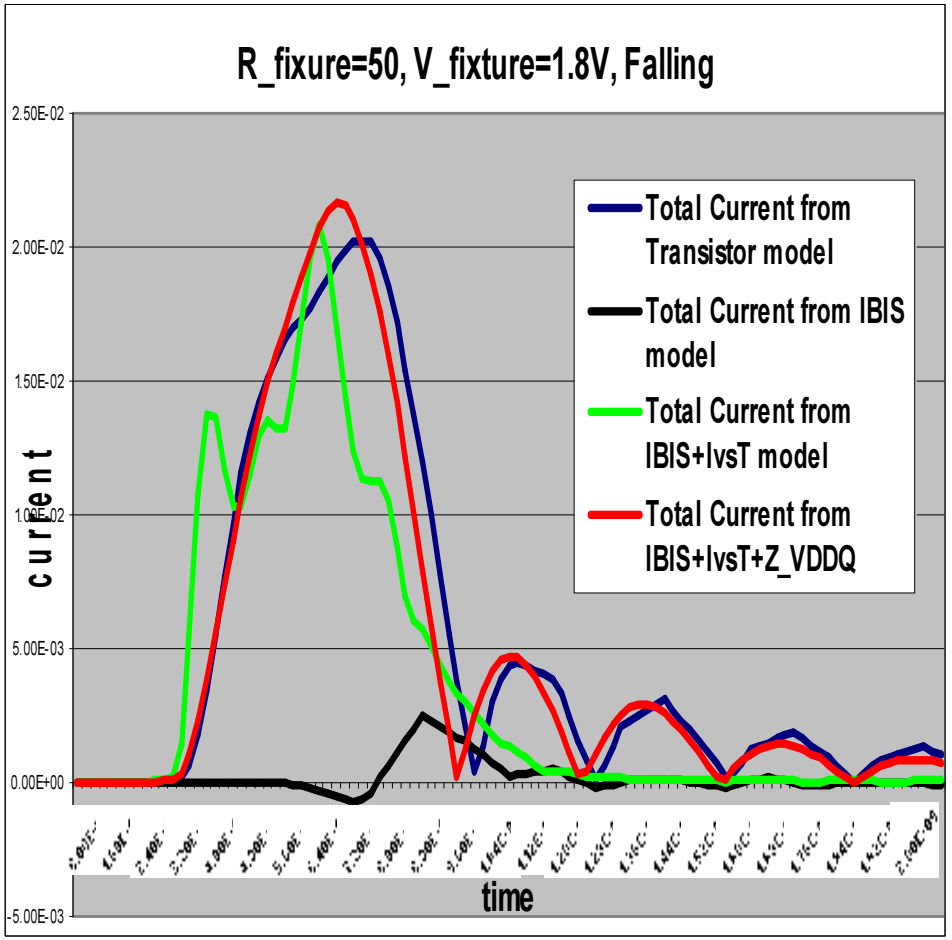
Note: IvsT* is different with IvsT table in BIRD95, but it is derived from IvsT table

IvsT* and parasitic components

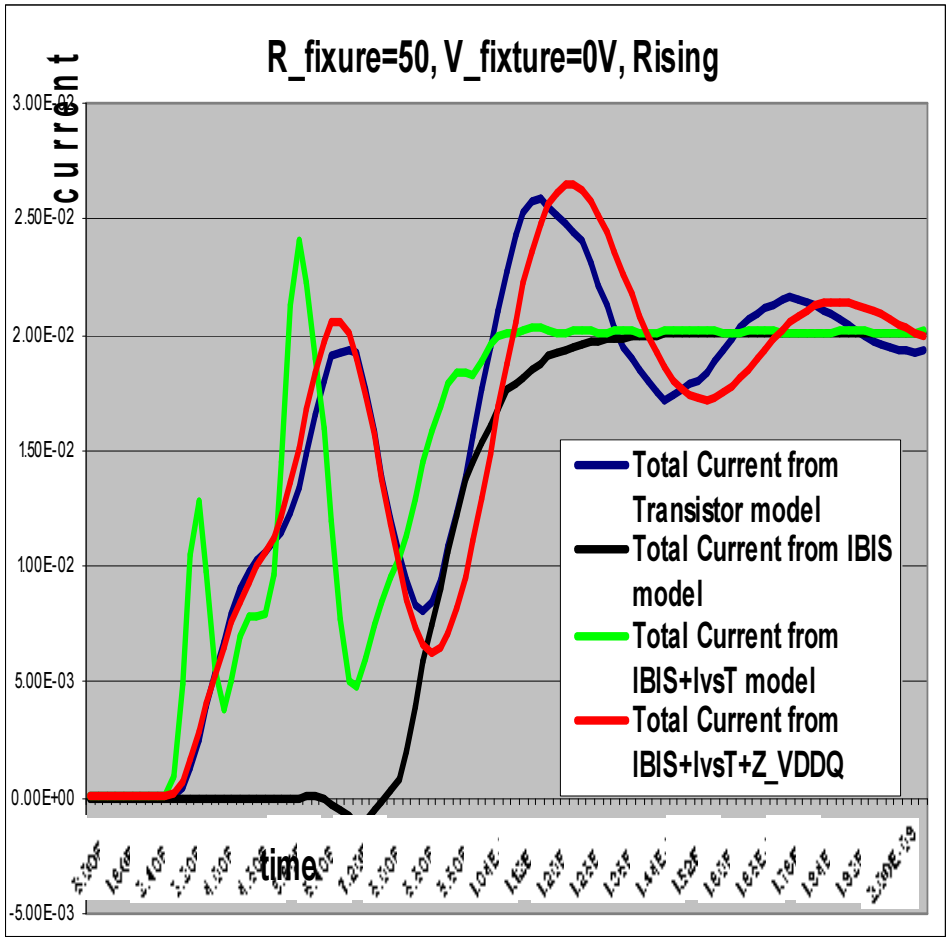
- IvsT*=IvsT (*BIRD95* table)-IvsT**
- IvsT** is the total current from the VDDQ by using existing IBIS model with Z_VDDQ connected in parallel.
- All currents here are under ideal power supply and standard loading conditions.
- Two sets of IvsT* associated with rising and falling edge were derived by averaging different loading conditions in our examples. More complicated model could be derived from 6 IvsT* tables to compensate the load variation effects.
- ESR, ESL, C and R_dc can be extracted from Z_VDDQ to match the impedance in frequency domain
- The ESR, ESL, C and R_dc is just one example of the possible circuits to match Z_VDDQ. It could cover majority I/O buffers' on-die parasitic components.

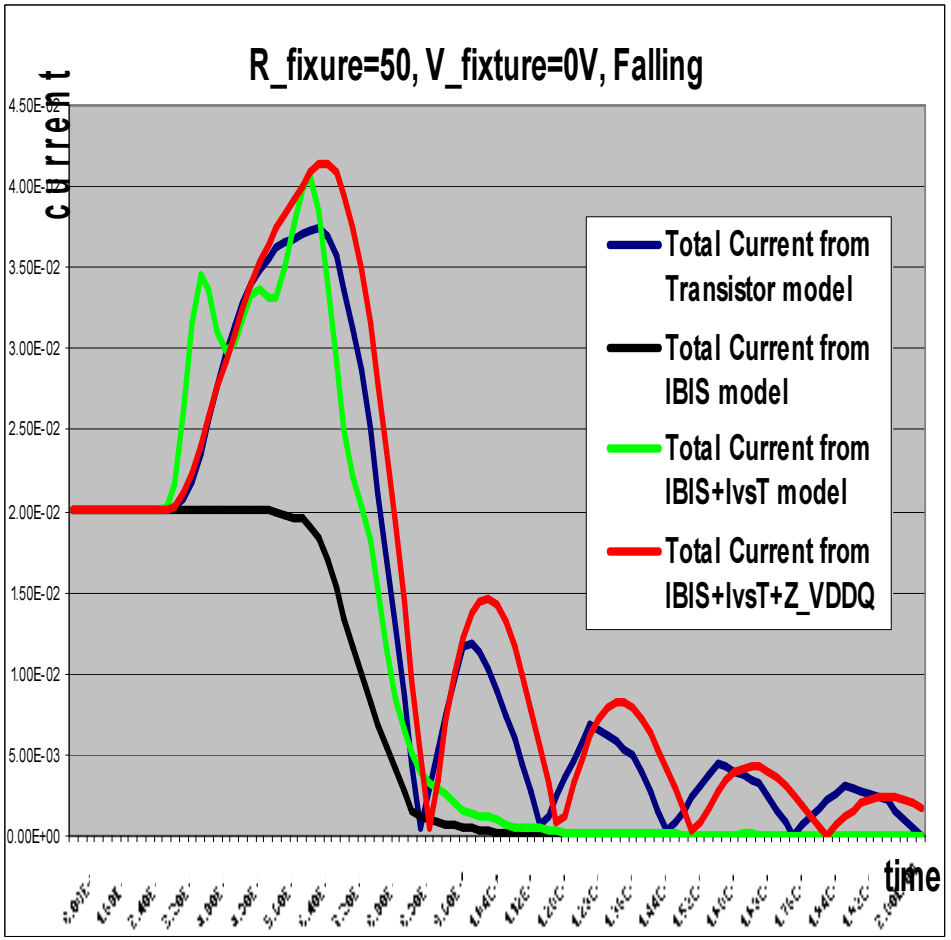
Total Current from VDDQ pin





Total Current from VDDQ pin (cont'd)





Total Current from VDDQ pin (cont'd)

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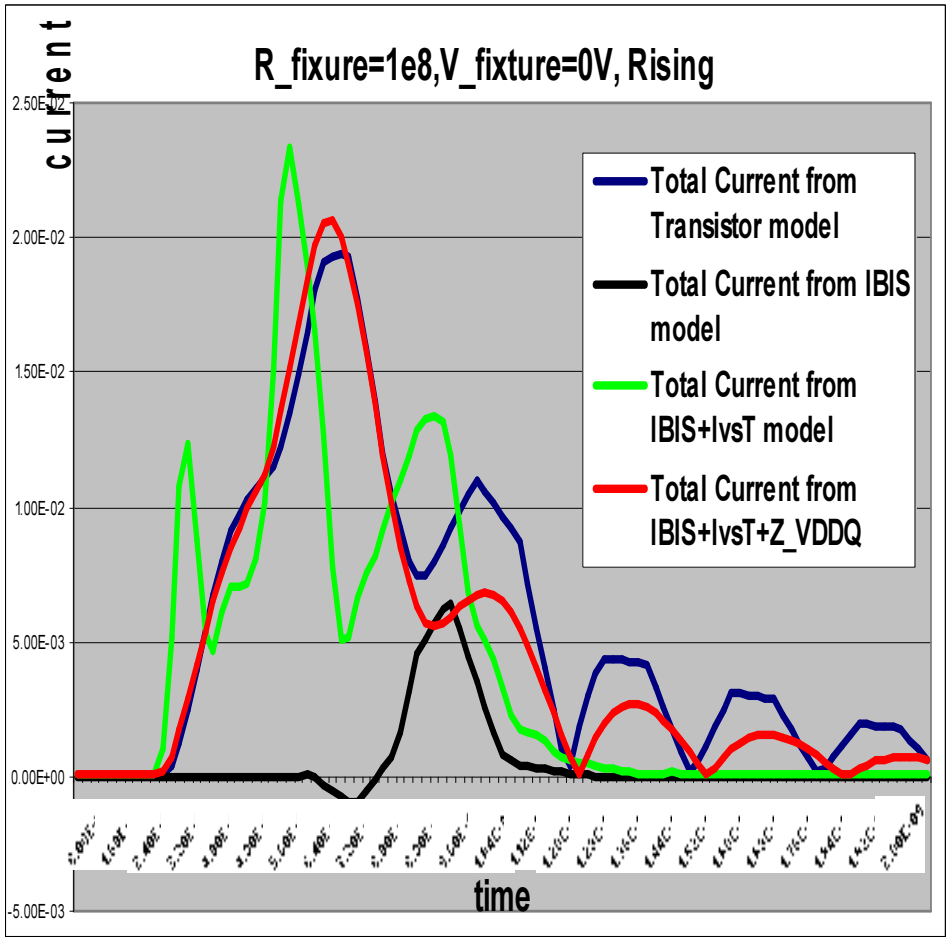
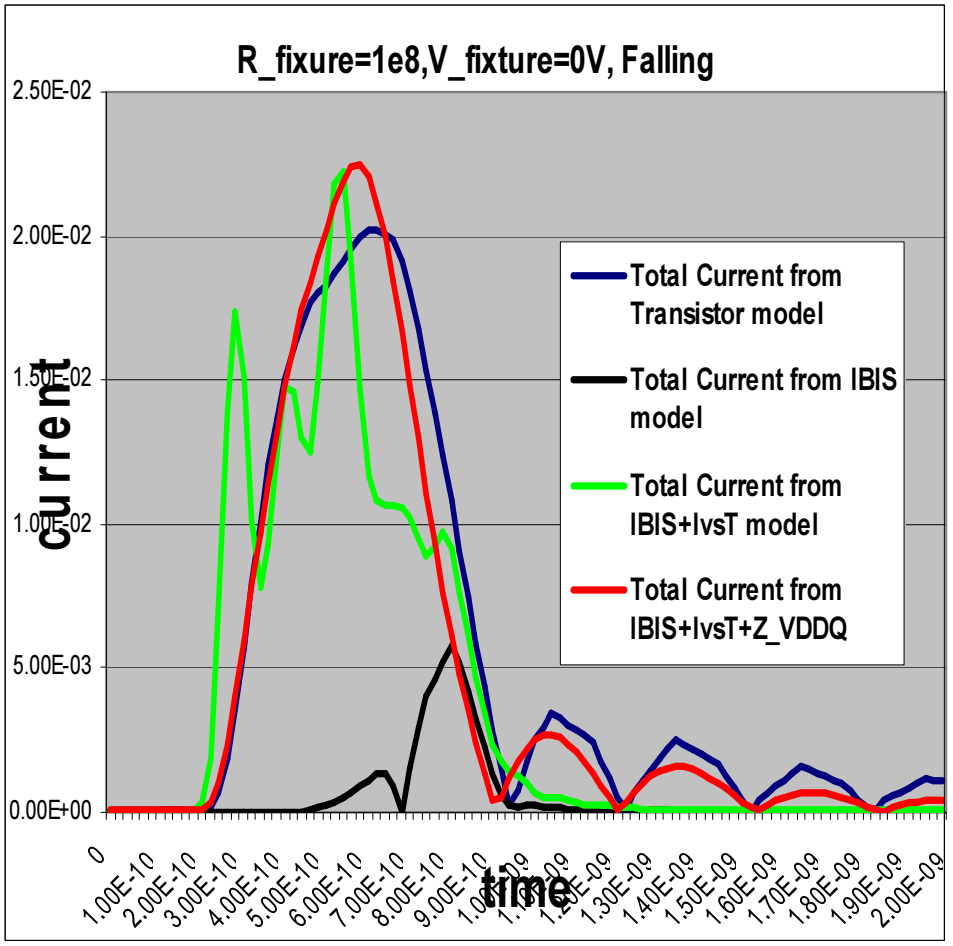
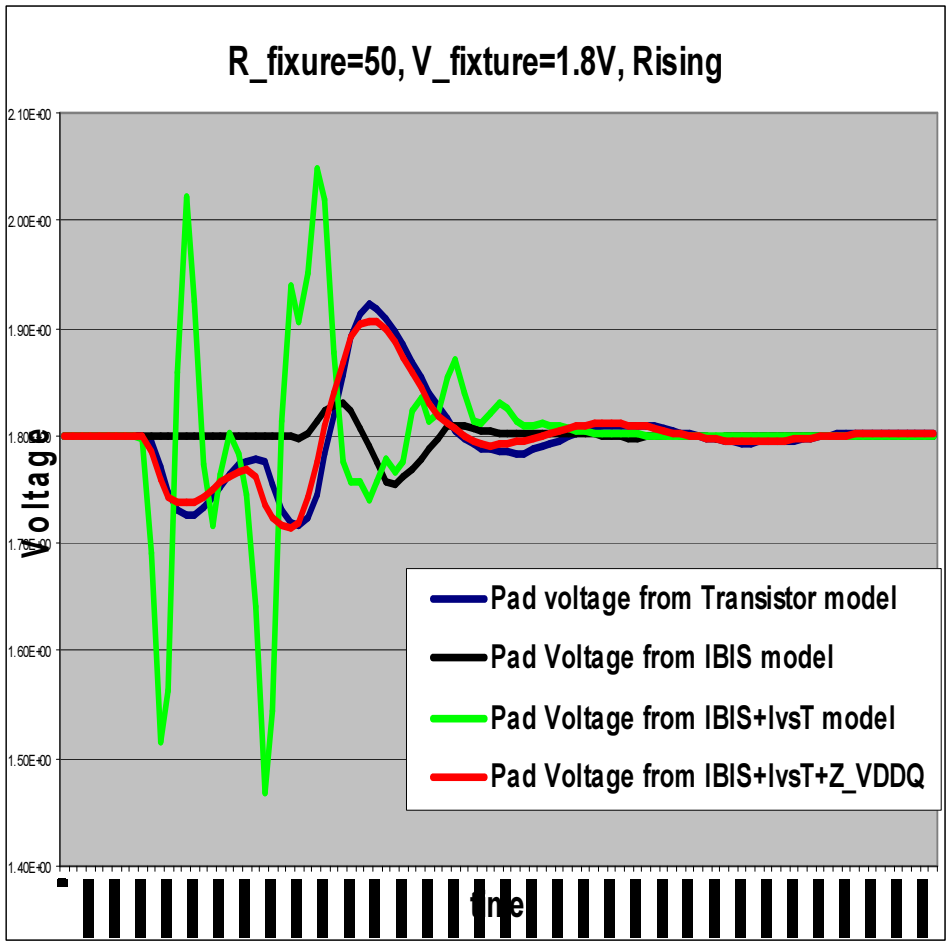
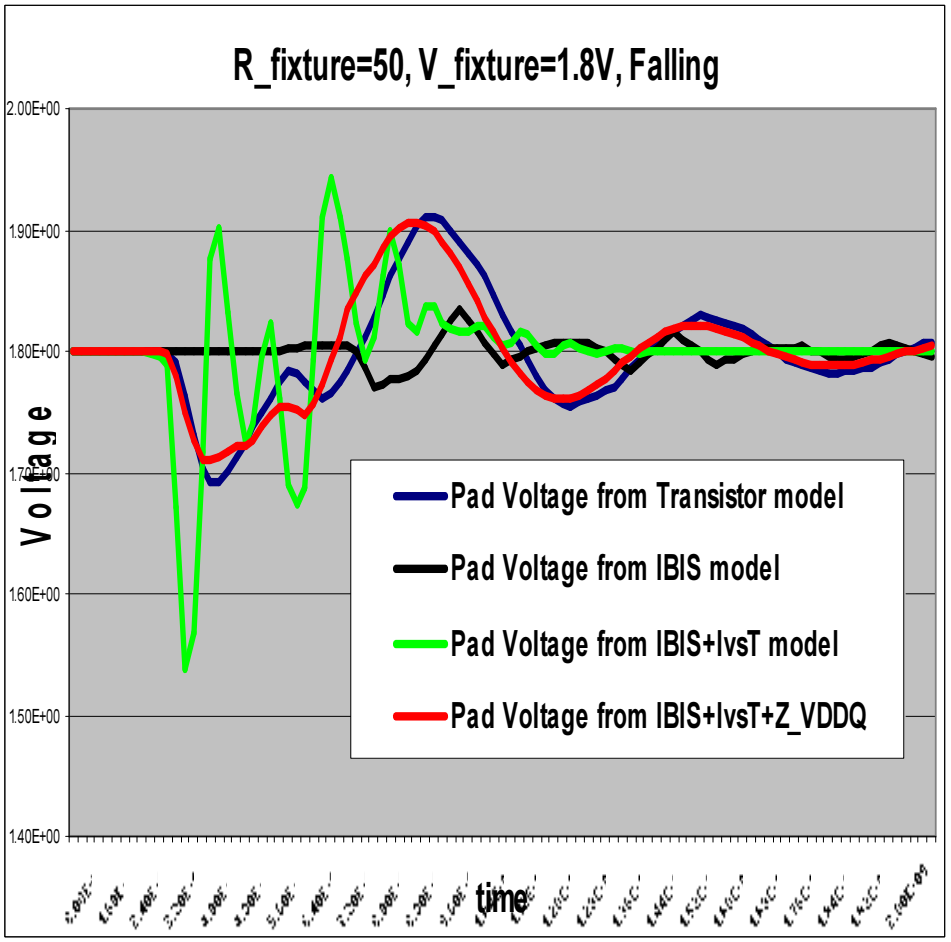


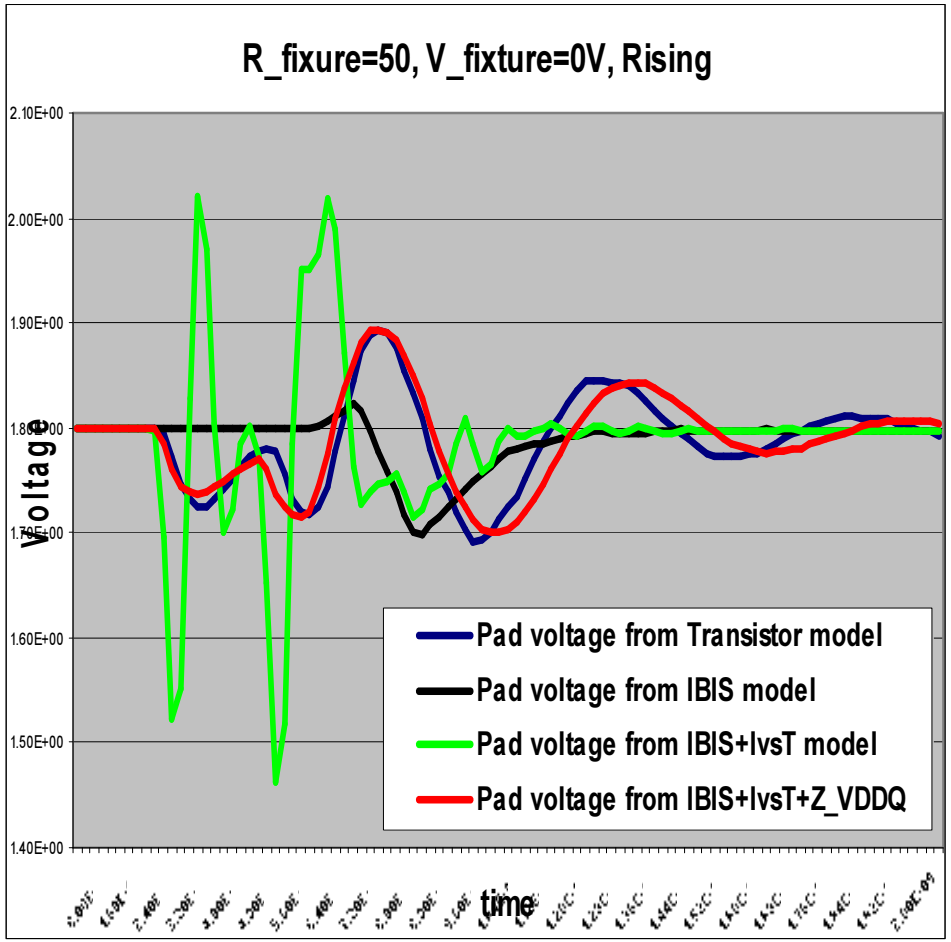


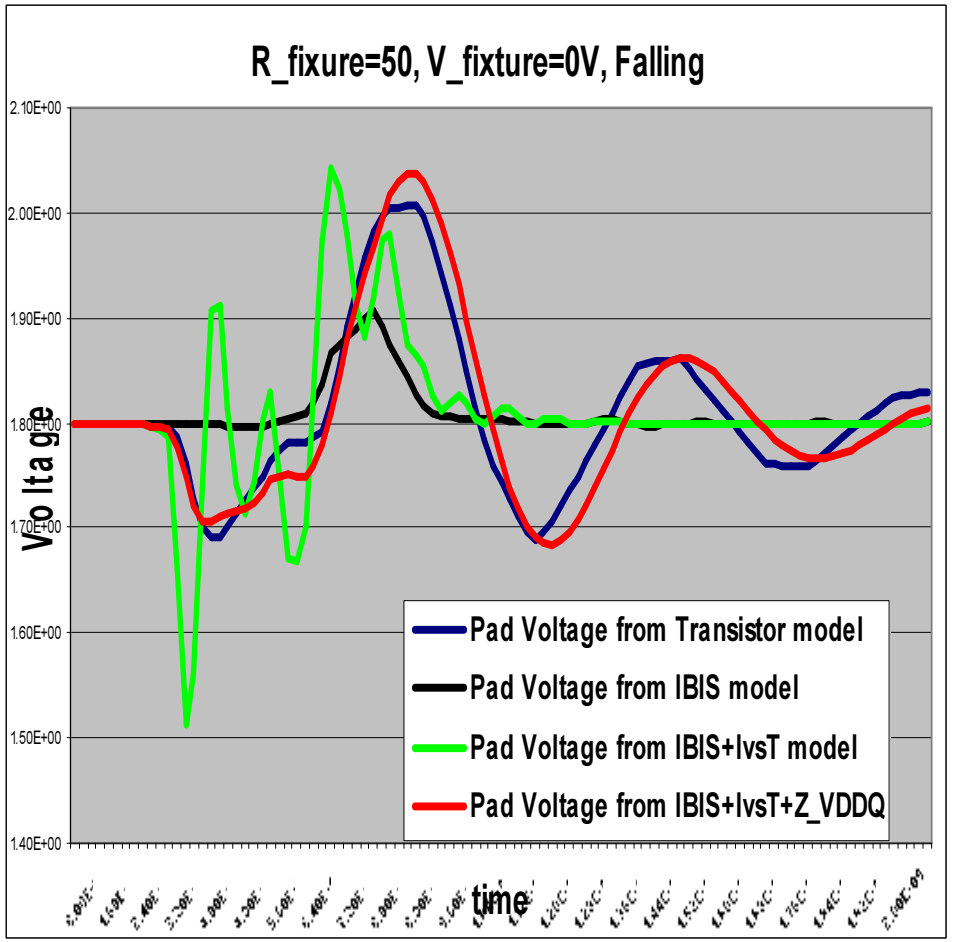
Voltage Noise at VDDQ Pin



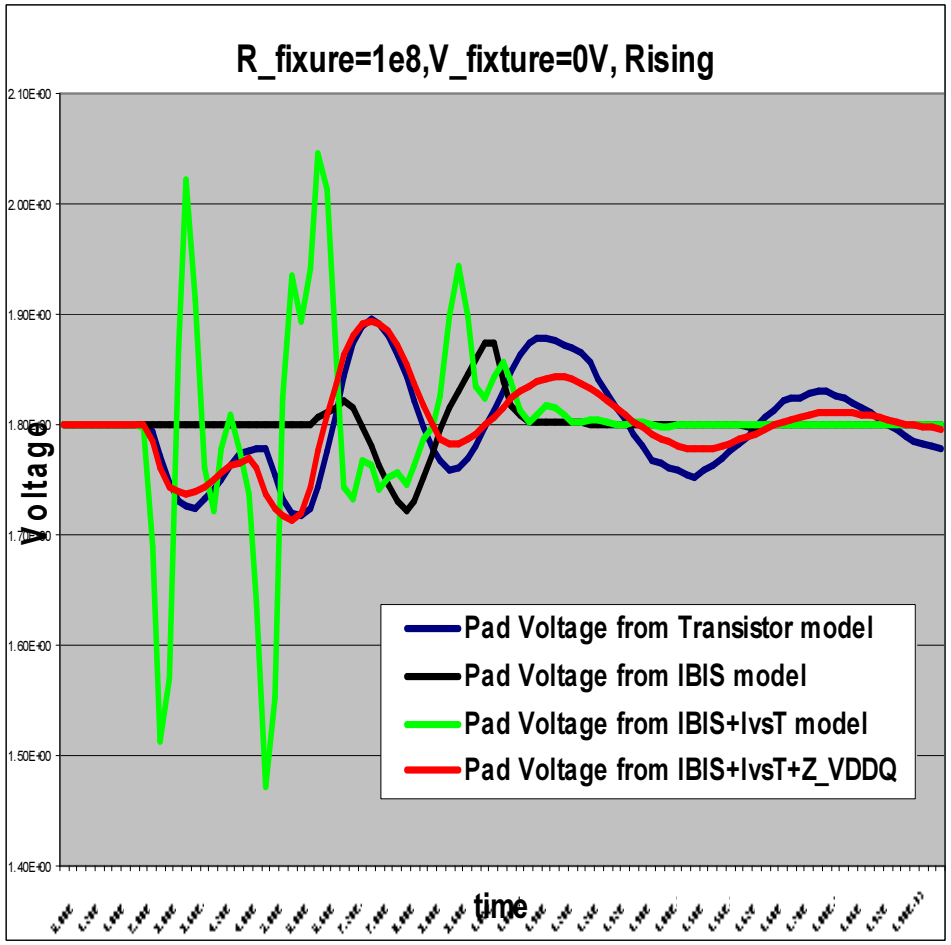


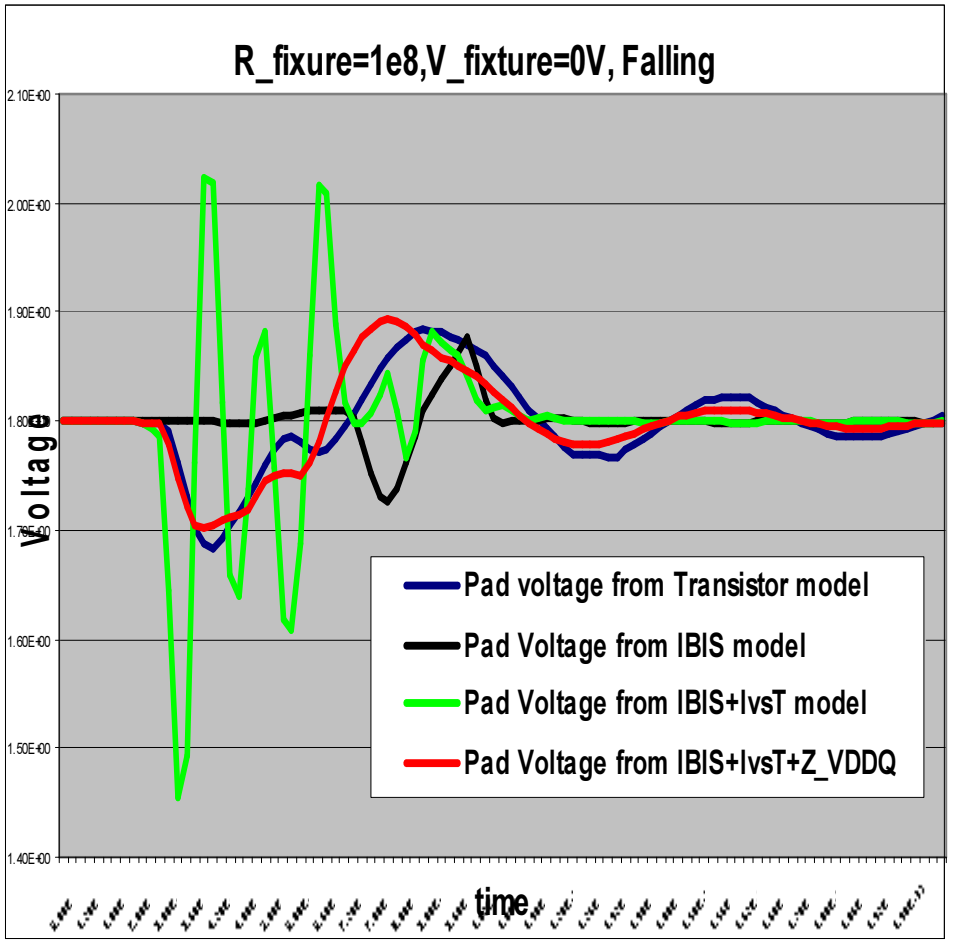
Voltage Noise at VDDQ Pin (cont'd)



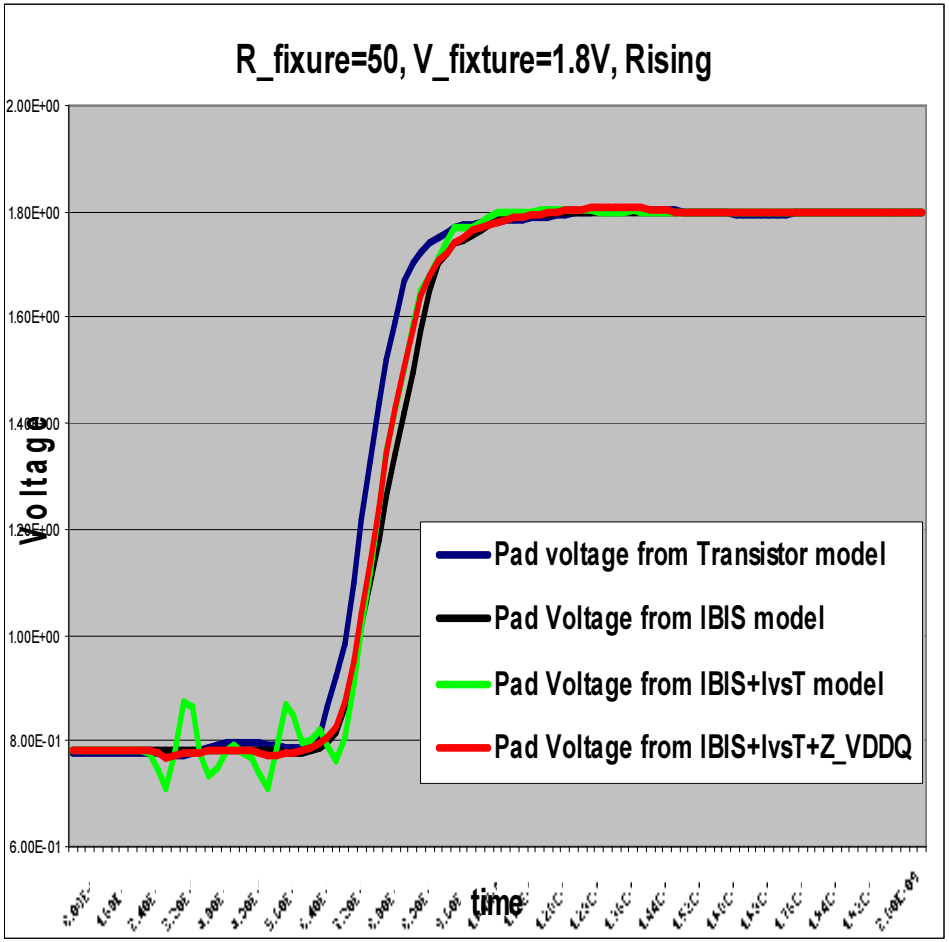


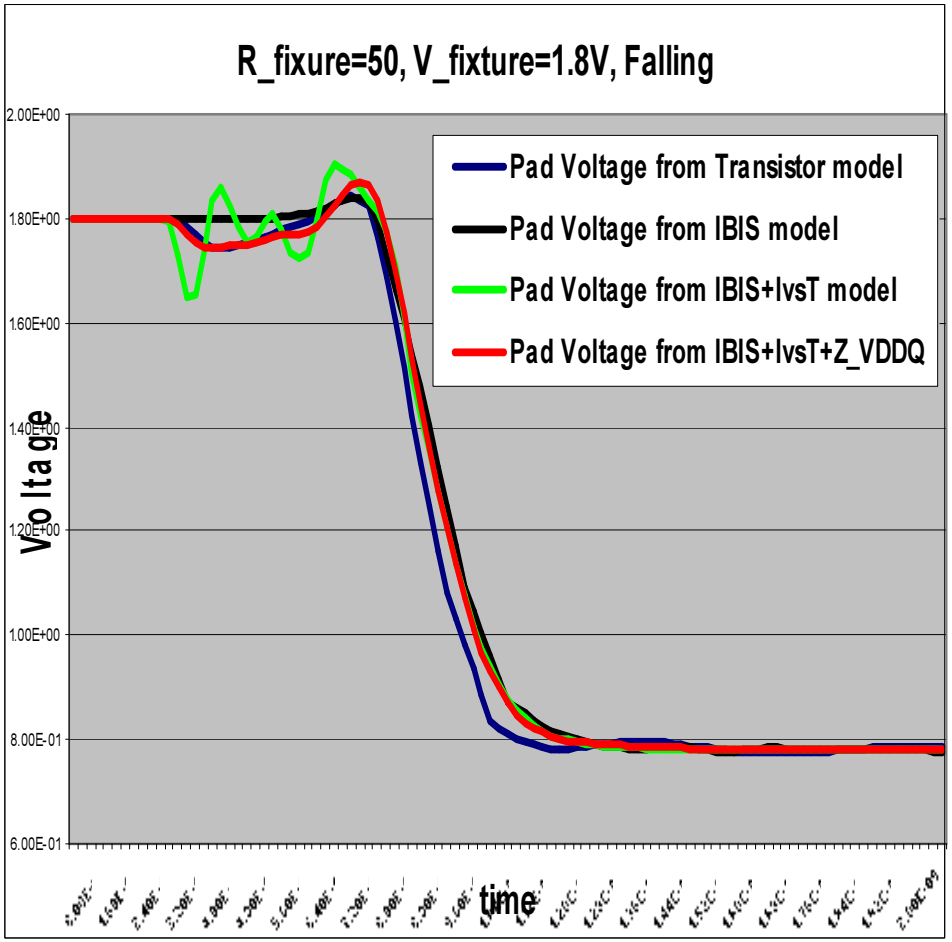
Voltage Noise at VDDQ Pin (cont'd)



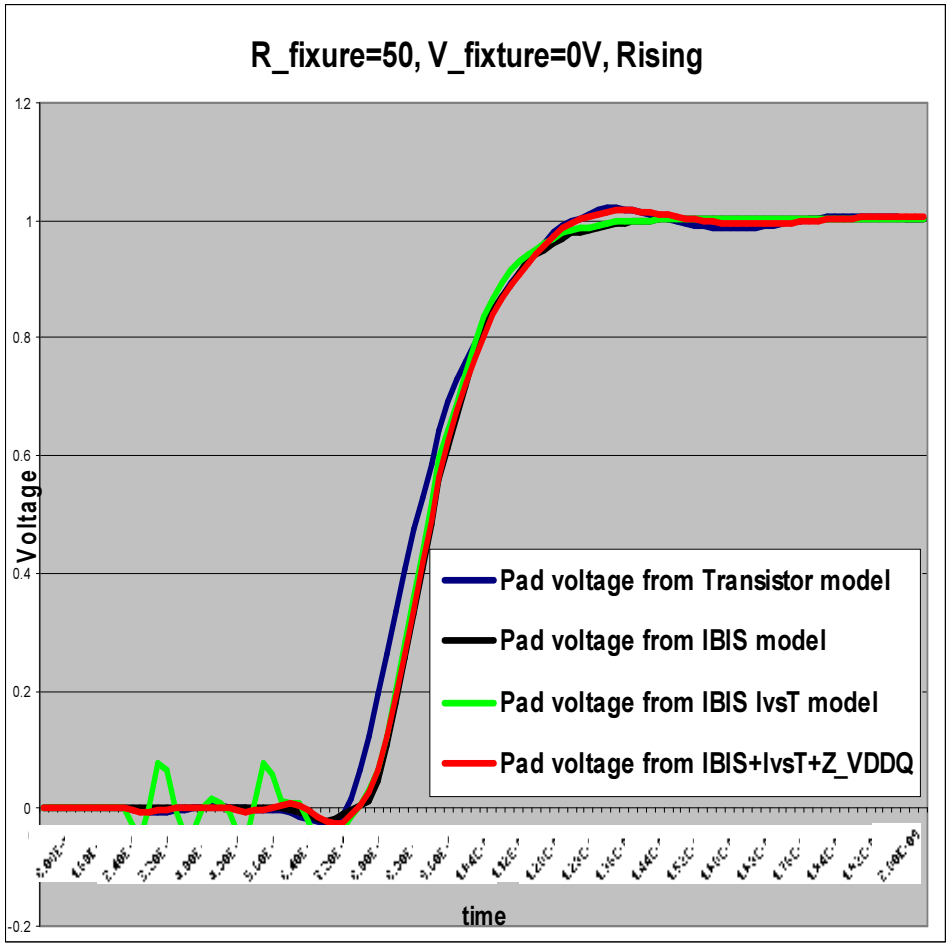


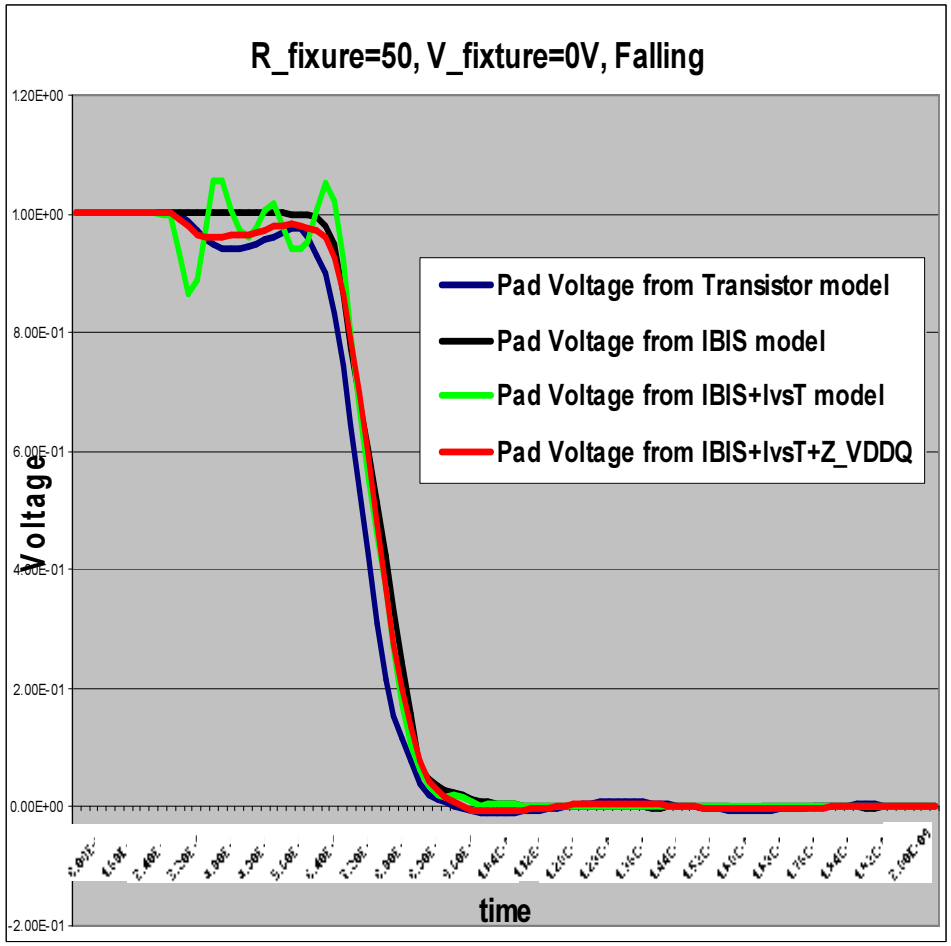
Voltage at Signal Pin



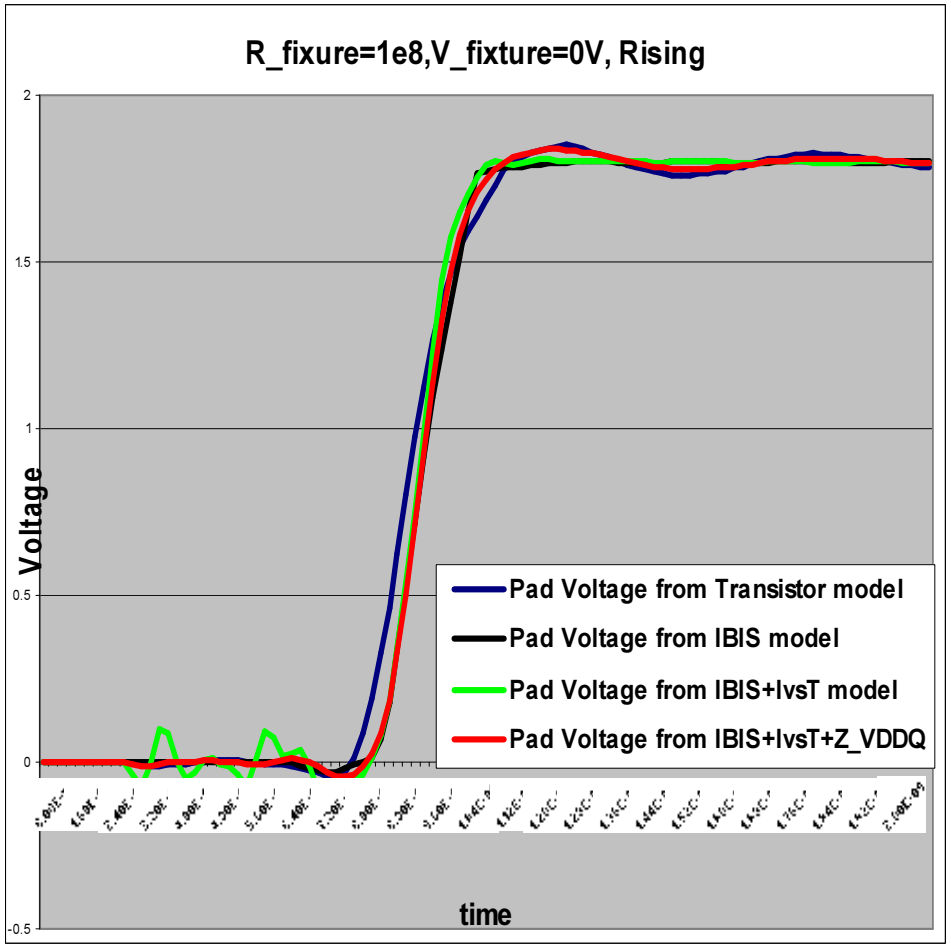


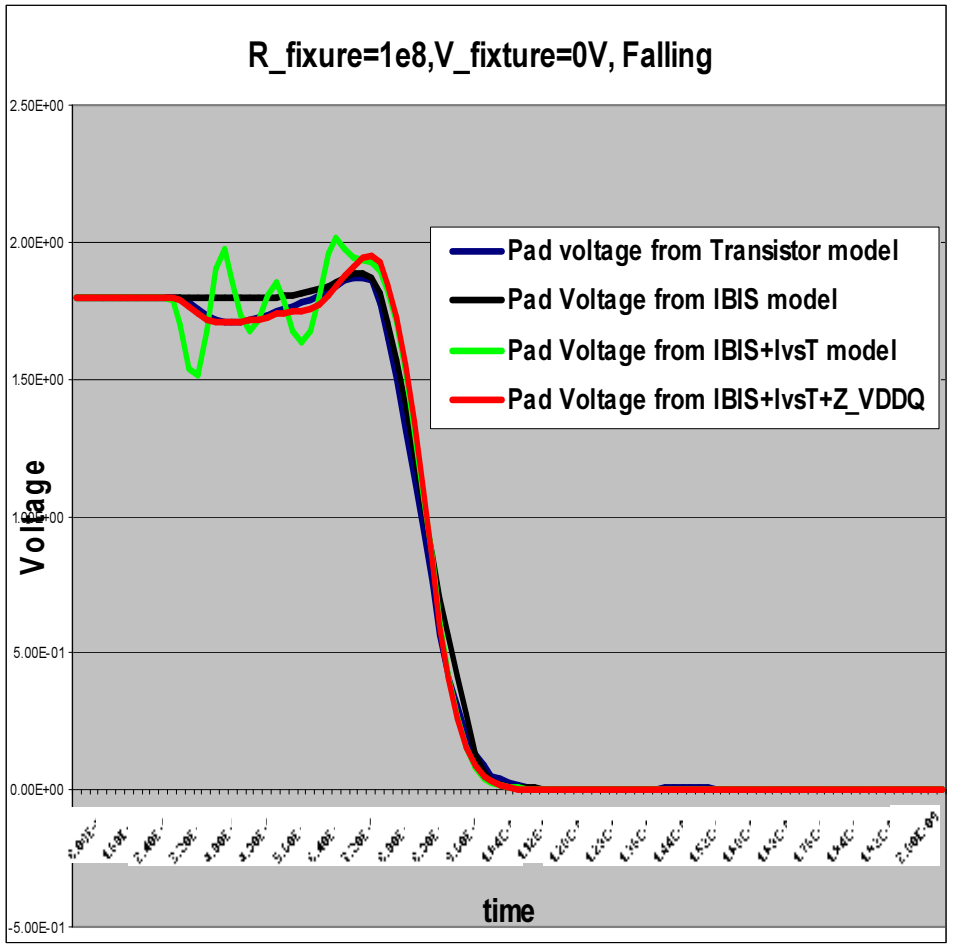
Voltage at Signal Pin (cont'd)





Voltage at Signal Pin (cont'd)





Conclusions

- ***BIRD95*** **can be easily implemented in HSPICE and other EDA tools**
- ***BIRD95*** **can greatly improve the simulation accuracy of power noise in SSN and other non-ideal power supply simulations with IBIS models**
- **On-die Impedance between the power and ground is very important in power related simulations**
- ***BIRD95*** **provides a feasible solution to evaluate the power noise impact on signal timing**

Questions and Answers

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