IBIS Summit 2005

IBIS Power/Ground Modeling of LSI Core Logic with High-Pin Count Package for EMI and PI

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****NEC Production Technology Laboratories**

Outlines

1. Introduction
2. Modeling of Core Logic Power/Ground for EMI Simulation
3. Modeling of High-Pin Count Package
4. Conclusion

1. Introduction

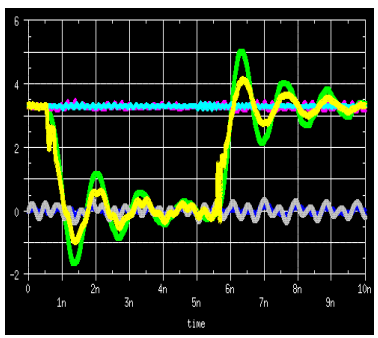
PI and EMI Simulation

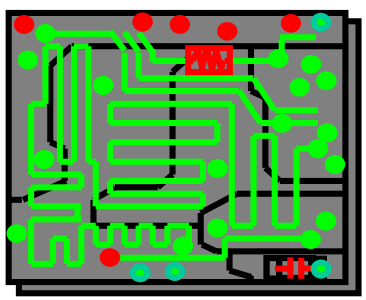
PI

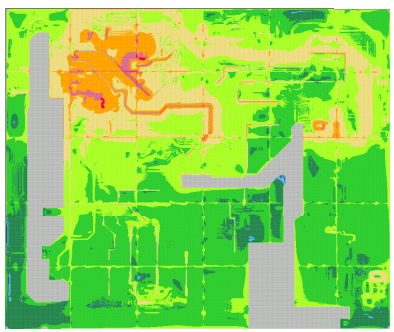
Power Integrity

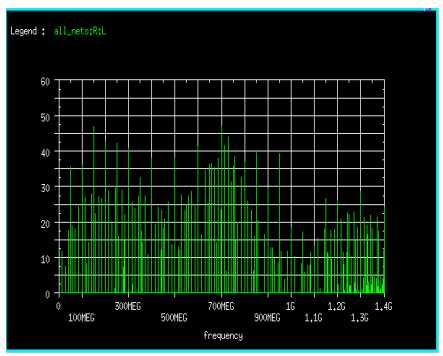
EMI

Electromagnetic Interference

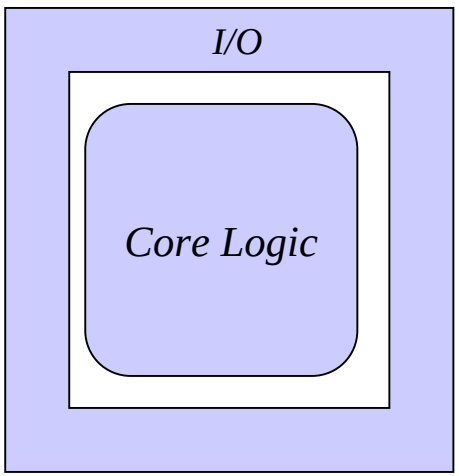








Two Types of LSIs



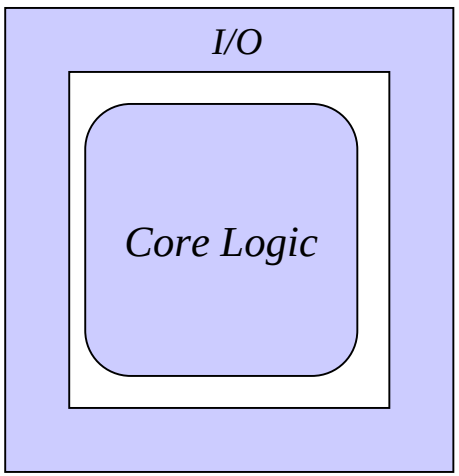
LSI for Digital Consumer/Auto Mobile

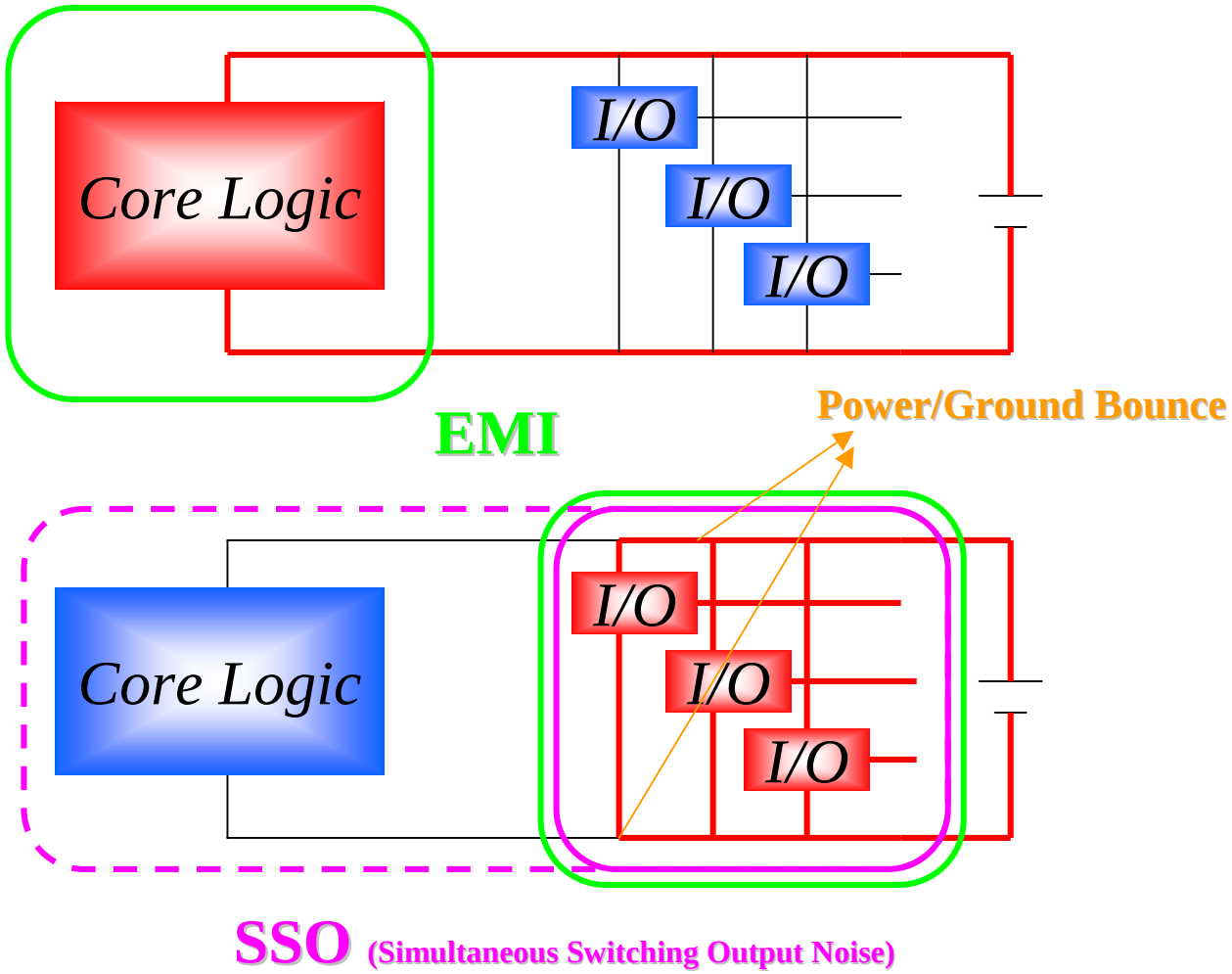
	Total Power/Current	*Clock Freq*	*Voltage*
Core Logic	***High***	***High***	***Low***
I/O	*Low*	*Low*	*High*

Driver IC

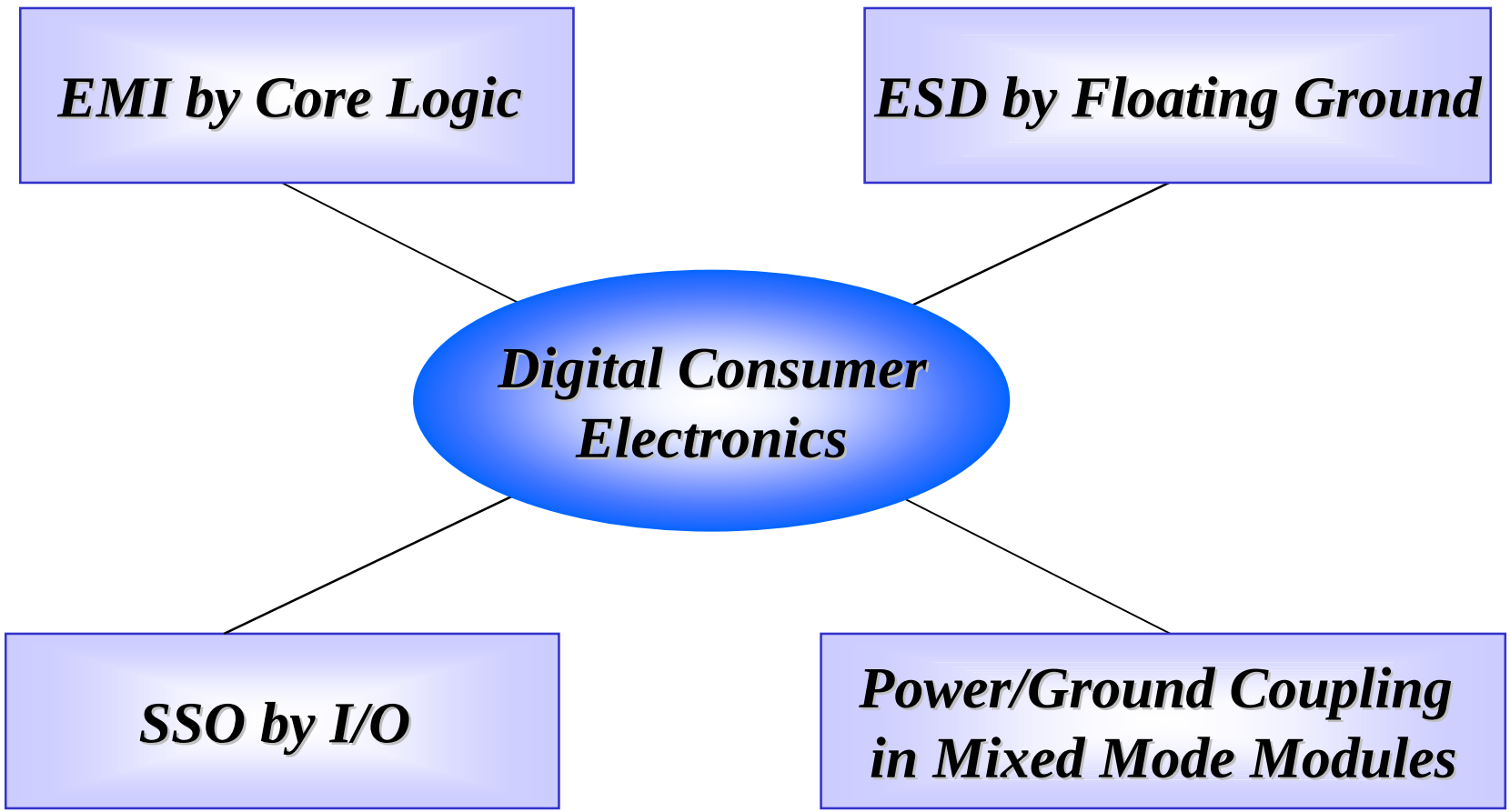
	Total Power/Current	*Clock Freq*	*Voltage*
Core Logic	*Low*	*Same/High*	*Low*
I/O	***High***	***Low***	***High***

Dominant Currents

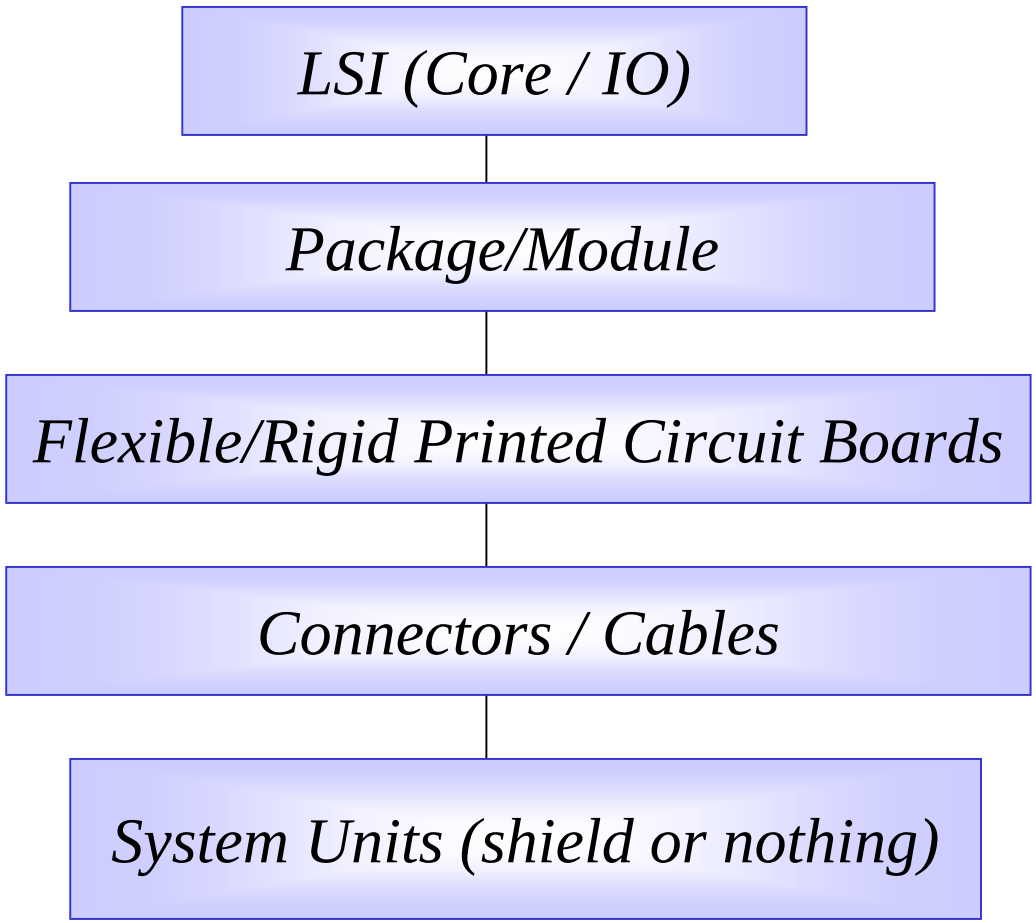




EMC in Digital Consumer Electronics



Non-Ideal Ground at Various Levels



Complex Power/Ground Phenomena

⇩

Simulators

⇩

Well-Balanced Model

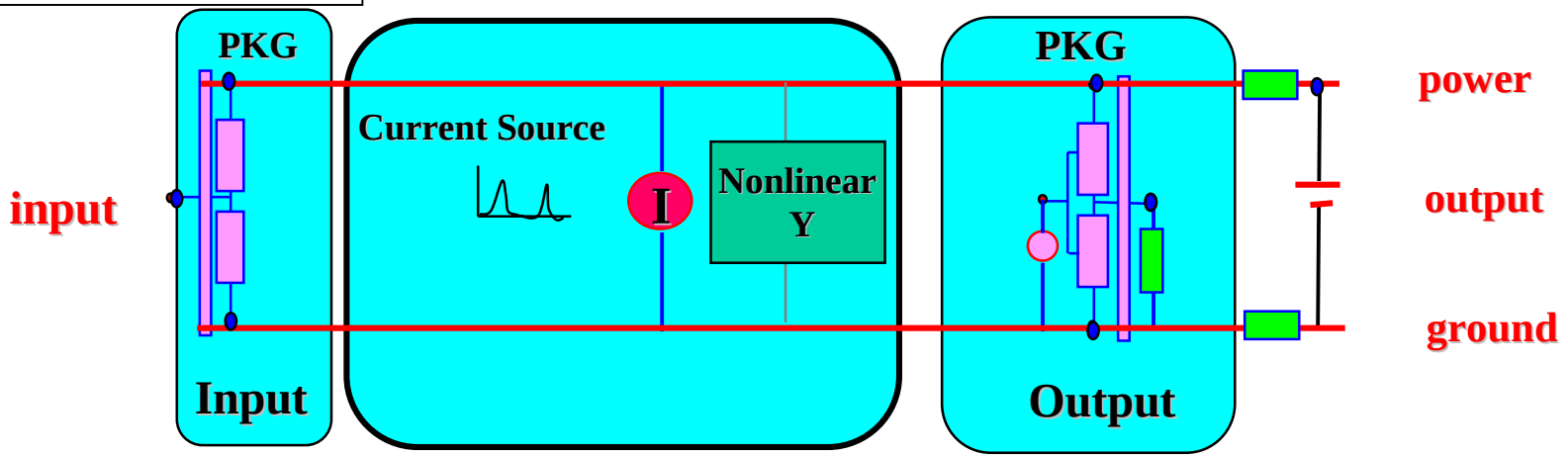
2. Modeling of Core Logic Power/Ground for EMI Simulation

System LSI for Digital Consumer Electronics

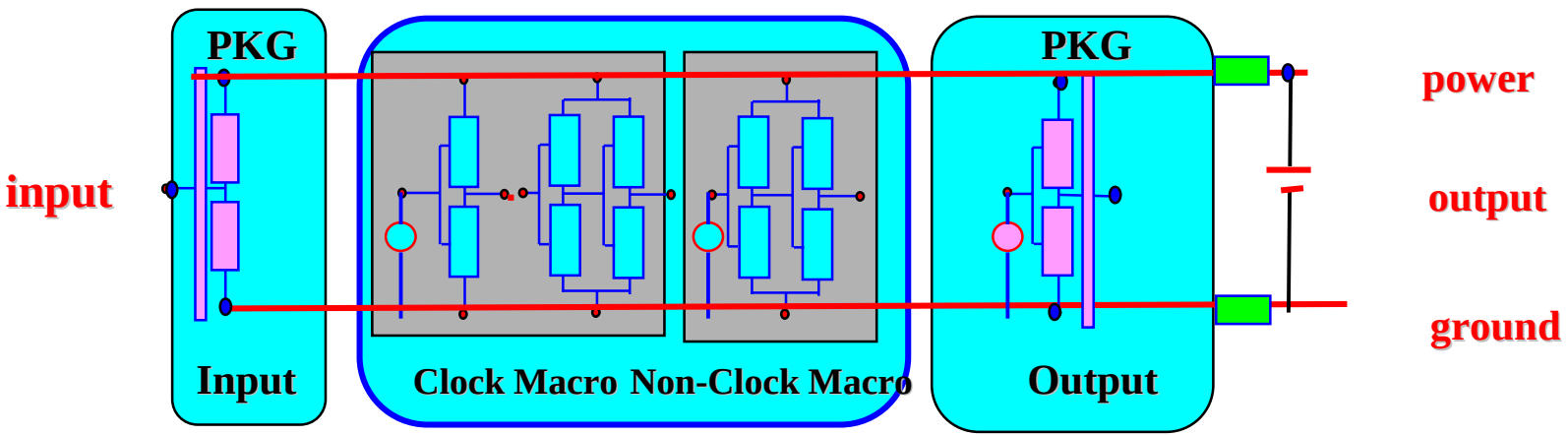
	Voltage	*Current*	*Clock Frequency*
Core Logic	***1.2V***	***2.5A***	***96MHz***
	1.8V	*0.2A*	*96MHz*
	2.5V	*0.5A*	*96MHz*
I/O	***3.3V***	***0.3A***	***48MHz***

Methods of Extraction of Core Logic Model for EMI

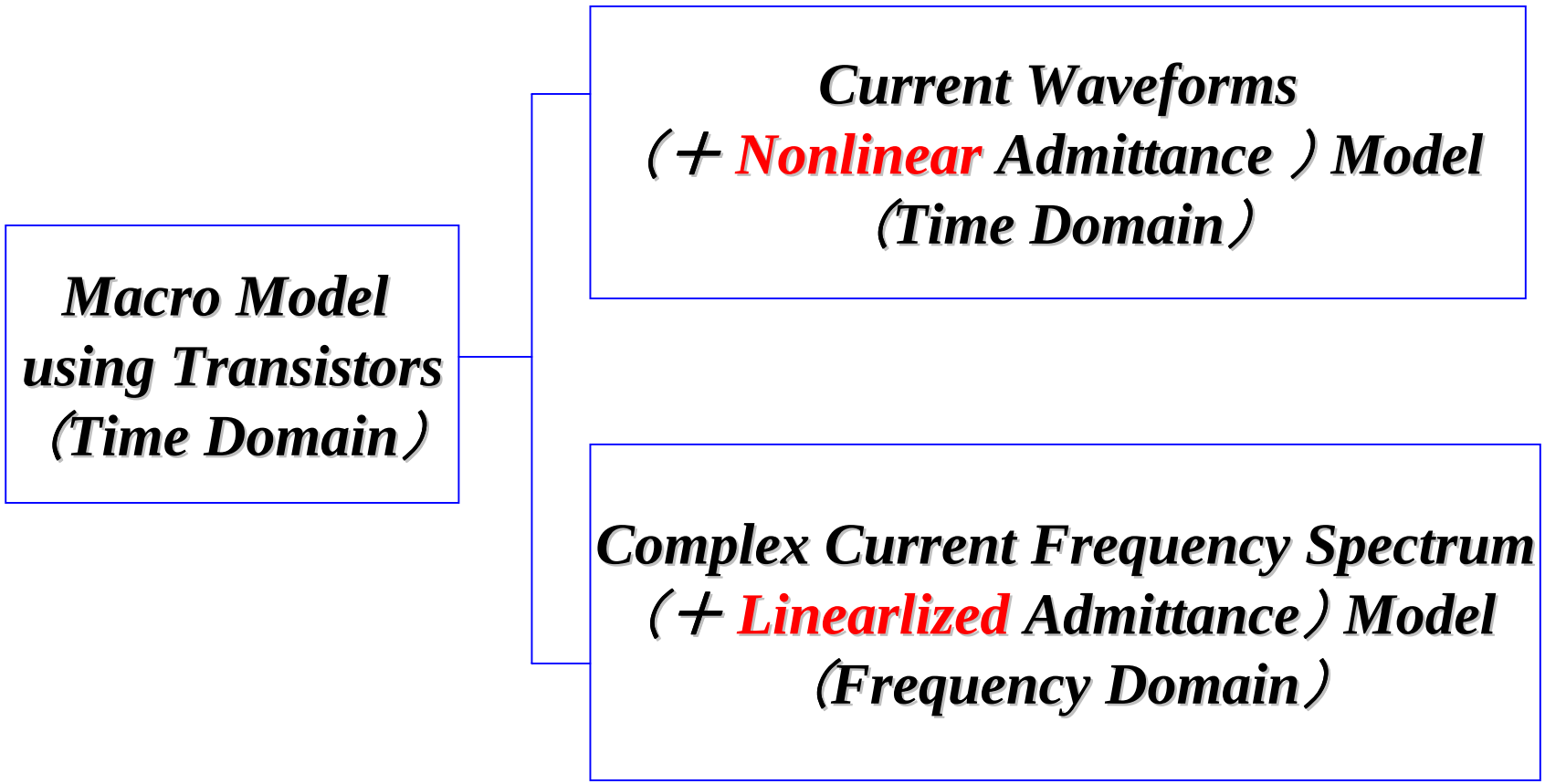
By Measurement



By CAD



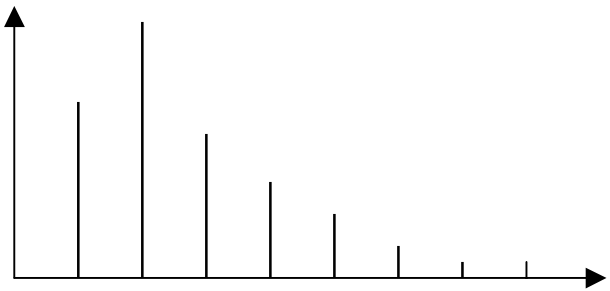
Three Types of Core Logic Model for EMI



+ Power/Ground Pattern on Chip and Package Model

EMI Simulation using Frequency Domain Model

Equivalent Circuit in Frequency Domain



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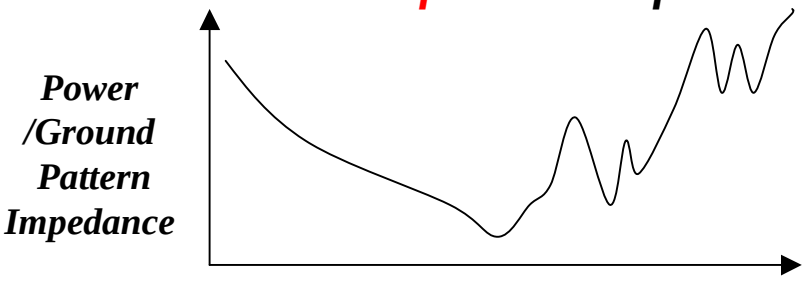
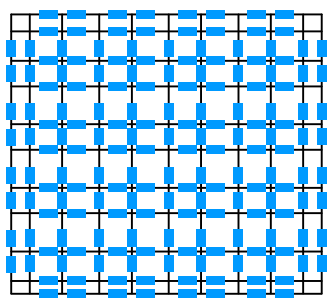
Equivalent Circuit in Frequency Domain with Location Information of PCB

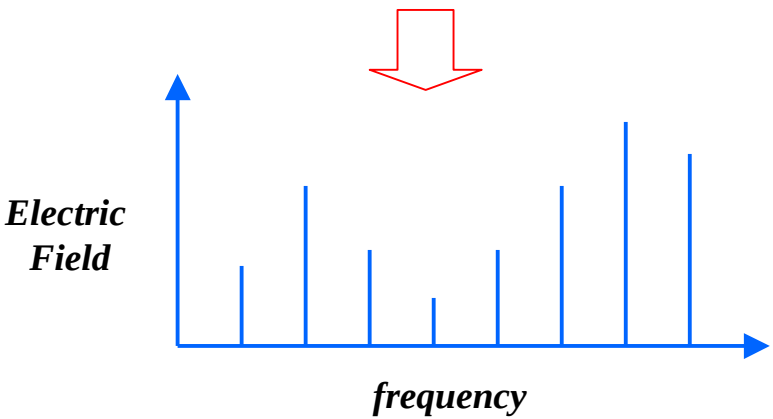


Freq	I(real)	I(imag)	
96MHz 192MHz 288MHz ⋮	40mA 80mA 30mA ⋮	-50uA 200uA -5mA ⋮	Admittance Equivalent Circuit Or Frequency Dependent Admittance

LSI Power Grid Model

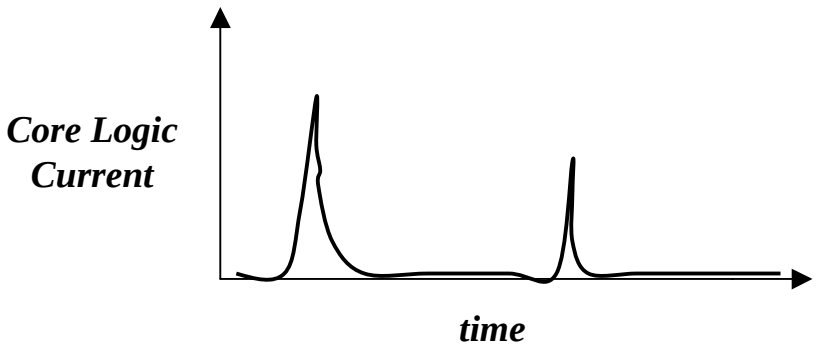


Current Distribution



EMI Simulation using Time Domain Model

Equivalent Circuit in Time Domain
(Current waveforms are not necessary:
Just switch Model between Voltage Source)



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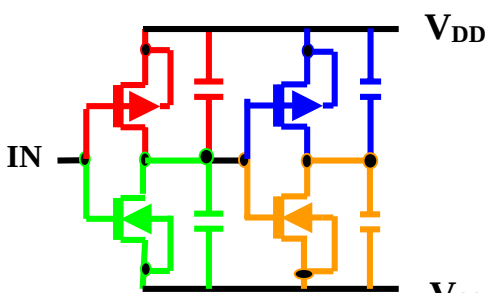
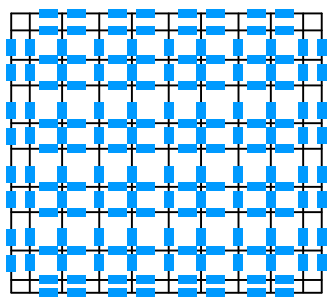
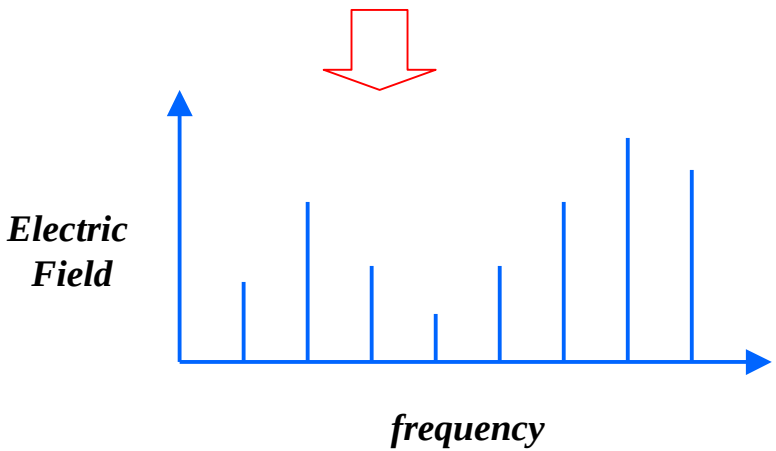
Equivalent Circuit of Power and
Ground Patterns in Time Domain
with Location Information of PCB

Current Distribution
(not current waveforms)

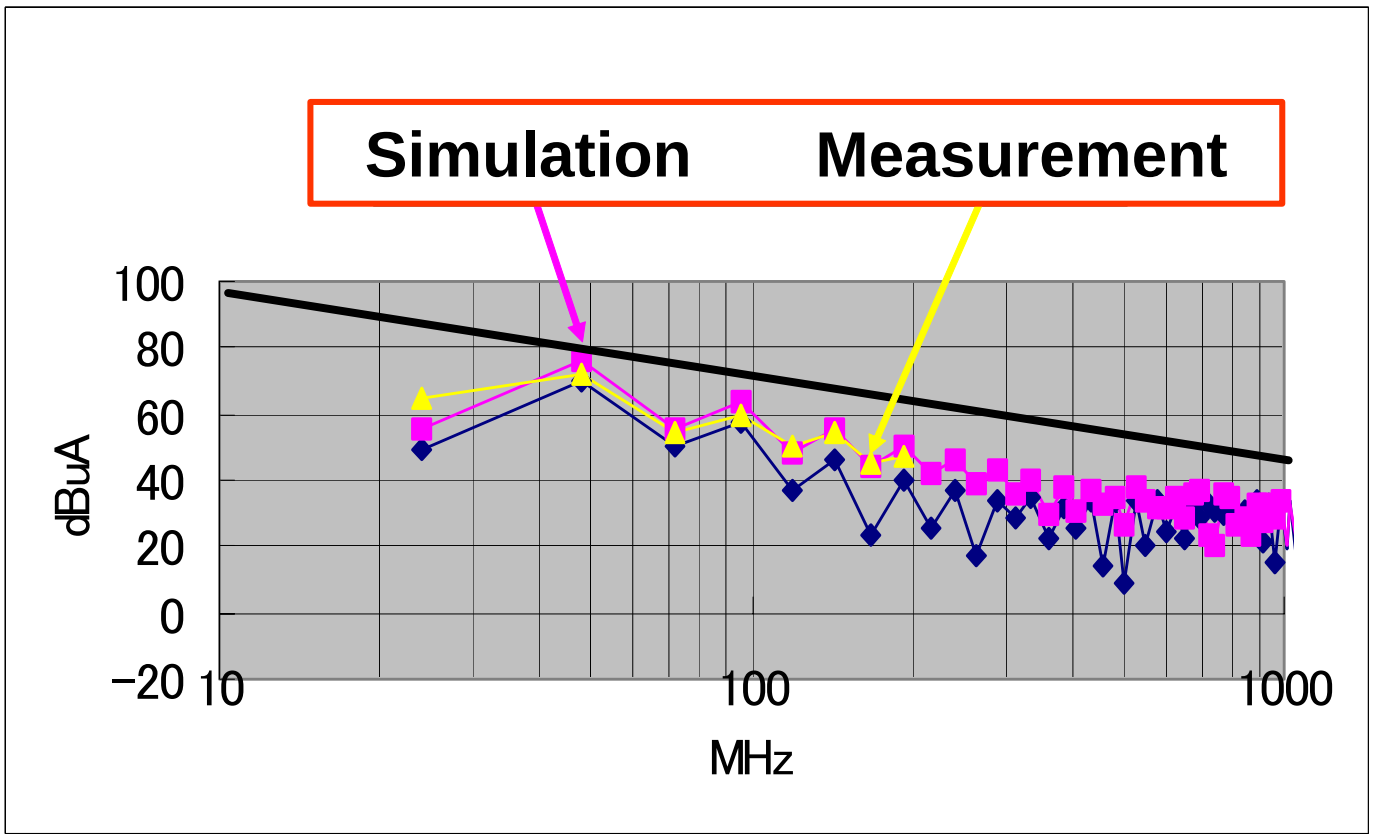




LSI Power Grid
Model

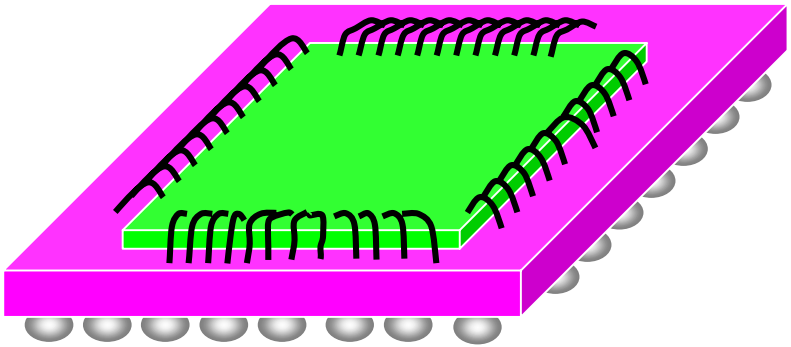


Accuracy

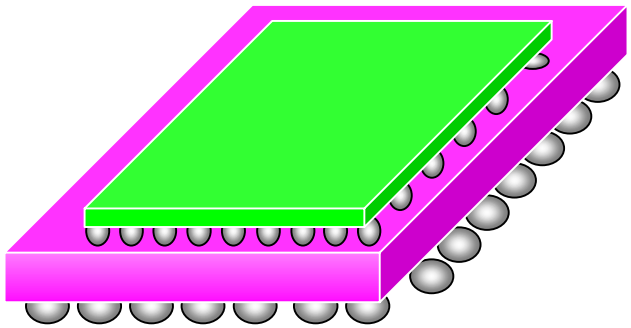


3. Modeling of High-Pin Count Package

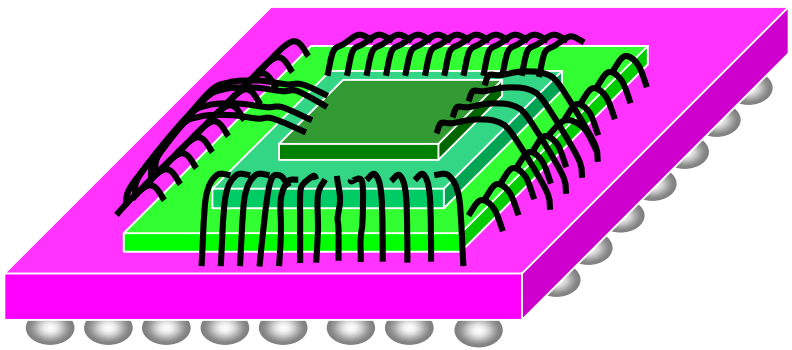
Advanced IC Packages



BGA/CSP (Bonding Wire)

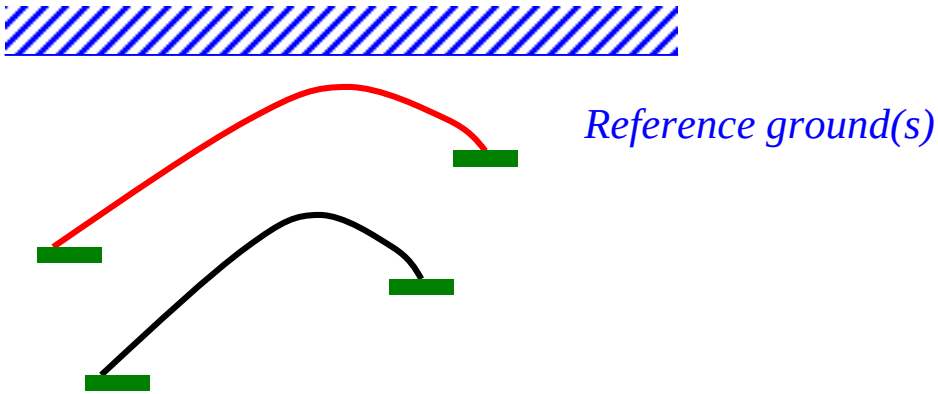


BGA/CSP (Flip Chip)



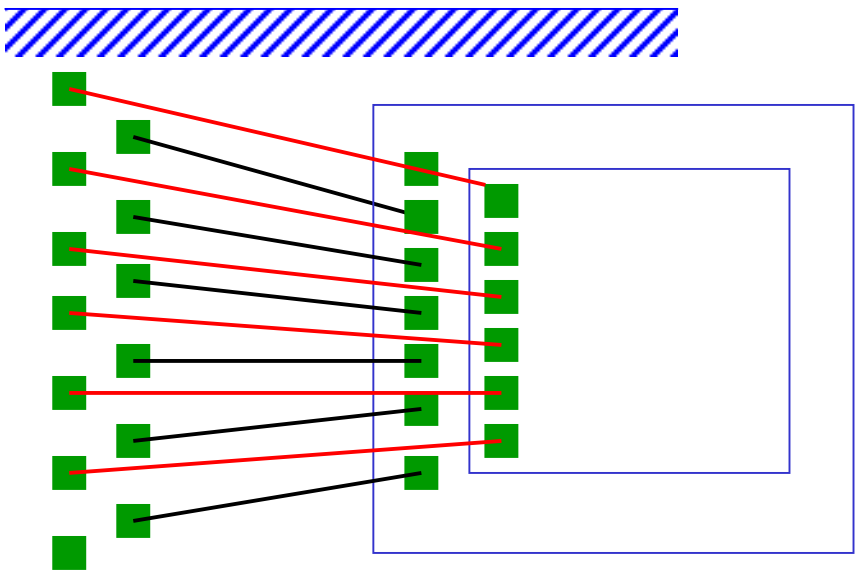
SIP

Bonding Wires and Balls



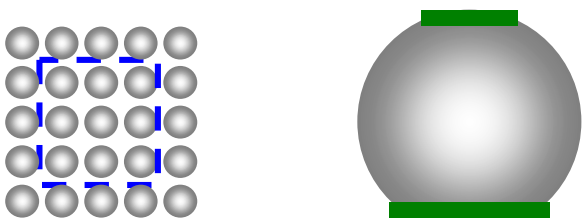
Coupling

Reference Ground



Flip Chip/Ball Pad

Pad on a chip/substrate



Pad on a substrate/PCB

A Problem in IBIS IC Package Model

No Models of Power/Ground Pins

Only lead frame type package

Too Huge Model for Arbitrary Shape Power/Ground

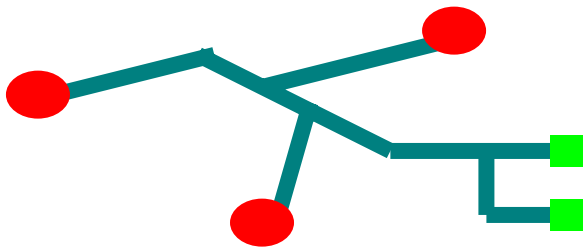
Patterns with Many Pins
Partial Models

Too complex to use for time domain analysis

Isolated Model from PCB and/or LSI chip
(Some case needs to merge CAD DB)

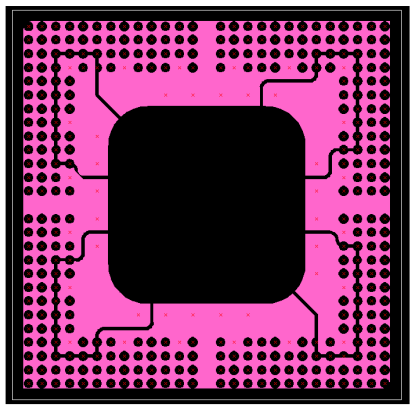
Non-Ideal Power/Ground Needs ICM/IBIS 4.1

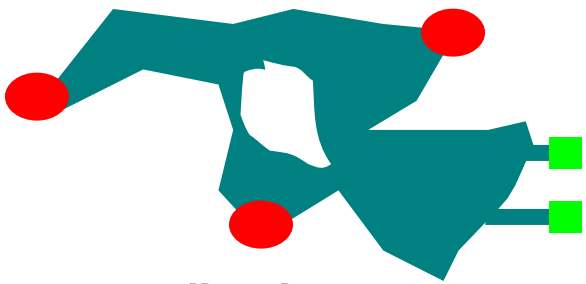
More than Two Terminals



Ball Pads

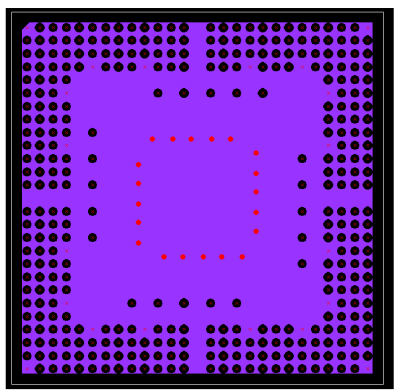
Bonding Pads



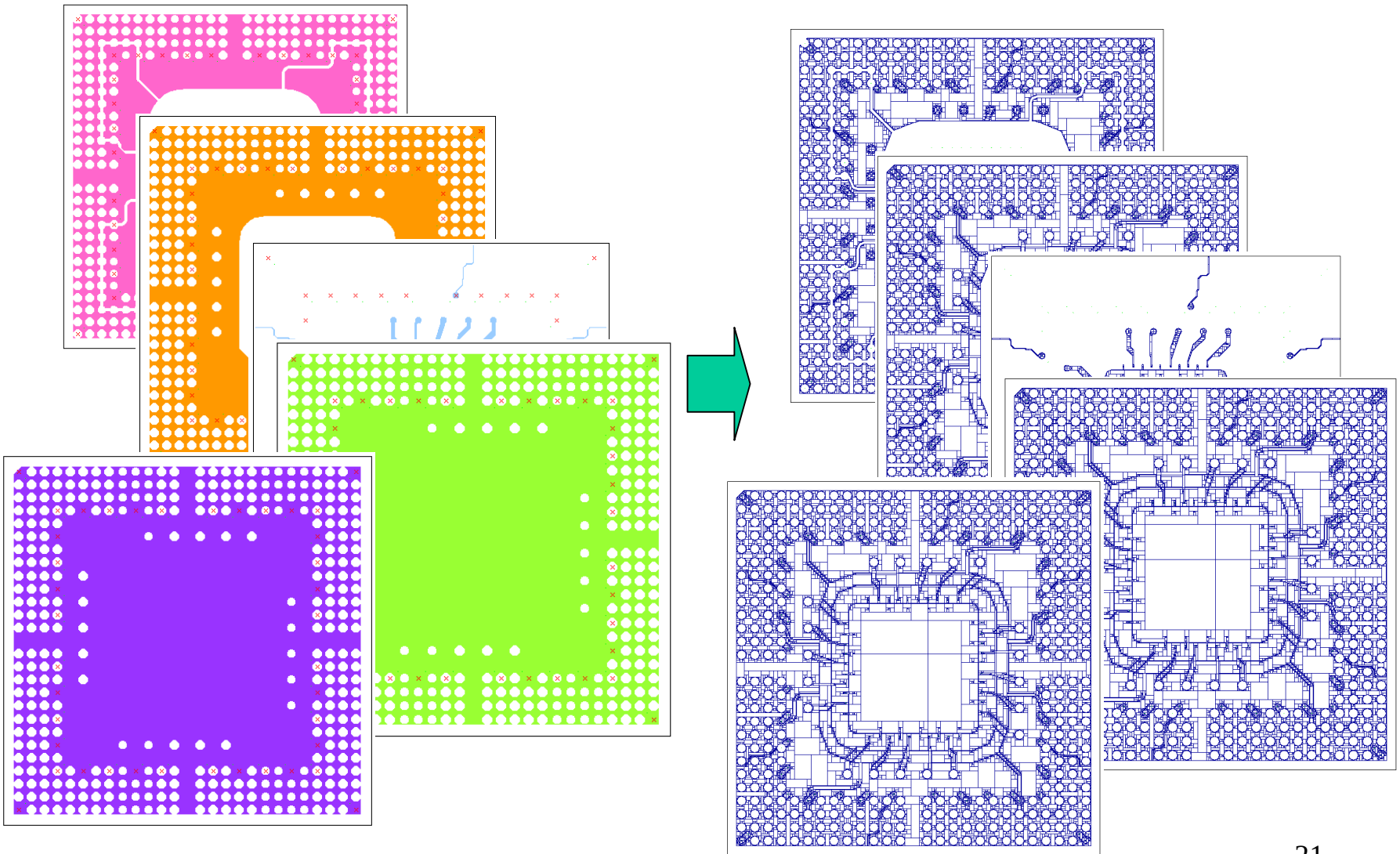


Ball Pads

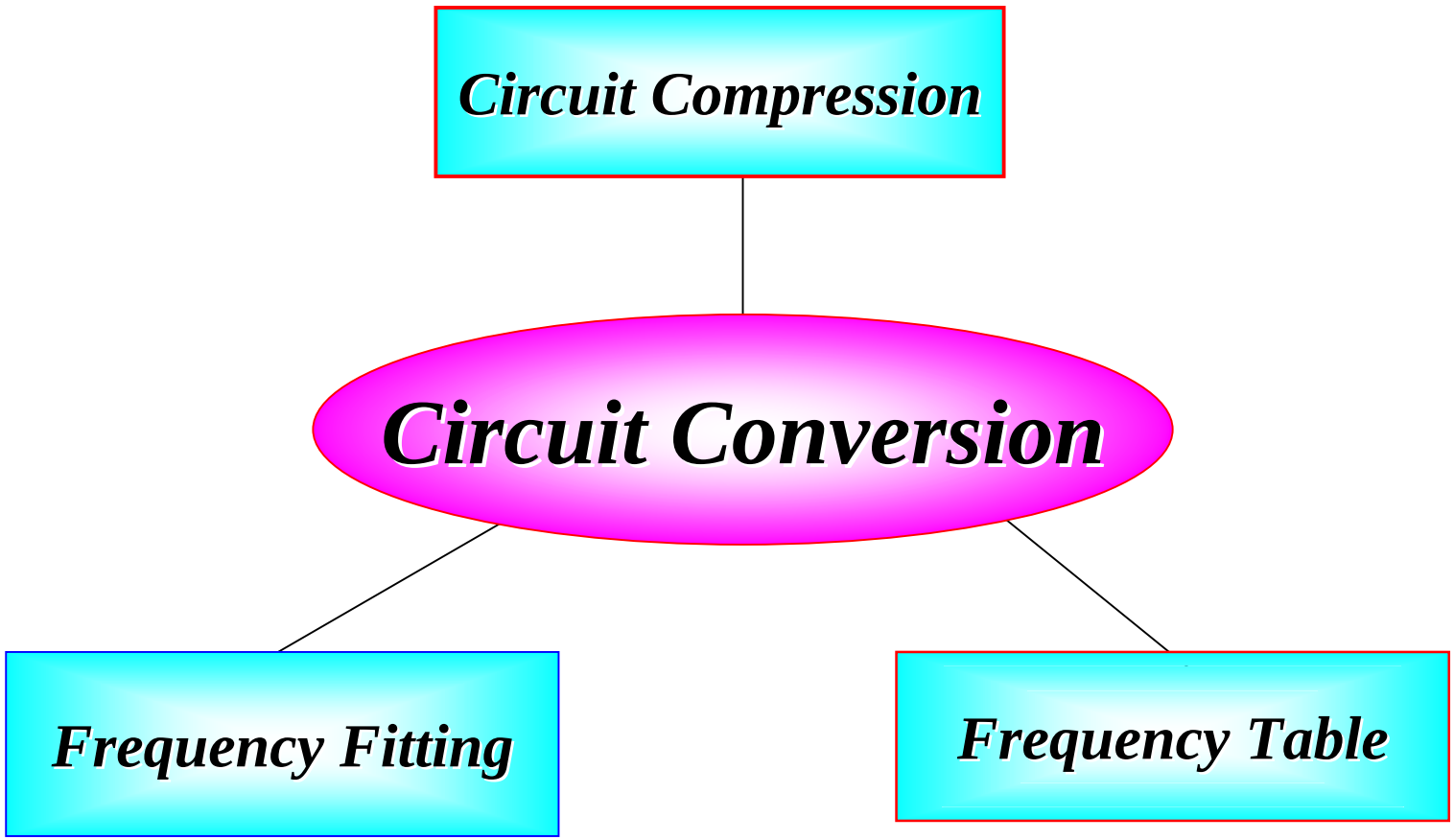
Bonding Pads



Meshing Power and Ground

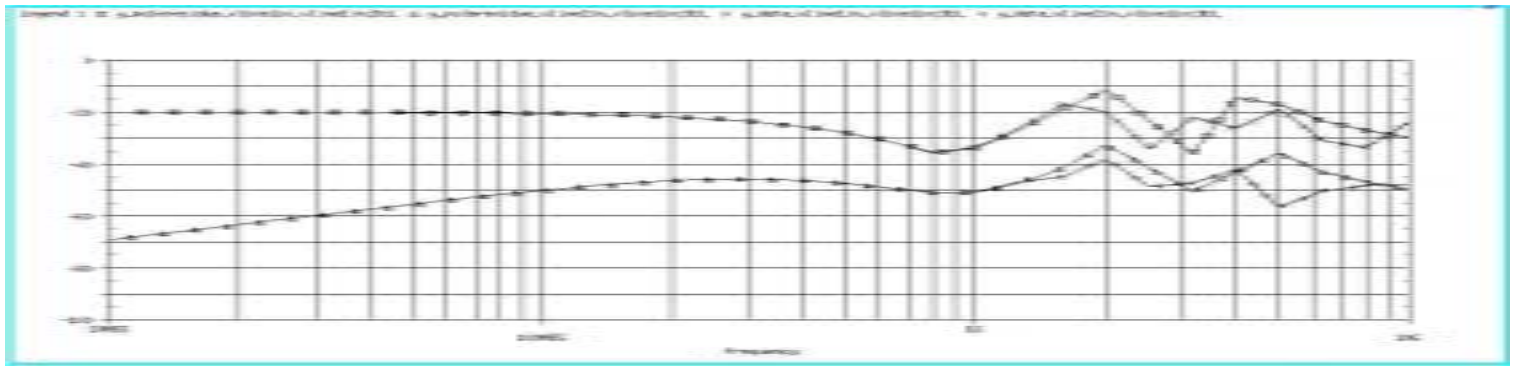


Three Types of Model Order Reduction (MOR)

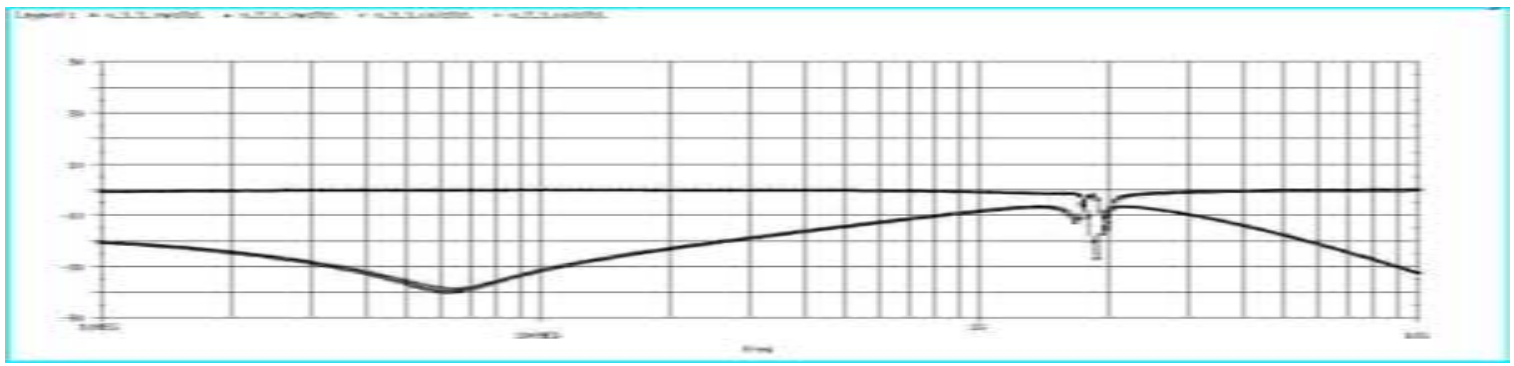


• Three Types of Model Order Reduction (MOR)

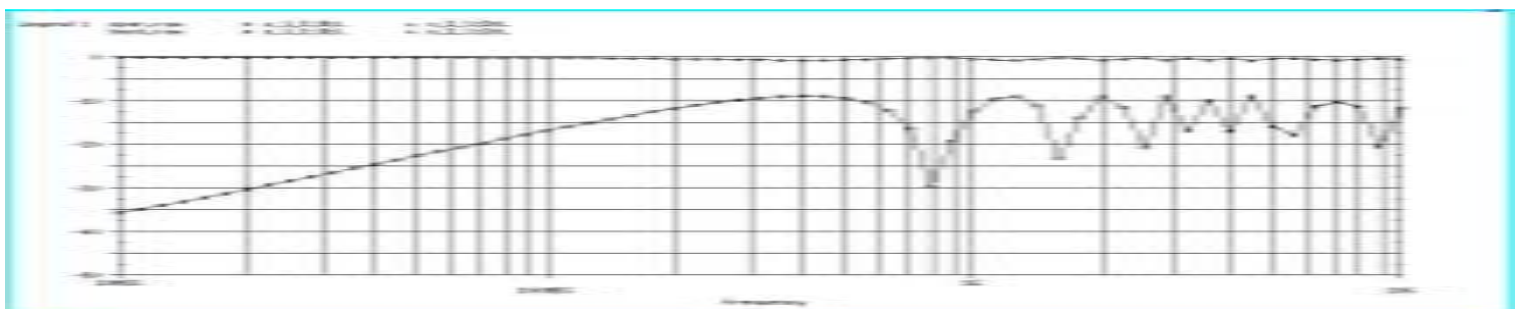
Circuit Direct Compression



Frequency Fitting



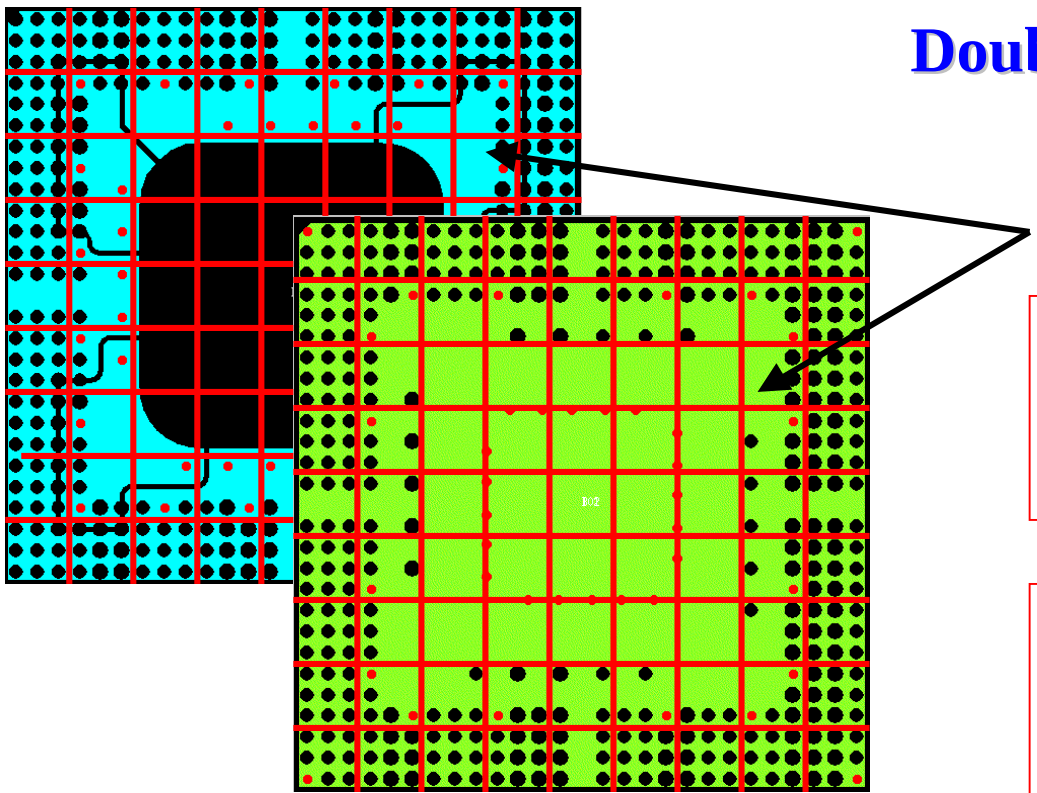
Frequency Table（SPICE IFFT）



Comparison of MOR

	Circuit Direct Compression	Frequency Fitting	Frequency Table
Input Data	Lumped Elements with no frequency dependency	N-port Parameters （by Measurement or Field Solver, Linear Elements with frequency dependency）	
Output Data	G-element, Segmented Lumped Elements	G-element (Polynomial)	G-element (Frequency Table)
Stability with Nonlinear Devices in Time Domain	Stable Fast	Unstable/Stable Fast	Unstable / Slow Stable needs huge data points
Applications	Need Circuit Data	Short Structure Few Resonance	Long Structure Many Resonance

Needs Huge Computation to Make a Macro Model for High-Pin Count Power/Ground Patterns



Double step MOR

Cell (I, J)

Each Cell model by MOR by Parallel Processing

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Whole model by MOR

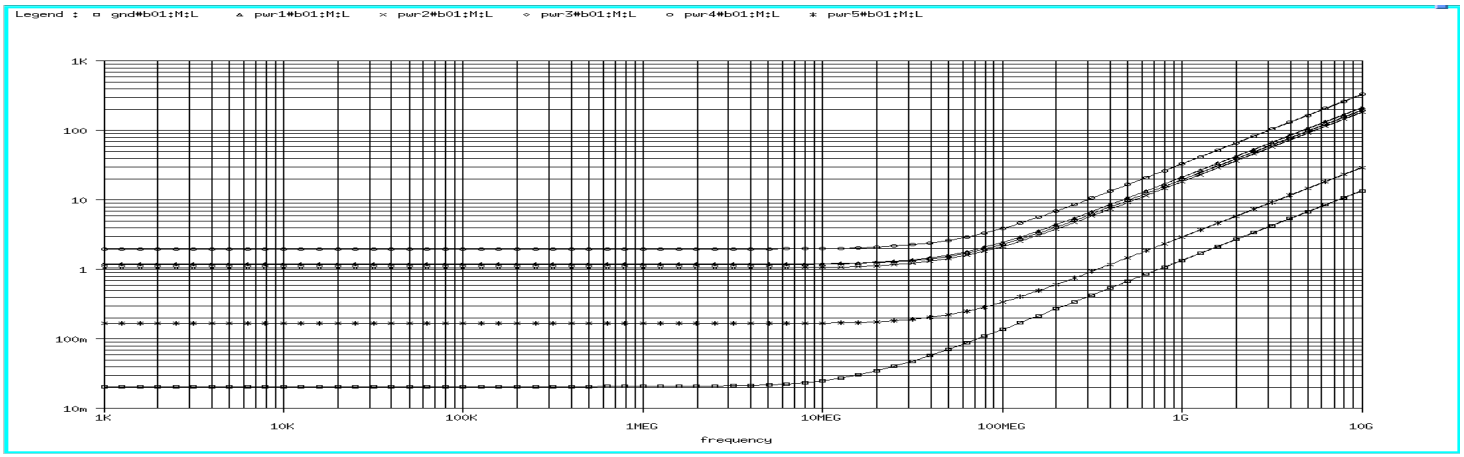
Double Step MOR

	Modeling		Model Size	Accuracy	Modeling Time	Comments
	Cell Level	Whole Level				
1	———	PEEC	*Too Large*	*highest*	*Memory Overflow*	*Too large*
2	PEEC	———	*Too Large*	*high*	*Medium*	*Too large*
3	Circuit Compression	———	*Large*	*high*	*Long*	*Hard to use*
4	Circuit Compression	Circuit Compression	*Small*	*low*	*Long*	*Inaccurate*
5	Circuit Compression	N-port Parameter Fitting	*Small*	*medium*	*Long*	*Best*

Impedance between Power and Ground

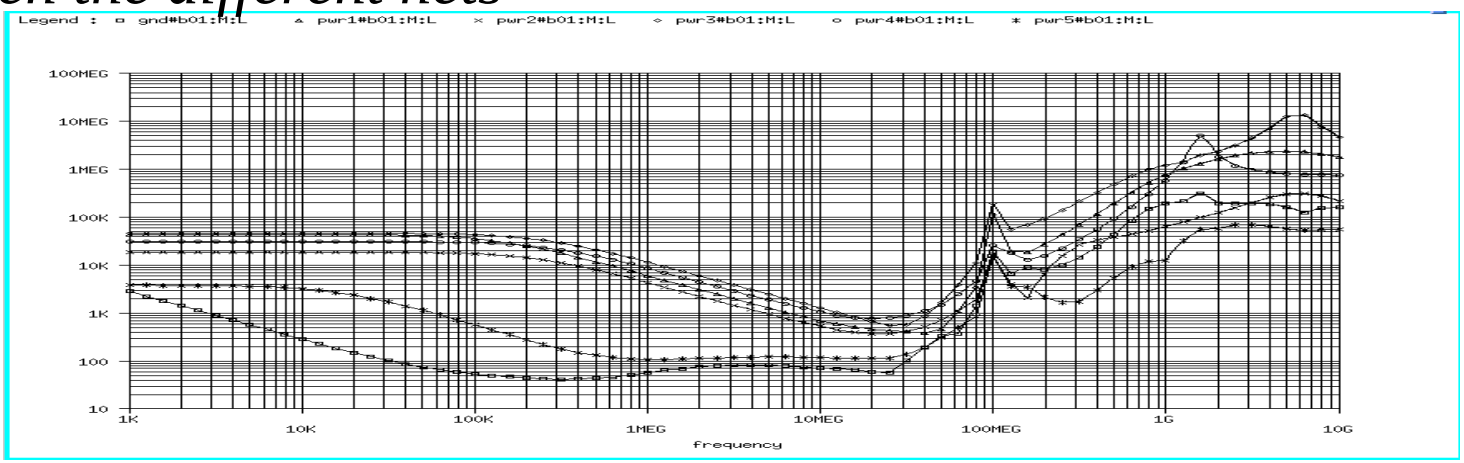
Along the same net

Impedance

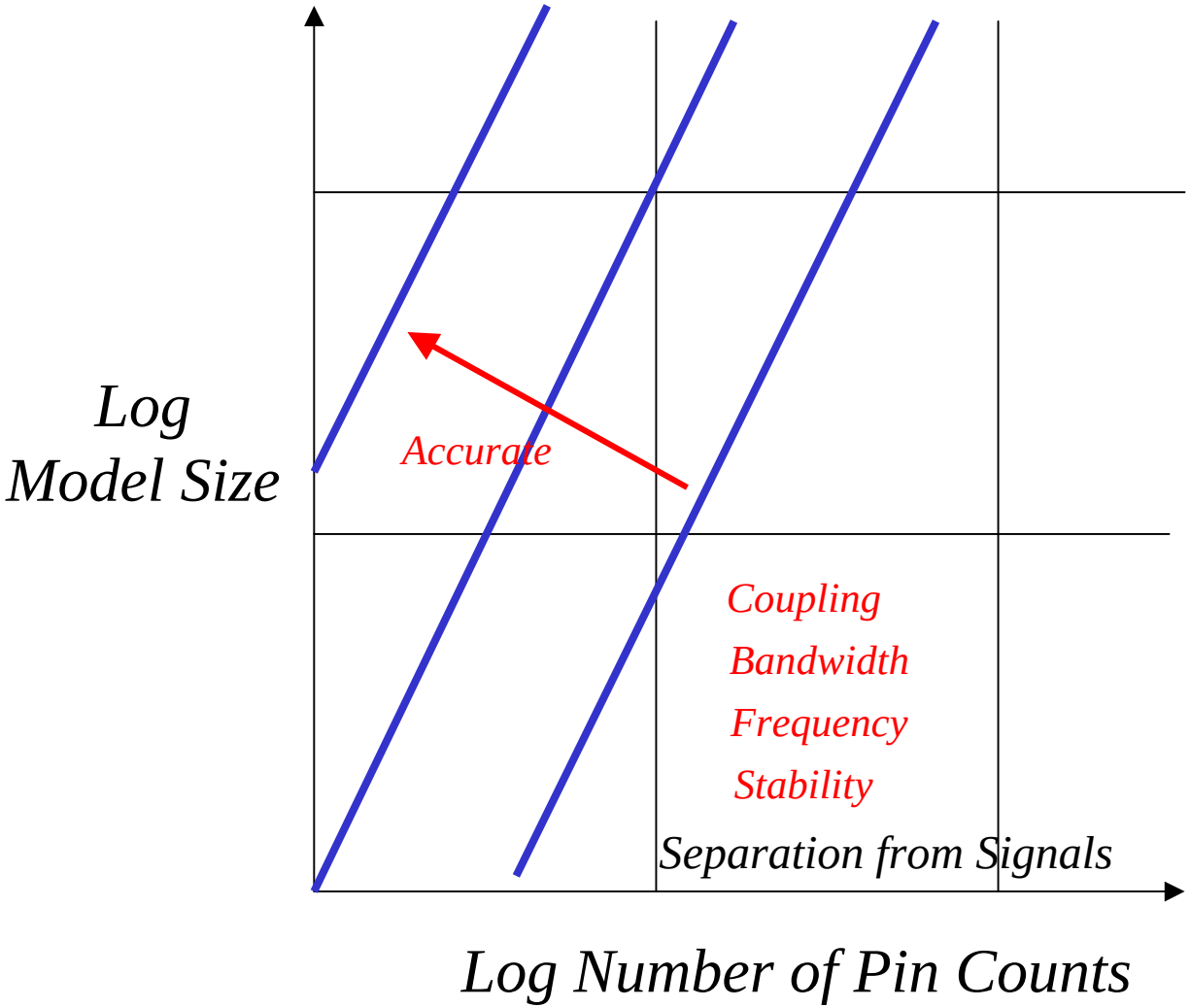


Between the different nets

Impedance



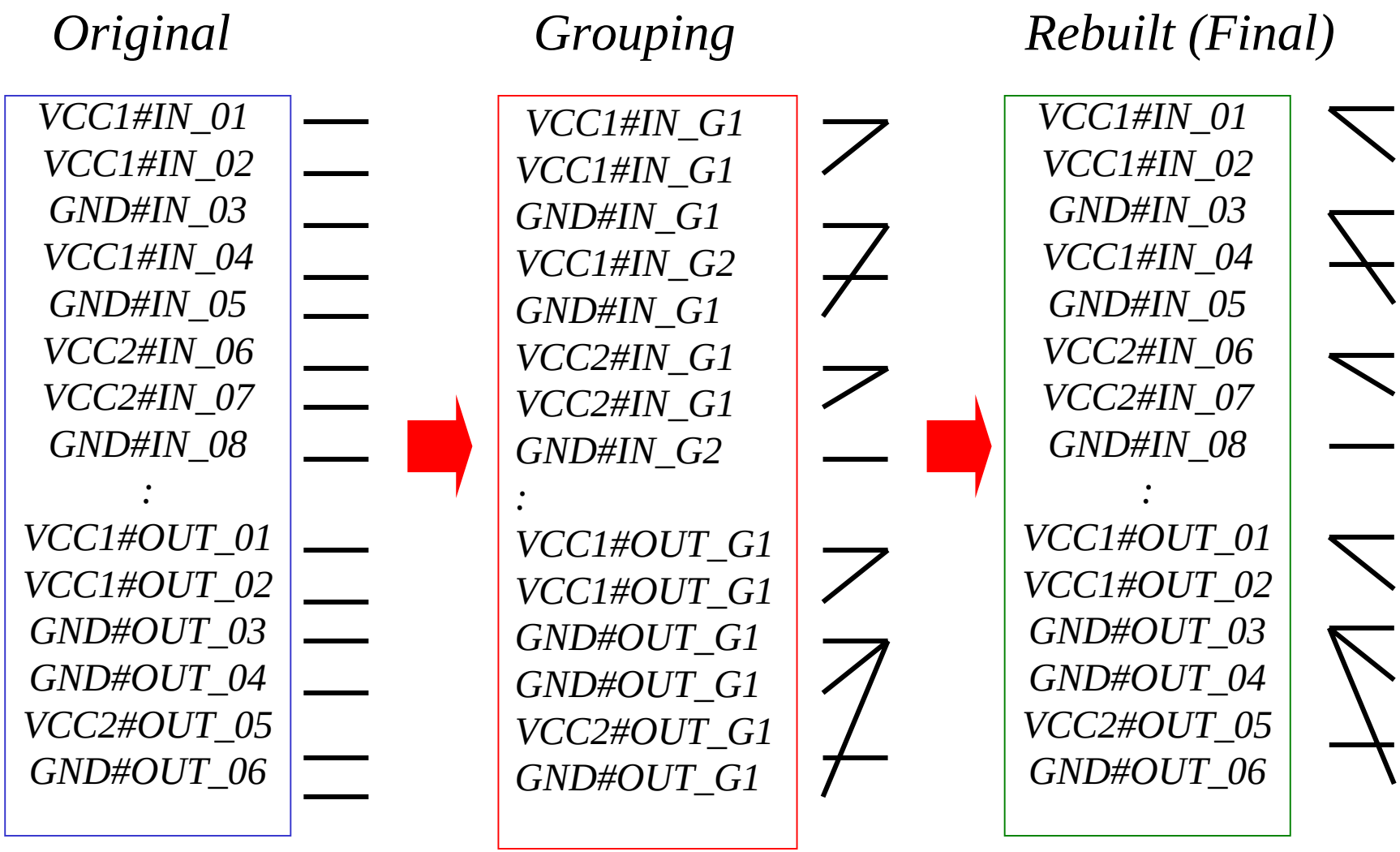
Still Needs a Smaller Model in Time Domain



Power/Ground has many pins

Individual Pin Model with coupling easily reaches MB in any format.

Grouping of closely located Pins may be needed



Choice of Formats

IBIS 4.1 / ICM 1.0 Formats

Applications

S-parameters

Time Domain

Lumped SPICE Networks

Frequency Domain

Coupled Transmission Line Networks

4. Conclusion

Simple is best / Well-balanced Model

Different Models for SSO/Bounce/EMI