

High Accuracy Behavioral Modeling for Frequency and Time Domain Simulations

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Outline



Part I – Problem statement

- Why frequency domain analysis?
- Resonant circuit example

Part II – Frequency response of an IBIS model

- The impedance of an IBIS model
- Facts and problem statement

Part III – New modeling proposal

- Some theory and complex algebra
- Transfer functions and Laplace elements
- HSPICE examples
- Introducing the FD/TD behavioral model
- More HSPICE examples
- Conclusion







Part I

Introduction



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Why frequency domain analysis?



Some times it is easy to tell that there is a signal quality problem by looking at the waveforms (in time domain), but often it is very easy to miss problems or it may take too long to find them.

We need a methodology that can reliably and quickly tell us whether there is a problem and what it is.

- The waveforms of time domain simulations may change when we run the simulation at different frequencies even if we don't change anything in the circuit (due to reflections and resonance)
 - this frequency dependency can be studied much easier with frequency domain analysis to uncover problems
 - FD simulations run much faster than TD simulations, so more work can be done in less time

Once we are done optimizing for signal quality in the frequency domain we still need to run simulations in the time domain to find best/worst timings for the design.





The bottom line is time



The timing of our designs is determined by the shape of the waveforms.

The shape of the waveforms, however, are very strongly effected by the resonance effects.

Eliminating resonance results in more precise, stable and predictable timings. So our goal is to find and remove resonances.

In order to be able to do that we need buffer models which are accurate at all frequencies.





What makes these waveforms so unpredictable?



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Waveforms without resonance are predictable

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The circuit of the previous two sets of waveforms



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Part II

Frequency response of an IBIS model



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Looking into an IBIS buffer - Z₁₁





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Frequency response at 0.1 V DC bias

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Frequency response at 2.0 V DC bias

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Facts and problem statement



- Voltage dependent impedance (Z₁₁ vs. bias)
 - this is the steady state DC behavior
 - IBIS uses IV curves to describe this
 - good match (at very low frequencies)

• Frequency dependent impedance

- we use C_comp to describe (part of) it
- C_comp matches a single parallel RC circuit well
- series-parallel RC combinations not accurate
- cannot model voltage (bias) dependency
- Time dependent impedance
 - this is the transient (switching) behavior
 - IBIS uses Vt curves to describe this
 - need to find a method to analyze AC response during transients







Part III

New modeling proposal



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Some theory







(ior a parallel KC circuit



To express this as a function of voltage, we can write $Z(V) = R(V) \parallel 1/j\omega C(V)$ $Y(V) = G(V) + j\omega C(V)$



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Transfer functions and the Laplace element

The Y₁₁ transfer function of a resistor:

 $\mathbf{H(s)}=1/\mathbf{R}$

The Y₁₁ transfer function of a capacitor:

H(s) = sC

The Y₁₁ transfer function of a parallel RC circuit:

$$H(s) = \frac{1}{R} + sC = \frac{1 + sCR}{R}$$

In HSPICE this can be modeled with a Laplace element the following way:





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An undocumented(?) HSPICE feature

The same transfer function can also be expressed with parameters who's value depends on another variable. The Y₁₁ transfer function of the parallel RC circuit as a function of voltage is:

$$H(s, V) = \frac{1}{R(V)} + sC(V) = \frac{1 + sC(V)R(V)}{R(V)}$$

(This works in HSPICE up to a few dependent terms).

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Proving that it works







Revisiting complex algebra

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$$Z_{\text{measured}} - Z_{\text{DC}} = Z_{\text{AC}}$$

Since Z_{DC} (IV curve) is a real number, it does not have an imaginary part, and $Im(Z_{AC}) = Im(Z_{measured}).$

Also, because Z_{DC} is a frequency independent number (i.e. constant), $Re(Z_{AC}) = Re(Z_{measured}) - k$ (which is a simple shift)





Medium complexity example with Mathcad



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Real and Imaginary part plots from Mathcad







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HSPICE netlist segment for Mathcad example



```
.param Bias= 0.0
.param C1 = 1.0pF
.param C2 = 9.0pF
.param R1 = 10
.param R2 = 90
*
.param n0 = 0
.param n1 = 'C1*pow(R1,2)+C2*pow(R2,2)'
.param n2 = 'C1*pow(R1,2)*C2*R2+C1*R1*C2*pow(R2,2)'
.param d0 = 'pow(R1,2) + 2*R1*R2 + pow(R2,2)'
.param d1 = 'pow(R1,2)*C2*R2+R1*C2*pow(R2,2)+C1*pow(R1,2)*R2+C1*R1*pow(R2,2)'
.param d2 = 1e-21
                           $ 1e-21 to keep HSPICE happy
Vac1 RC1
        0
            AC= 1 DC= Bias
*
        RC1a R= R1
R1a
   RC1
       RC1a C= C1
C1a
   RC1
R1b
   RC1a
           R= R2
        0
C1b
   RC1a
        0
            C = C2
Vac2 RC2
           AC= 1 DC= Bias
        0
   RC2
G2a
        0 CUR = 'V(RC2)/100'
                        $ Parallel R
*-----
                                 G2b
   RC2
        0
           LAPLACE RC2 0
*
                         $ Two || RCs in series minus DC
+ n0 n1 n2 / d0 d1 d2
*******
                   . END
```





Frequency domain response with HSPICE

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Time domain response with HSPICE (.IC = 5 V)







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HSPICE netlist segment of real buffer model

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	******	* * * * * * * * * * * * *	******	* * * * * * * * * * *	*****	****
	Vac2	RC2	0	AC=Vac	DC= Bias	
	X2a	RC2	0	FET_IV		
	* G2b	0	RC2	LAPLACE	RC2 0	
		156E-02 \\	1(02		1(62 0	
		192E-02*V(RC2				
		658E-04*pow(V		\ \		
		509E-03*pow(V				
		795E-06*pow(V				
		981E-05*pow(V		~ ~		
		576E-12 \\	(,,,			
		567E-11*V(RC2) \\			
		304E-11*pow(V		\ \		
		631E-11*pow(V				
		243E-12*pow(V				
		699E-13*pow(V				
		814E-22 \\				
	-8.1	507E-22*V(RC2) \\			
	+6.4	066E-22*pow(V	(RC2),2) [\]	11		
	-2.6	783E-22*pow(V	(RC2),3) [\]	11		
	+5.5	096E-23*pow(V	(RC2),4) [\]	11		
	-4.3	215E-24*pow(V	(RC2),5)'	/		
	+ 1					
	+ '+1.5	954E-10 \\				
	+6.5	574E-10*V(RC2) \\			
		825E-10*pow(V				
		850E-10*pow(V				
		452E-11*pow(V		\ \		
		923E-12*pow(V	(RC2),5)'			
		650E-23 \\				
		570E-22*V(RC2				
		402E-22*pow(V				
		774E-22*pow(V				
		593E-23*pow(V		\ \		
		119E-24*pow(V				
	******	* * * * * * * * * * * * * * *	******	* * * * * * * * * * *	* * * * * * * * * * * * * * * * * *	
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Frequency response of a real buffer with HSPICE

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dV/dI and dR/dV



R1 = V1 / I1 R2 = V2 / I2but $\frac{V2 - V1}{I2 - I1} \neq R2 - R1$ or $\frac{dV}{dI} \neq \frac{dR}{dV}$

In .AC analysis SPICE uses the slope of the IV curves for transistors, diodes and PWL sources. However, an IV curve implemented as a voltage controlled resistor (VCR) will produce delta R in a .AC sweep.

For this reason we need to use PWL sources to implement IV curves (in SPICE) for behavioral models.





AC sweep of FET, I-V and R-V models



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Issues / work in progress

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- TRAN mode simulations of real buffer is still in progress

• Numerical issues make it difficult to achieve a working model

- the accuracy of these experiments was limited by the order of curve fitting function (due to the available space in the HSPICE Laplace element)
- not may tools can curve fit to a complex number data table
 - HSPICE optimization doesn't converge well
- second curve fitting for voltage dependency
 - could be more accurate if done in a single process as a multi dimensional problem
- H(s) and table format for Laplace element did not converge in .TRAN yet for a real buffer behavioral model
 - could be due to numerical stability issues (denominator must be higher order than numerator), or the range of exponents is too wide for HSPICE
 - rearranging transfer function to have higher order denominator may get this to work
- could try pole-zero format
- these problems may not be an issue if a tool was designed to do this

• Transient behavior of AC components need to be studied more

- extending the concept to multi dimensional transfer functions (time variant, voltage dependent) could account for transients
- could possibly use the V-t curves or similar information to control transient behavior of the AC components of the model, but more research is needed to understand this

Conclusions



- We need to consider only one additional element for the IBIS-X specification to achieve a highly accurate FD/TD behavioral model
 - this element would replace the existing C_comp parameter
 - this element needs to interpret some sort of a transfer function
 - various formats could be supported, table driven, transfer function (equation) driven, or pole-zero driven
 - various types of data could be supported, Z, Y, S-parameters, and/or voltage and current (each of which is complex)
- Complex number capability is needed to make this work
- The concept shown here using a one-port circuit can be extended to a special multi terminal port representing all nodes of the buffer
 - need at least two terminals for the power and ground rails
 - need one or two terminals for single ended or differential buffers
 - the complex impedance as a function of output and supply voltage, time, temperature, process, etc. between each of these terminals can be described according to the concept shown here

