Driver Schedule Modeling

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- Driver Schedule Enhancement and Reduction Setups
- Possible Improvement for Over-clocked mode where start of next transition if before the finish of previous transition
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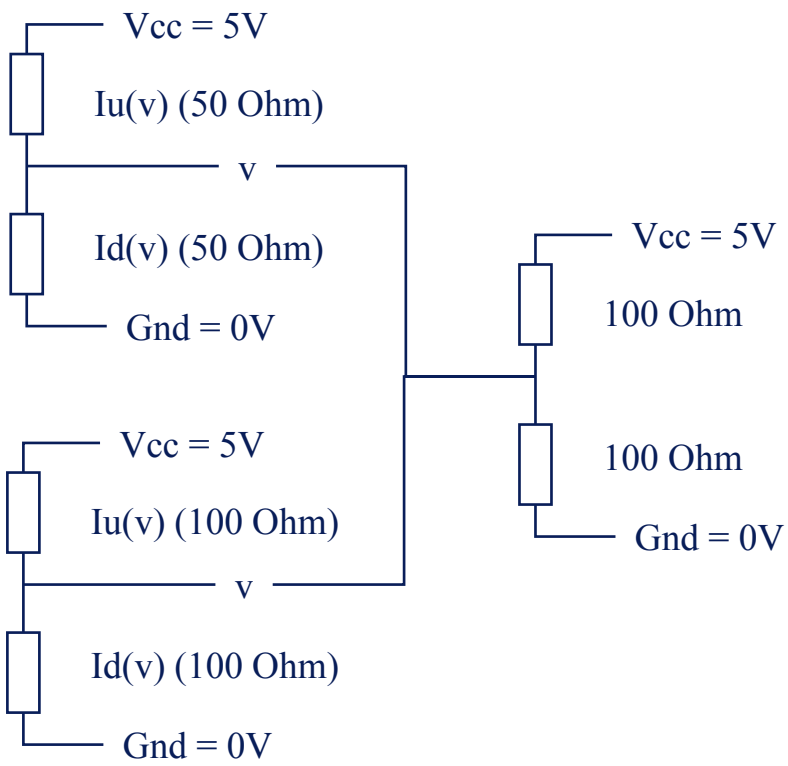
- Illustration of Driver Schedule for Discrete Waveform Shaping

Driver Schedule Examples (D6 is not legal - ambiguous)

Name	Rise-on	Rise-off	Fall-on	Fall-off
D1	0	na	0	na
D2	na	0	na	0
D3	0	5ns	na	na
D4	5ns	0	na	na
D5	na	na	3ns	5ns
D6	0	5ns	0	5ns

Driver Schedule Test Circuit (Produces 1, 2, 3, 4 V outputs)



Name	*50-Ohm*	*100-Ohm*	*V*
Ls	Low	Low	1
Lw	Low	High	2
Hw	High	Low	3
Hs	High	High	4

Valid Setup Examples for Enhancement and Reduction

Driver	*Rise-on*	*Rise-off*	*Fall-on*	*Fall-off*
D_50	0ns	na	0ns	na
D_100	1ns	na	1ns	na

Driver	*Rise-on*	*Rise-off*	*Fall-on*	*Fall-off*
D_50	0ns	na	0ns	na
D_100	na	1ns	na	1ns

Driver	*Rise-on*	*Rise-off*	*Fall-on*	*Fall-off*
D_50	0ns	na	0ns	na
D_100	1ns	4ns	na	na

Driver	*Rise-on*	*Rise-off*	*Fall-on*	*Fall-off*
D_50	0ns	na	0ns	na
D_100	4ns	1ns	na	na

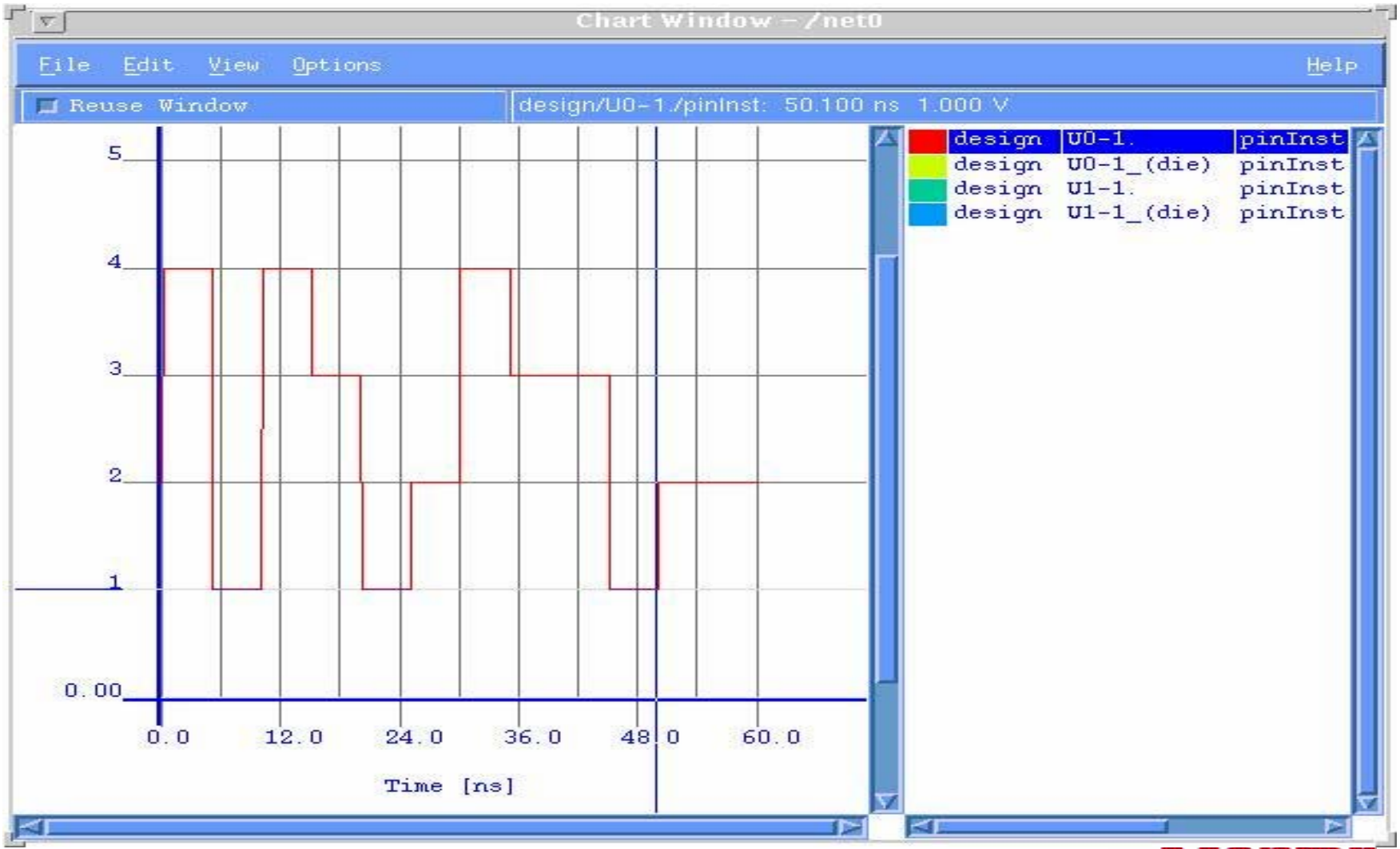
SCSI Driver Example Using Reduced Strength Driver

Driver	*Rise-on*	*Rise-off*	*Fall-on*	*Fall-off*
D_50	0ns	na	0ns	na
D_100	na	5ns	na	5ns

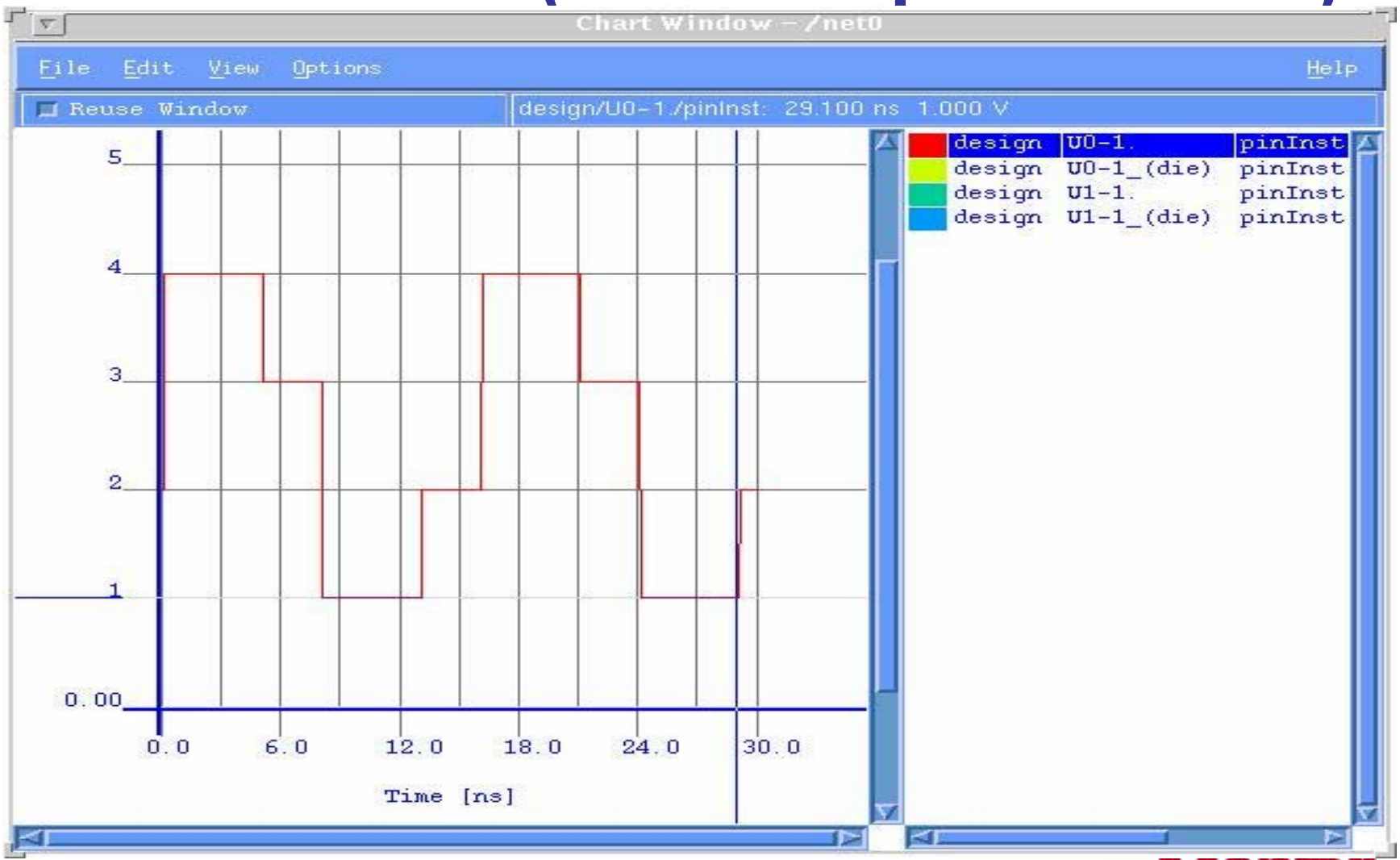
Driver	*Rise-on*	*Rise-off*	*Fall-on*	*Fall-off*
D_50	0	na	0ns	na
D_100	0	5ns	0	5ns

- **Two versions of the SCSI Driver**
  - **Version 1 is legal IBIS - next page**
  - **Version 2 is not legal, but responds more cleanly to over-clocking. However the pulse widths are not made narrower and are wrong - page after next.**

Valid Second Bit Reduction



2-bits = 8 nS (but 5 nS pulse width)

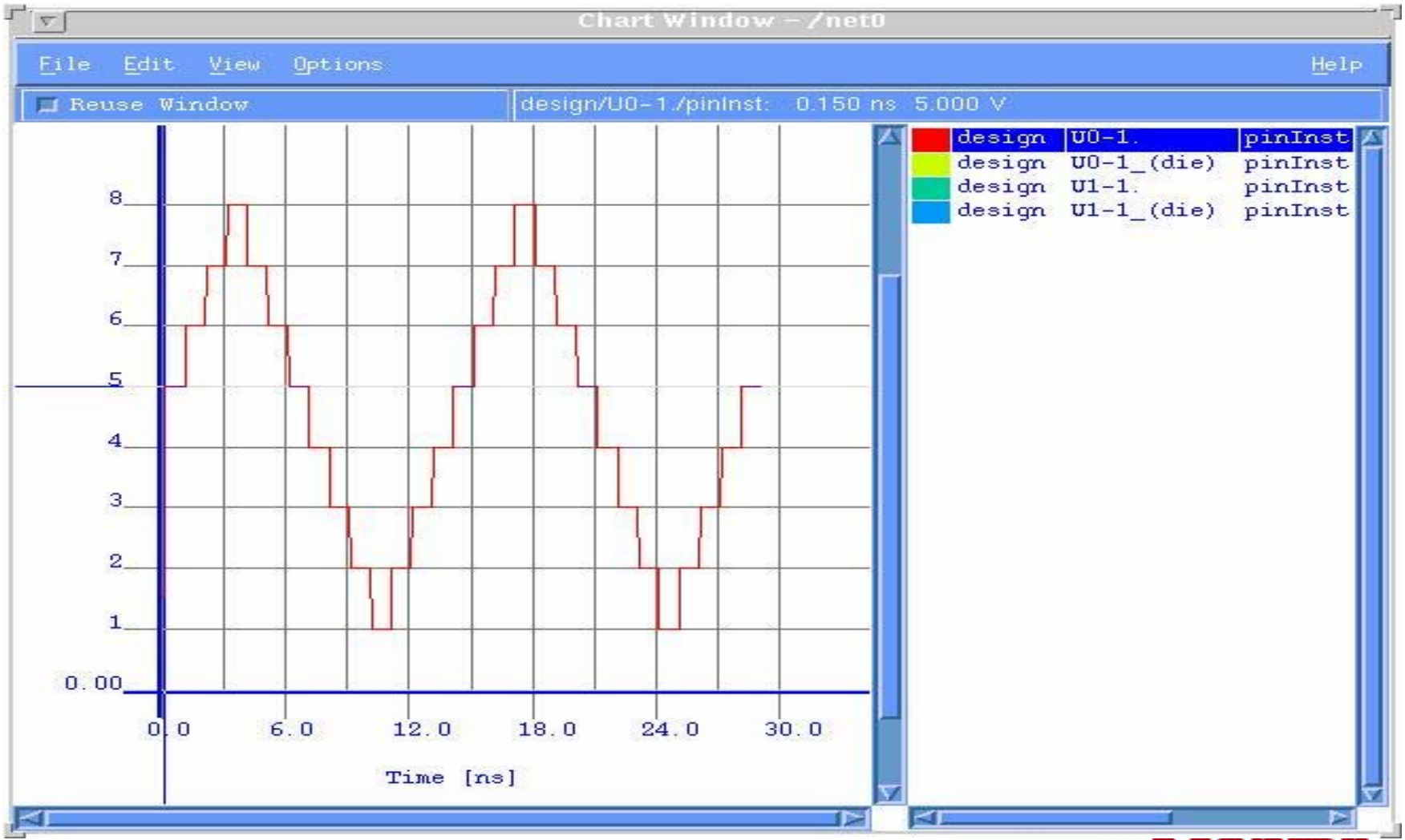


Stair Step Waveform Showing Enhancement and Reduction

- Drivers (9 V)
  - U0 - 25 Ohm - Output
  - U1 - 50 Ohm - Open_drain and Open_source
  - U2 - 100 Ohm - Open_drain and Open_source
  - Open_* used because of several transitions in “Rise_*” and “Fall_*” pulse
- Terminator - 100 Ohm 9V, 100 Ohm Gnd
- 1 V to 8 V in 1 V Steps

```
|*****************************************************************************
|                          typ               min               max
[Voltage range]           9V                NA                NA
|
|*****************************************************************************
|
[Driver Schedule]
|  Model             Rise_on   Rise_off Fall_on  Fall_off
U0                   0         7n       NA       NA

U1_UP                2n        5n       NA       NA
U1_DOWN              2n        0n       NA       NA
U1_DOWN              7n        5n       NA       NA

U1_UP                NA        NA       2n       0n
U1_UP                NA        NA       7n       5n
U1_DOWN              NA        NA       2n       5n

U2_UP                1n        2n       NA       NA
U2_UP                3n        4n       NA       NA
U2_UP                5n        6n       NA       NA
U2_DOWN              1n        0n       NA       NA
U2_DOWN              3n        2n       NA       NA
U2_DOWN              5n        4n       NA       NA
U2_DOWN              7n        6n       NA       NA

U2_UP                NA        NA       1n       0n
U2_UP                NA        NA       3n       2n
U2_UP                NA        NA       5n       4n
U2_UP                NA        NA       7n       6n
U2_DOWN              NA        NA       1n       2n
U2_DOWN              NA        NA       3n       4n
U2_DOWN              NA        NA       5n       6n
```

Pulse Width 7 nS, Period 14 nS



Driver Schedule Observations

- Existing Driver Schedule can be used for second bit reduction for SCSI applications for a given clock rate.
- Allowing another Driver Schedule mode produces some improvement, but produces other distortions. This improvement is not recommended.
- Driver Schedules with Open_* modes can be used for discrete pulse shaping.