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# Buffer Impedance and Quality Issues


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# Summary

- Recall of results from previous presentation
- Modeling a 5-Volt CMOS buffer
- Time behaviour : 2 examples
- Frequency signature of other buffers
- What would be added in the IBIS specification
- Frequency domain analysis: a tool to enhance the quality of IBIS models
- Conclusions

# Recall: the IBIS model impedance

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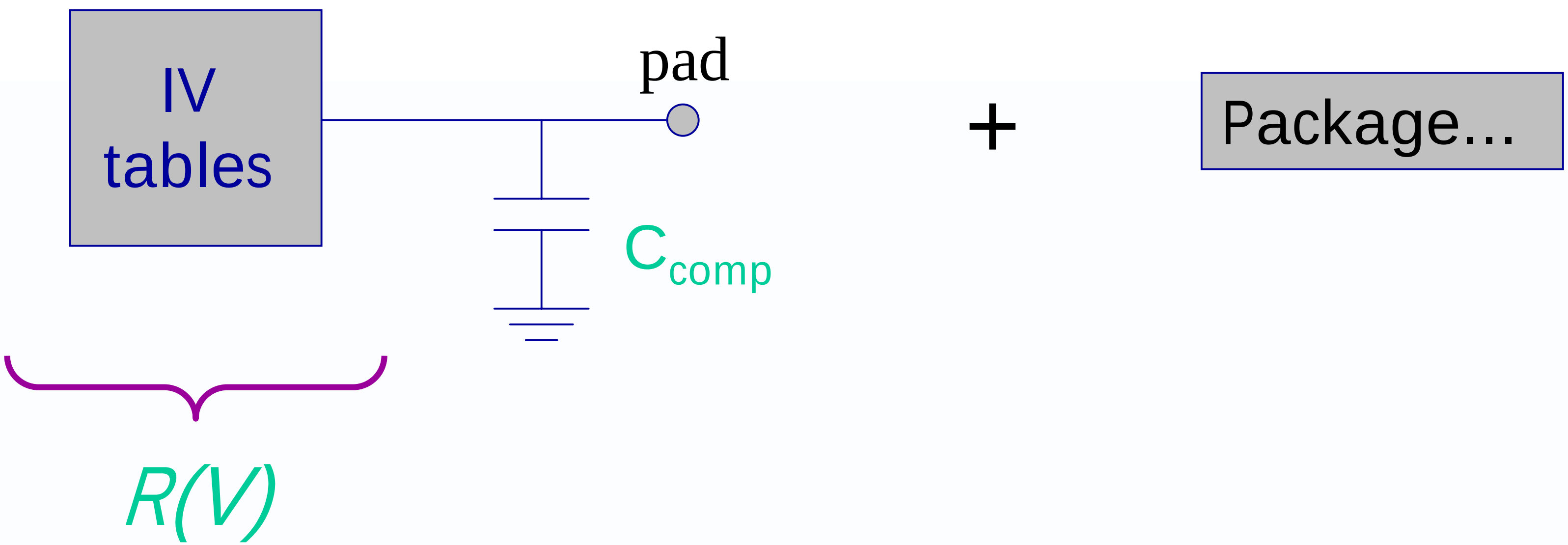


*i.e.* ⇒ $Z_{buffer,pad}$ is a shunt RC circuit, with « *R* » accounting for the whole non-linearity

NB: the resistance R(V) is the differential resistance of the IV-tables.

# Recall (2)

In the last IBIS-summit (March ’02), the limits of C_comp in modeling the output impedance were presented.

The “real” capacitance of the buffer, as shown from the transistor model, is

1) voltage dependent (i.e. ‘non-linear’)

2) frequency dependent

Frequency domain analysis of the buffer impedance was used.

# Reading the frequency plots

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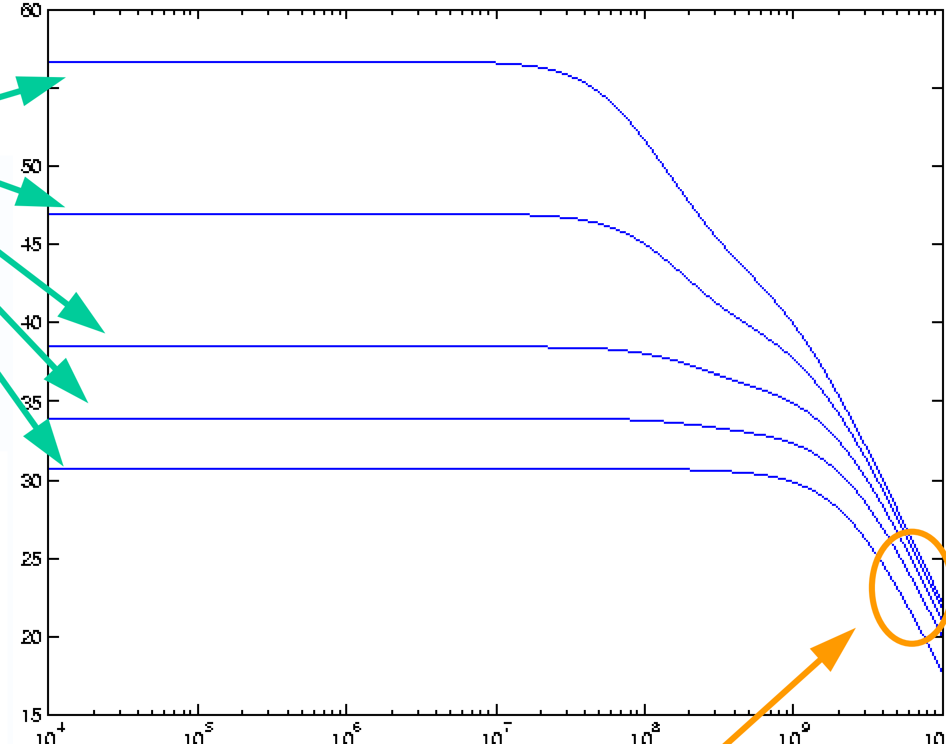
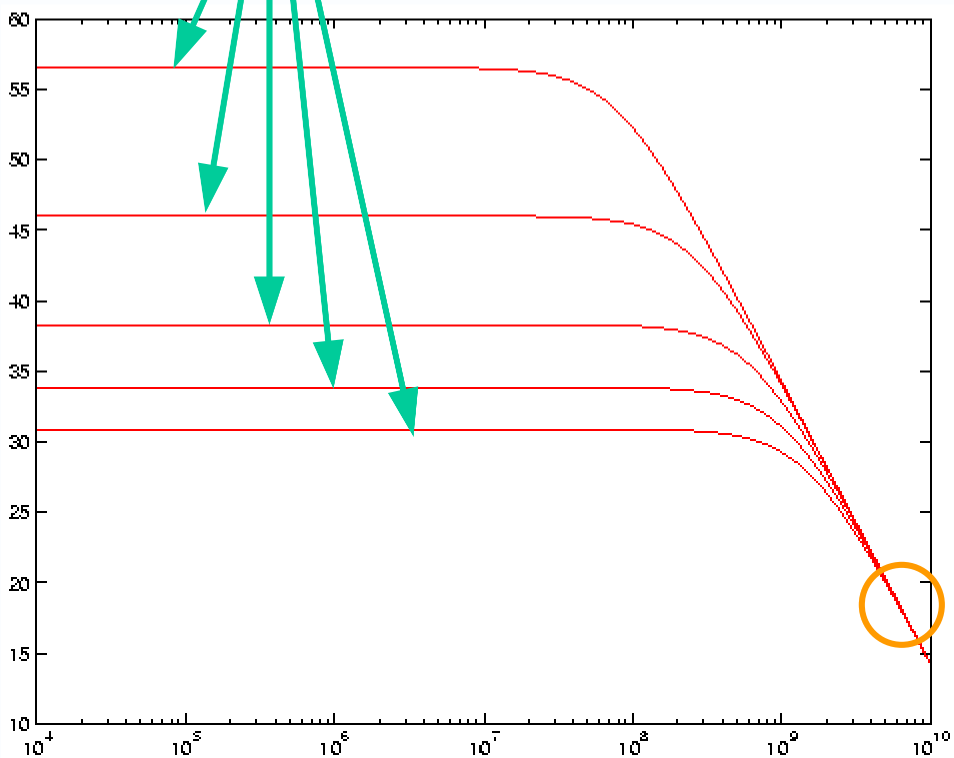
Frequency domain analysis is done in small-signal regime, at a certain bias level.
Each plot contains the result of various analyses, each one carried out at a different bias level from the others.




The “Transistor-model” capacitive behaviour at high-frequencies is non-linear (i.e. voltage dependent)!!

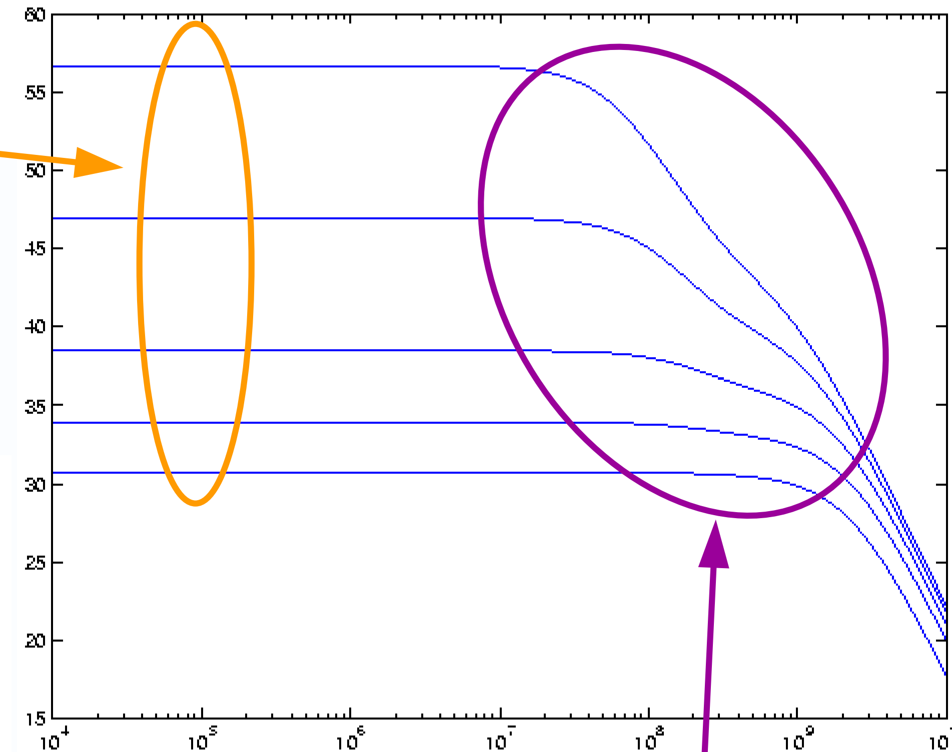


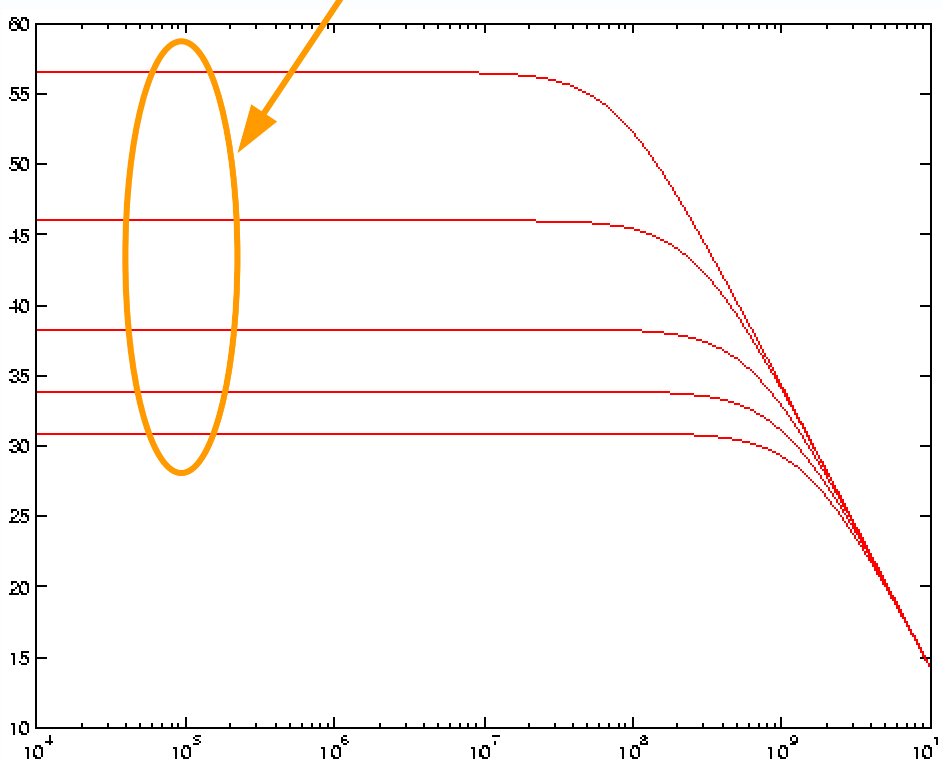

The IBIS-model capacitance “C_comp” is linear (i.e. voltage independent)!!

# Reading the frequency plots (2)

Overlapping the Transistor-model and the IBIS-model curves, the resistive zone at low frequencies (horizontal line) should perfectly match, at each bias level.

**If not**, then the IV-tables of the IBIS-model are too coarse around that bias level.

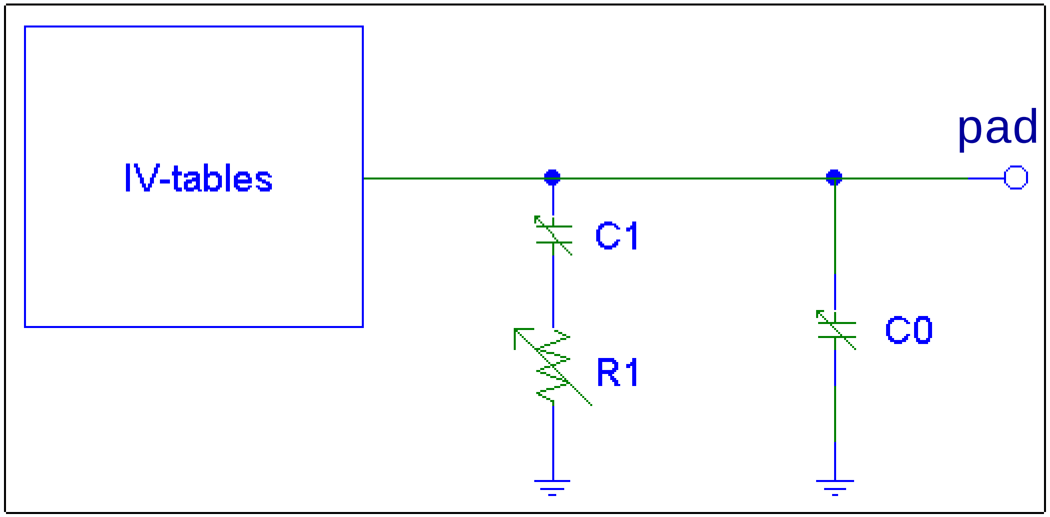



Often, the transistor model shows a “pole-zero-pole” behaviour in the [10 MHz ~ 1 GHz] range, in most of the bias levels.

# Recall (3)

A “modified IBIS” buffer was proposed :




This ‘modified-IBIS’ has been implemented in an in-house simulator. In the next slides the result will be presented.

# A 5-Volt CMOS buffer

# Output Buffer : *Transistor-model* vs. *"IBIS-classic"*

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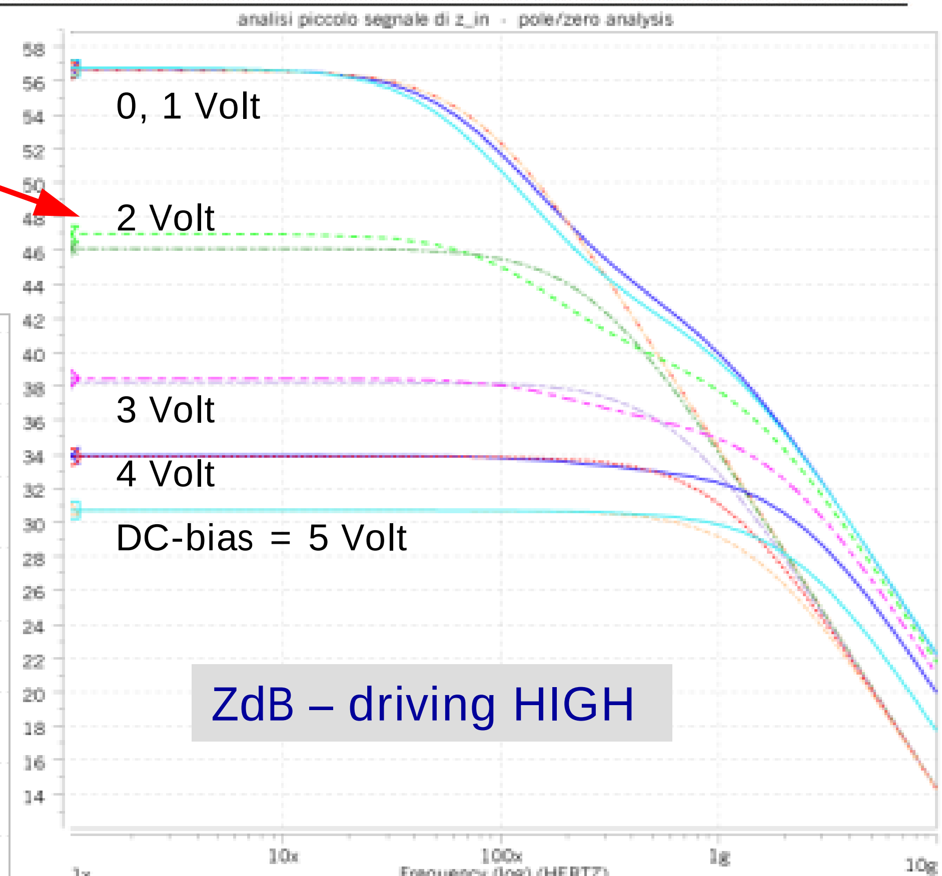
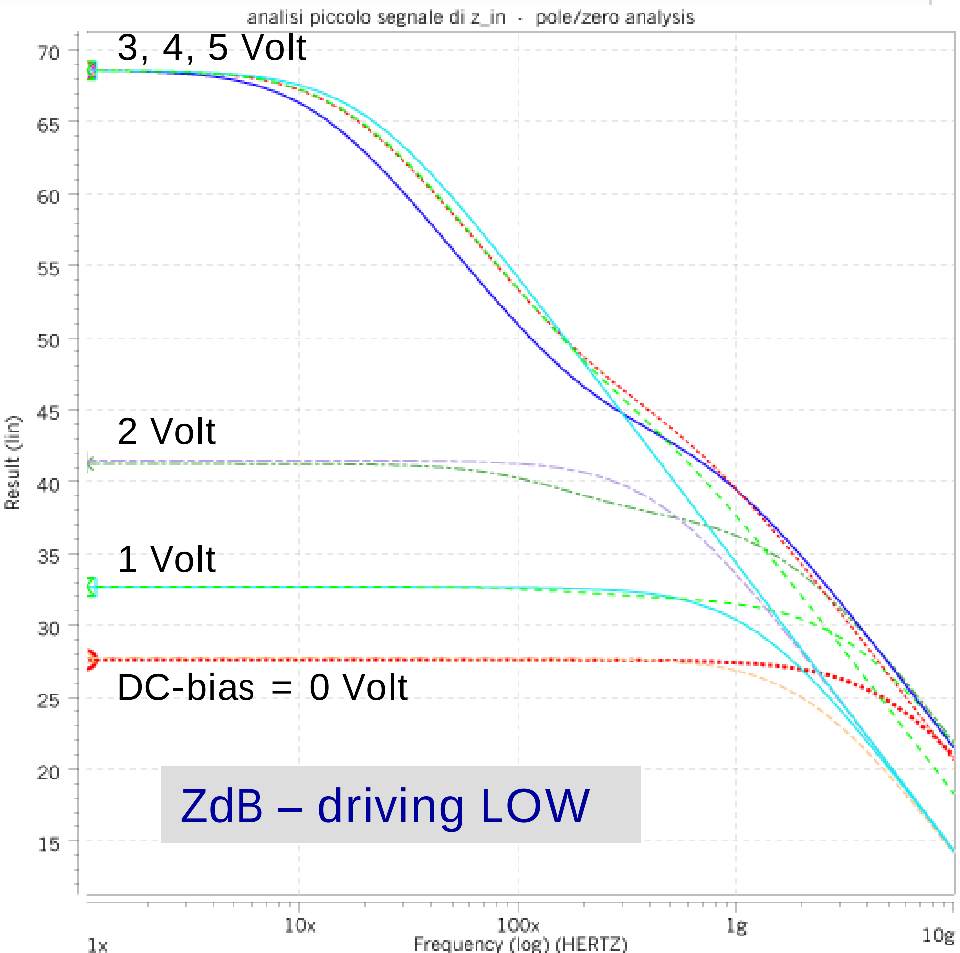
**NB:** the [pullup] IV-table in this model is not so precise at a bias of 2 Volt.



# Output Buffer :
# *Transist.-model* vs. *“IBIS-modified”*

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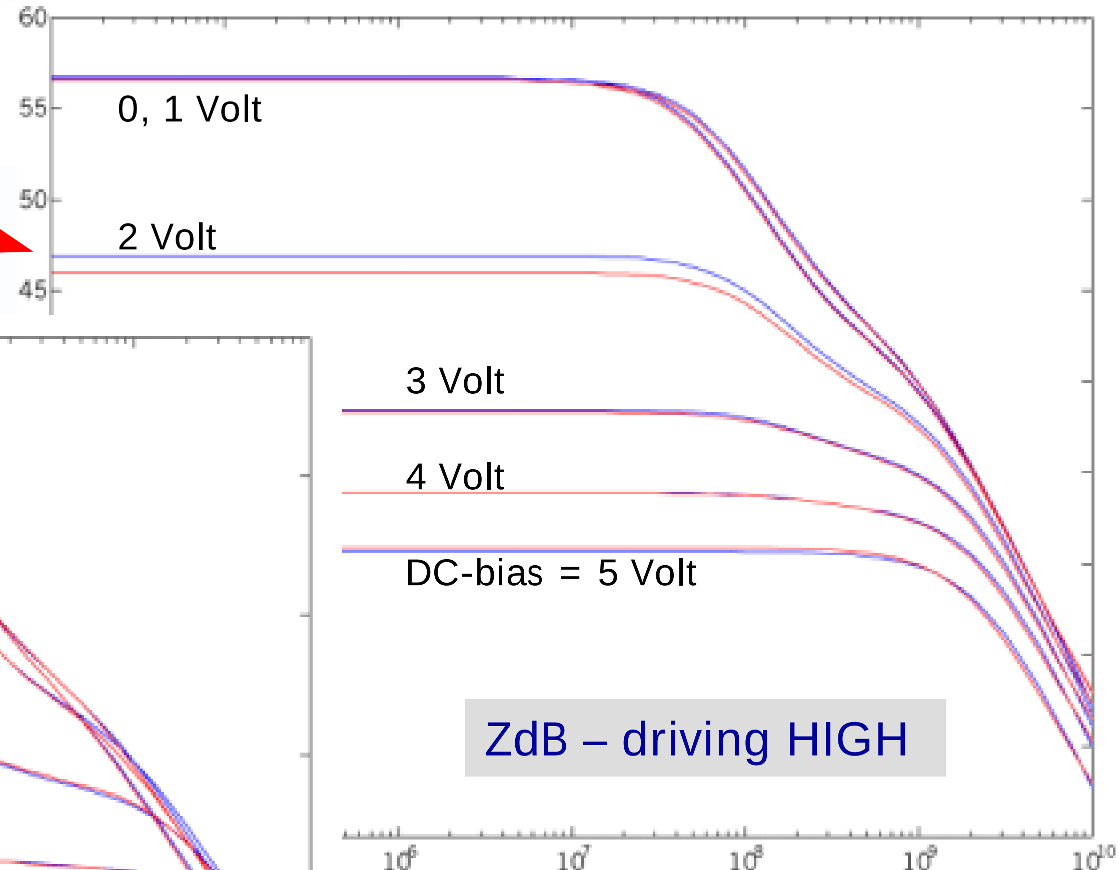
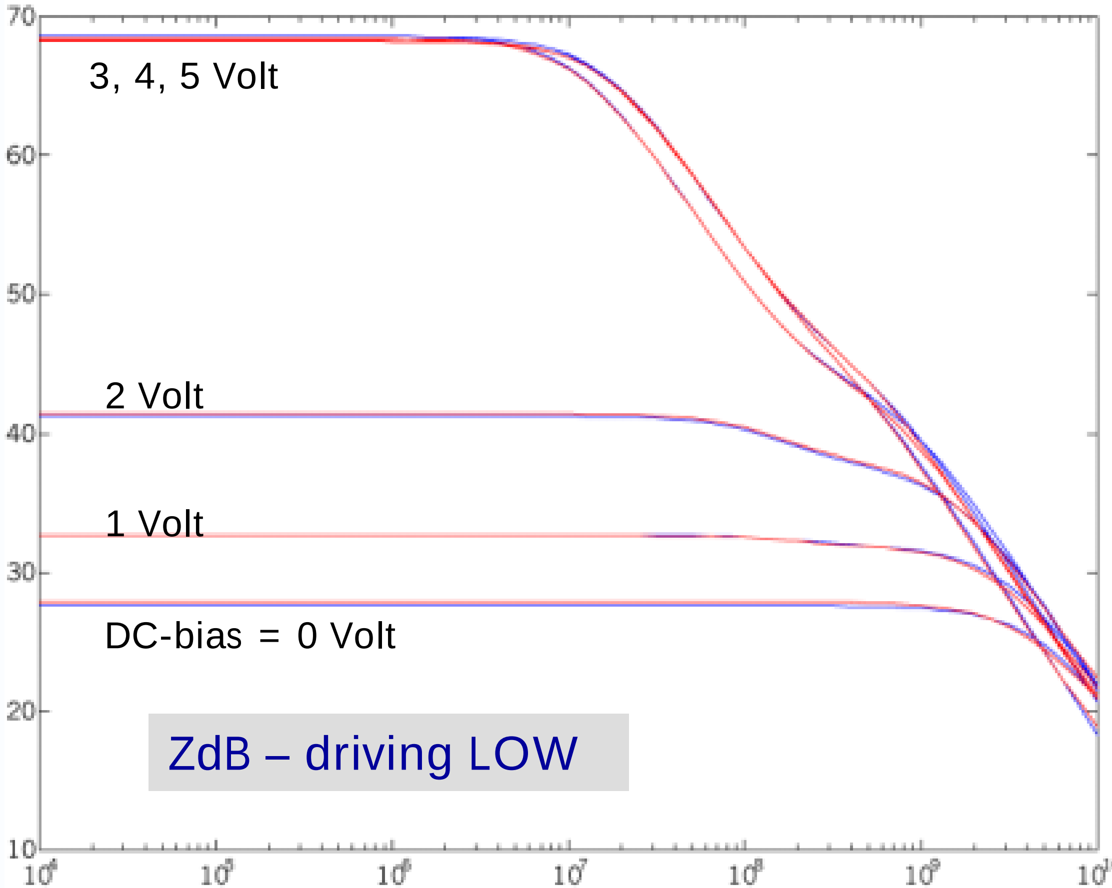
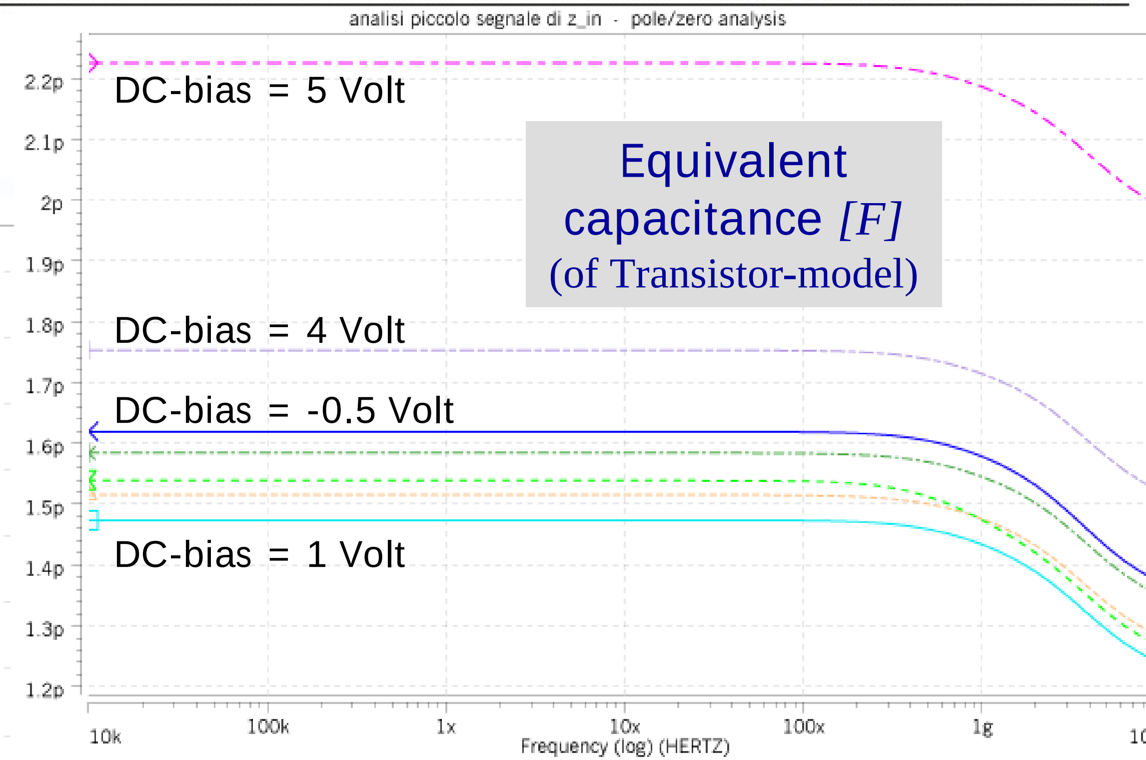
Same as before: IV-tables have not been touched!

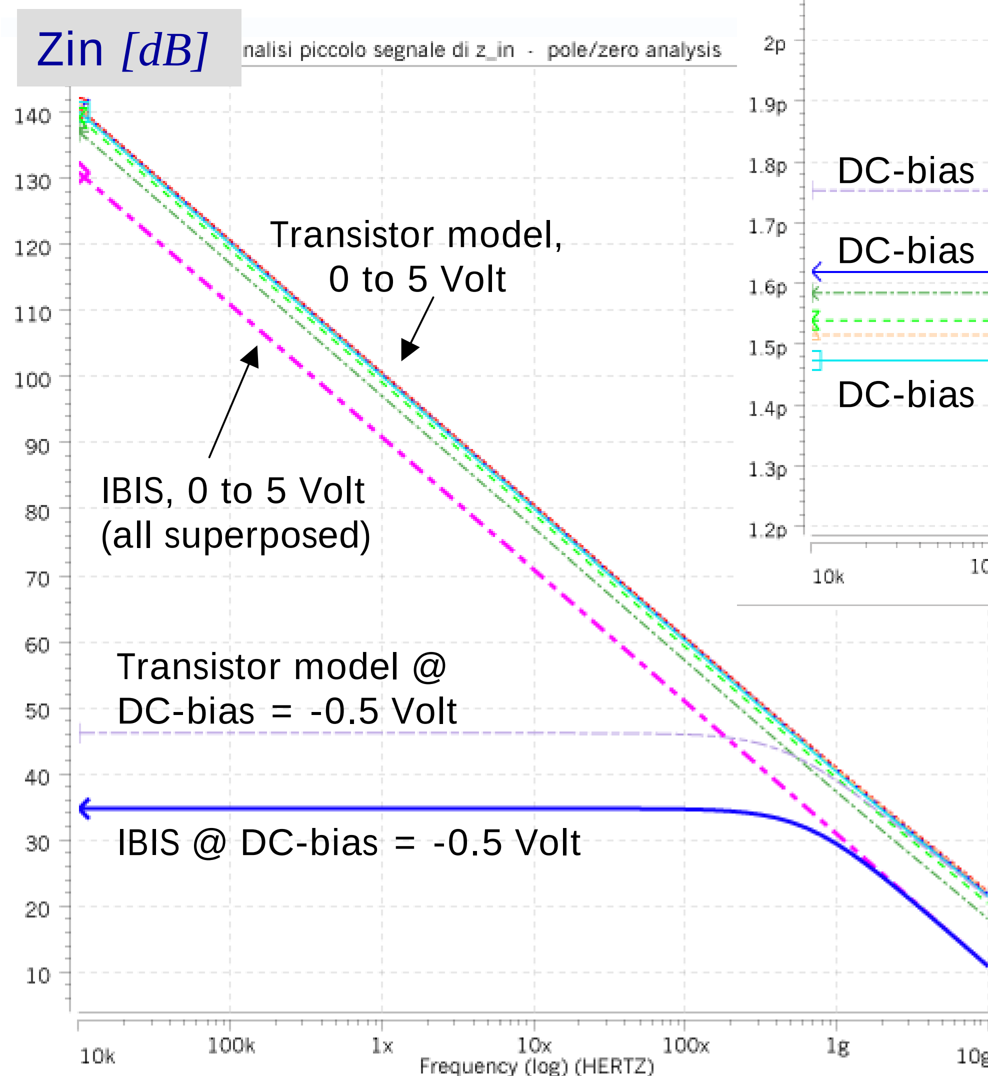



Blue is Transistor-model
Red is “IBIS-modified”

# Input Buffer :
# *Transistor-model* & *“IBIS-classic”*




In the original IBIS model C_comp = 4.55 pF !!
For the examples that will come nextly, this value has been corrected to 1.5 pF.

# How to find the parameters of the model

With the “*.pz*” SPICE command an immettance can be easily analyzed. Two frequency tables are generated in the output file: one with the poles and the other with the zeroes of the immettance under test.

An example of the command is :

```
.pz  i(Vac)  Vac
```

which analyzes the admittance “seen” by the voltage source “*Vac*”.

An example of the output tables is in the next slide.

# “.pz” : result

Most of the entries in the two tables cancel each other out.

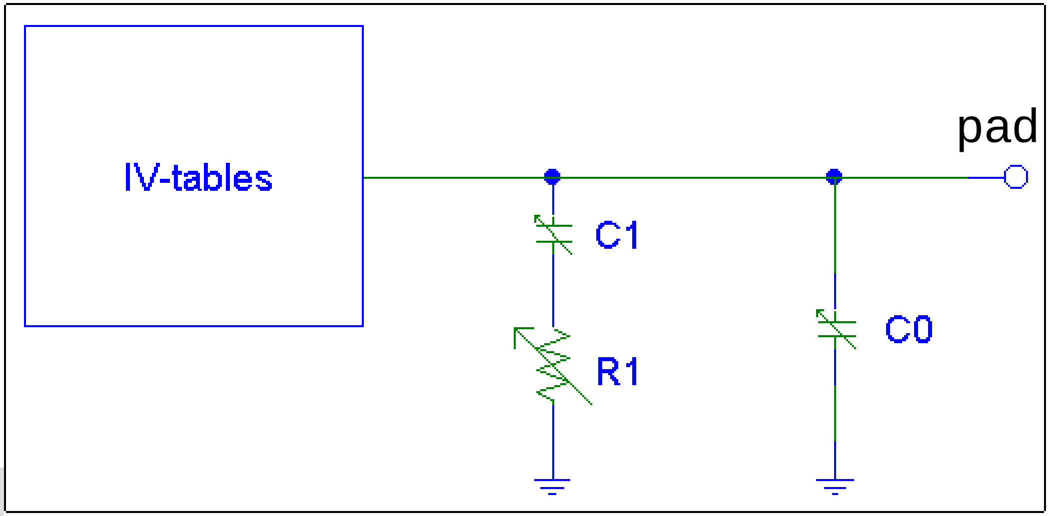
What remains (the values in red) are the frequencies of interest.

```
     zeros (rad/sec)                  zeros ( hertz)
****************************************************************
*********
   real             imag              real             imag
 -31.4675           0.                -5.0082          0.
 -19.4409x          0.                -3.0941x         0.
  -1.8874g          0.              -300.3848x         0.
  -3.8738g          0.              -616.5298x         0.
  -4.7536g          0.              -756.5546x         0.
  -7.4828g          0.                -1.1909g         0.
 -10.9686g          0.                -1.7457g         0.
 -19.1774g          0.                -3.0522g         0.
 -21.2075g          0.                -3.3753g         0.
 -25.0000g          0.                -3.9789g         0.
 -55.9813g          0.                -8.9097g         0.
-137.7153g          0.               -21.9181g         0.
-142.3580g          0.               -22.6570g         0.

     poles (rad/sec)                  poles ( hertz)
****************************************************************
*********
   real             imag              real             imag
 -31.4666           0.                -5.0081          0.
 -19.4409x          0.                -3.0941x         0.
-400.1013x          0.               -63.6781x         0.
  -3.6949g          0.              -588.0579x         0.
  -4.7535g          0.              -756.5382x         0.
  -5.8288g          0.              -927.6802x         0.
  -7.4921g          0.                -1.1924g         0.
 -10.9716g          0.                -1.7462g         0.
 -19.1878g          0.                -3.0538g         0.
 -21.3640g          0.                -3.4002g         0.
 -25.0000g          0.                -3.9789g         0.
 -55.9813g          0.                -8.9097g         0.
-137.7972g          0.               -21.9311g         0.
-142.3622g          0.               -22.6576g         0.
```

# The equations of the non-linear network parameters

The parameters for the topology on the right are related to the poles & zero as follows:




$$C_0 = G_{I-V} \cdot \frac{\omega_Z}{\omega_{P1} \cdot \omega_{P2}}$$

$$\frac{1}{R_1} = C_0 \cdot \left( \omega_{P1} + \omega_{P2} - \omega_Z - \frac{\omega_{P1} \cdot \omega_{P2}}{\omega_Z} \right)$$

$$C_1 = \frac{1}{R_1 \cdot \omega_Z}$$

where $G_{I-V}$ is the (differential) conductance representing the IV-tables

# Time Domain Comparisons

two examples

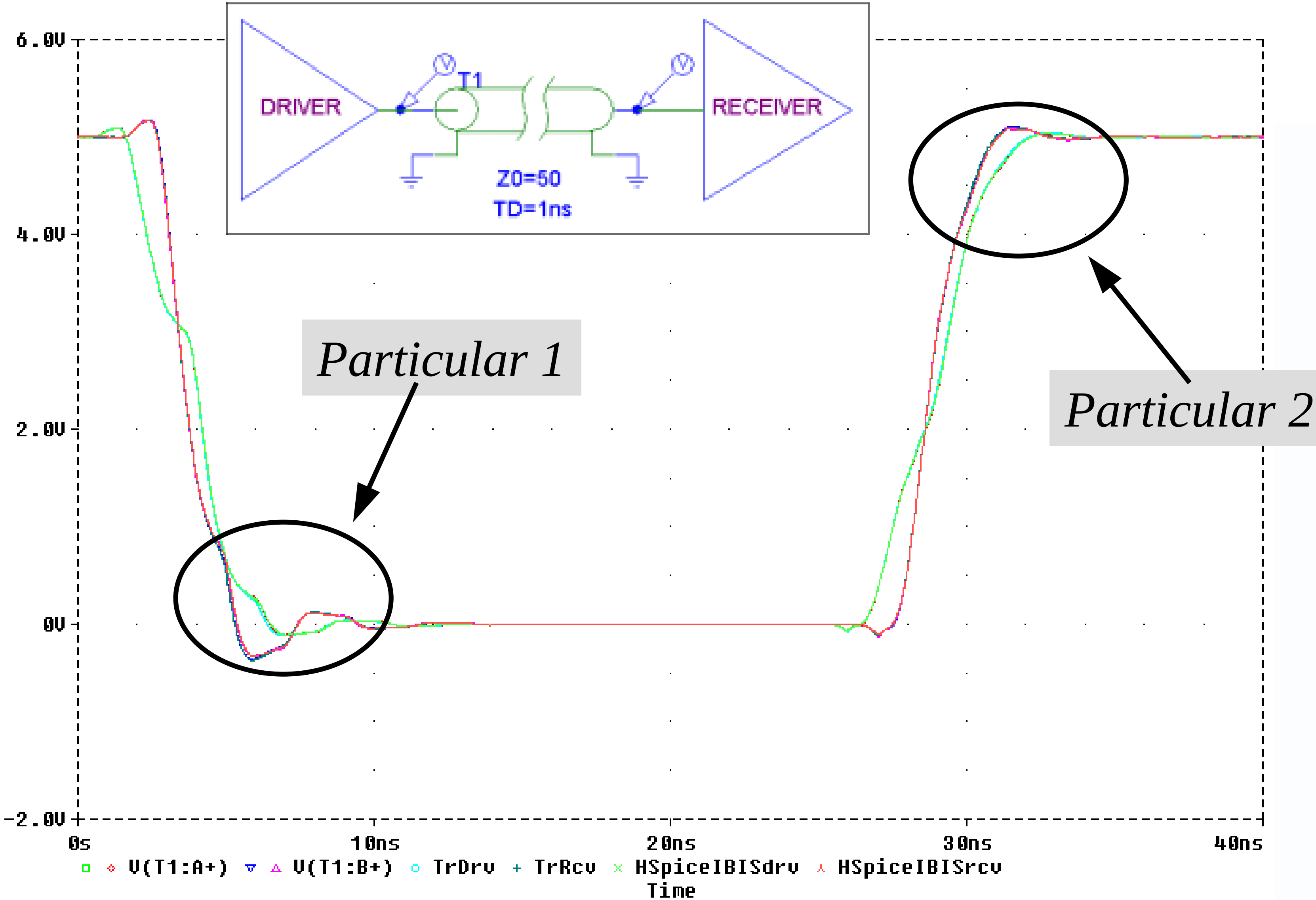
# Example 1

Driver and receiver are the 5-Volt CMOS models considered earlier.

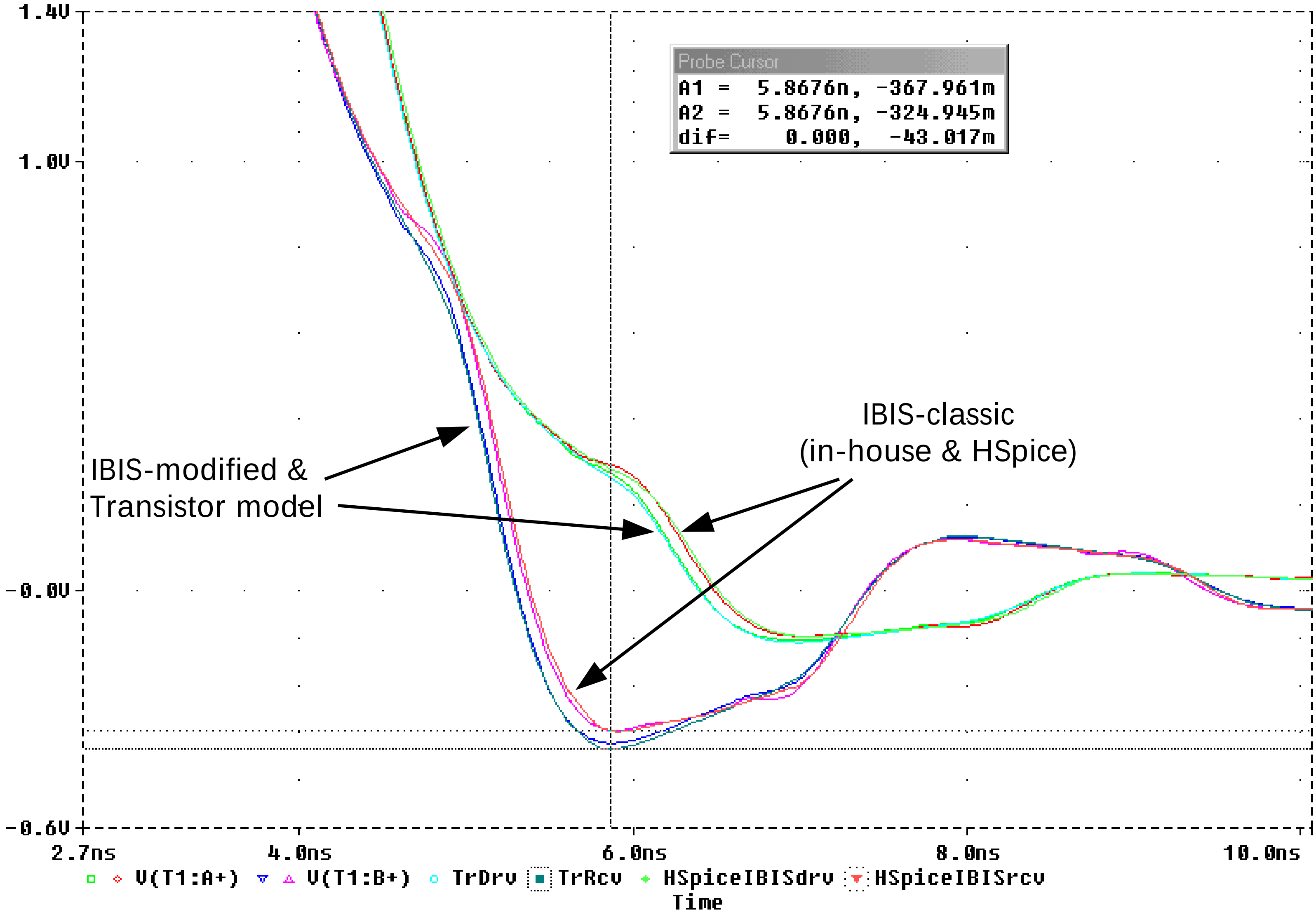
This first example considers a relatively short line (with respect to $T_r$).

In this case the reflections (i.e. where the impedance plays) are buried in the transition...

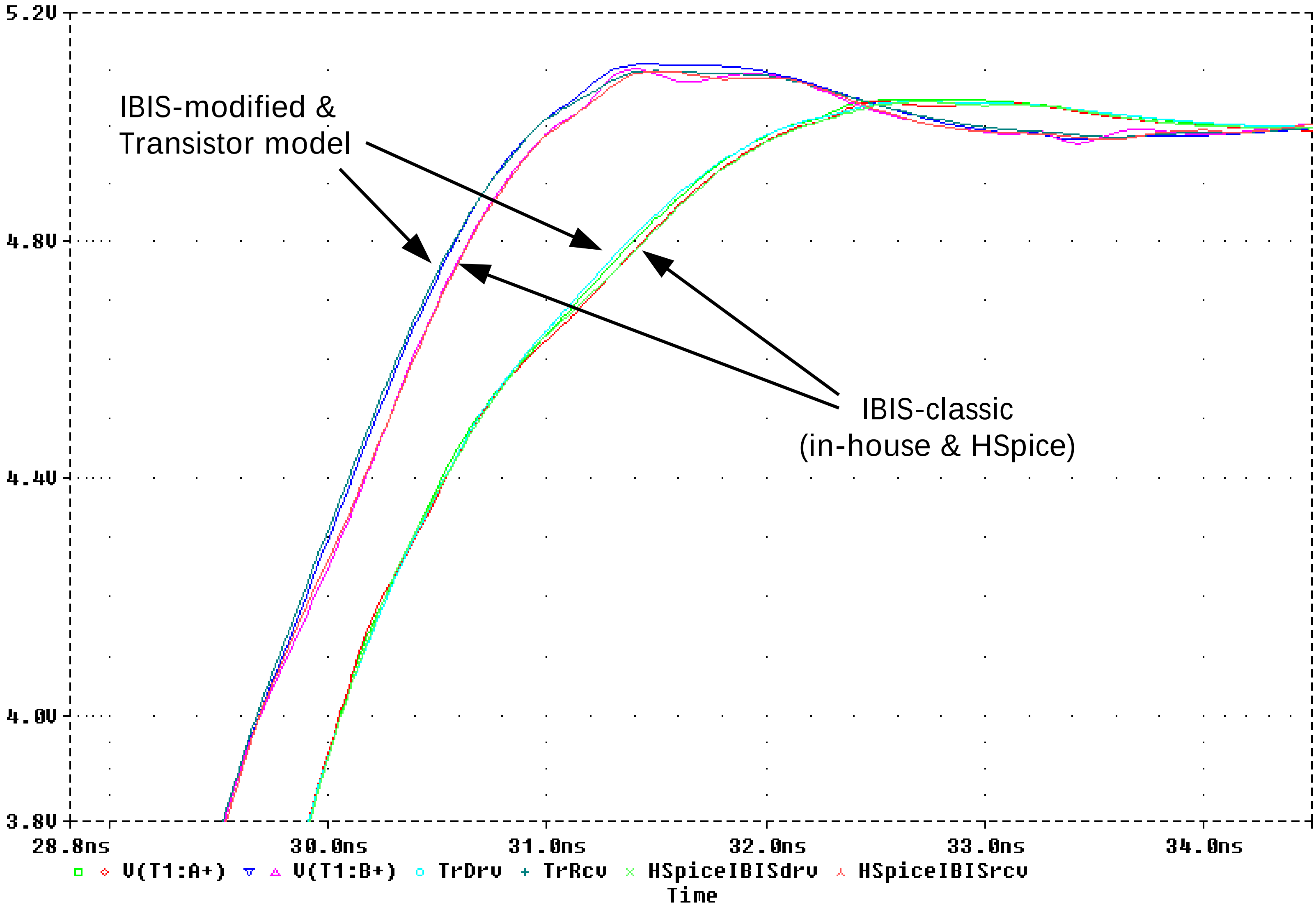
# Example 1 – global view



# Example 1 – particular 1



# Example 1 – particular 2



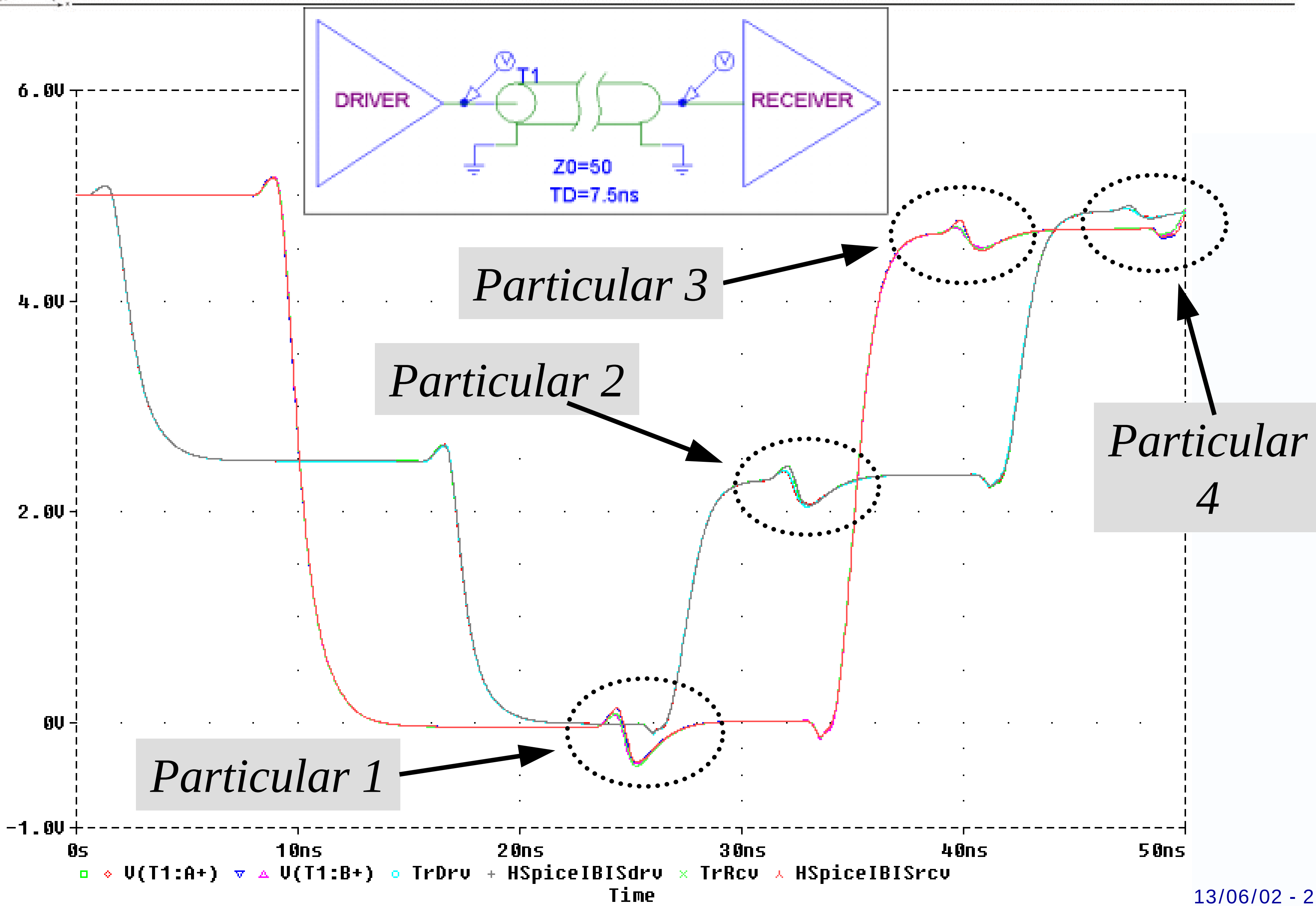
# Example 2

The second example considers a very long line (with respect to $T_r$).

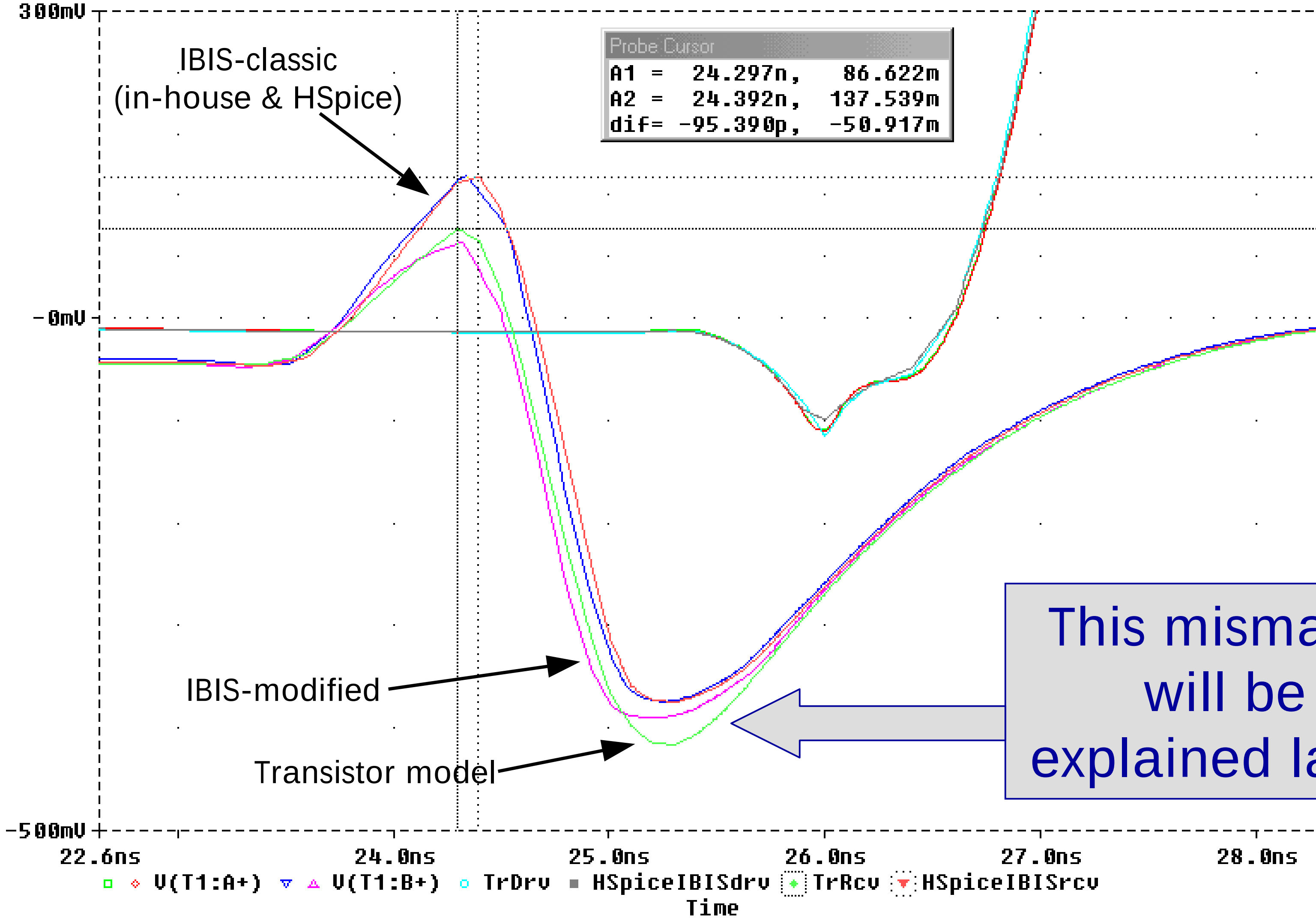
In this case the reflections (i.e. where the impedance plays) are more visible...

Again, driver and receiver are the 5-Volt CMOS models considered earlier.

# Example 2 – global view

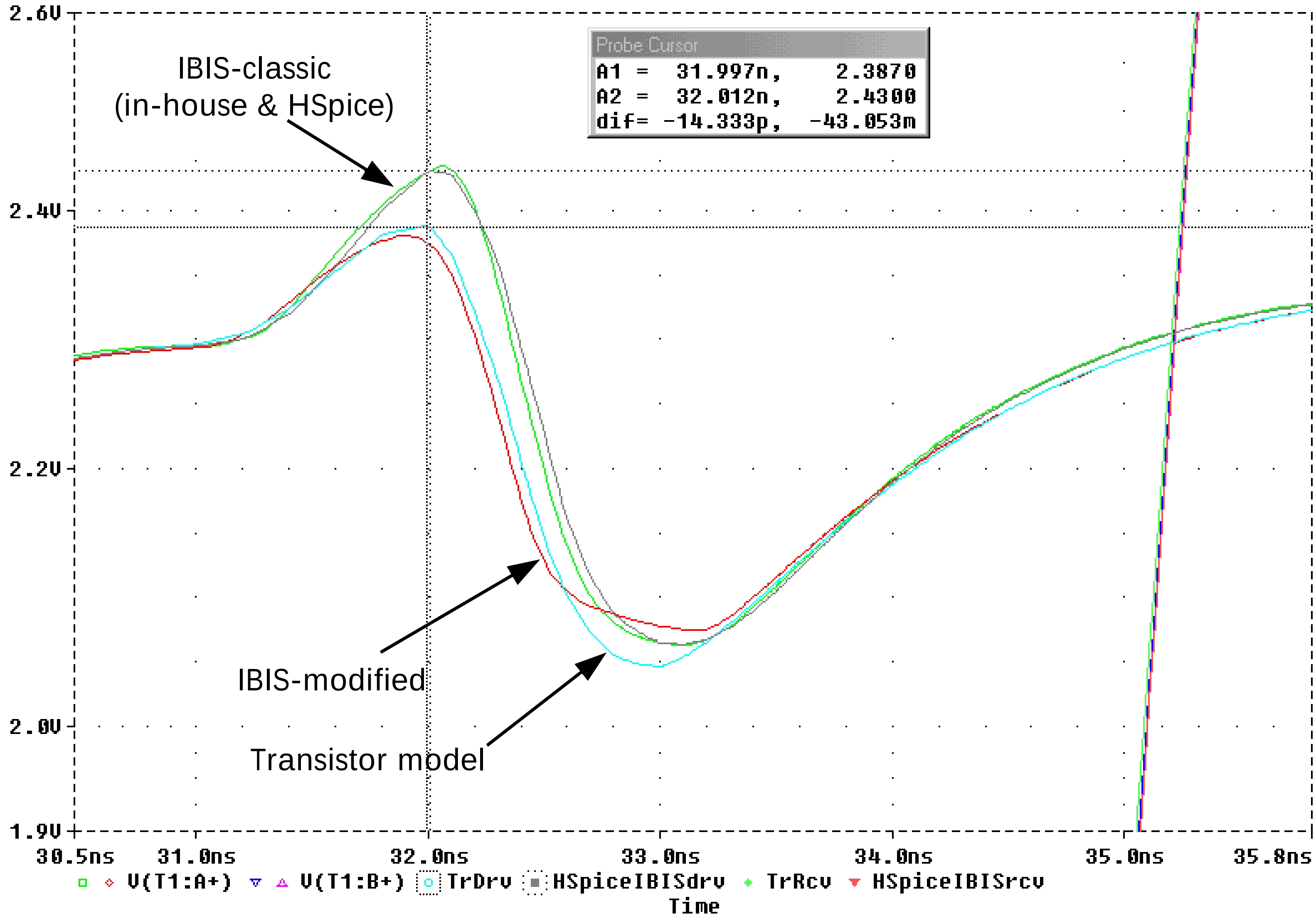


# Example 2 – particular 1

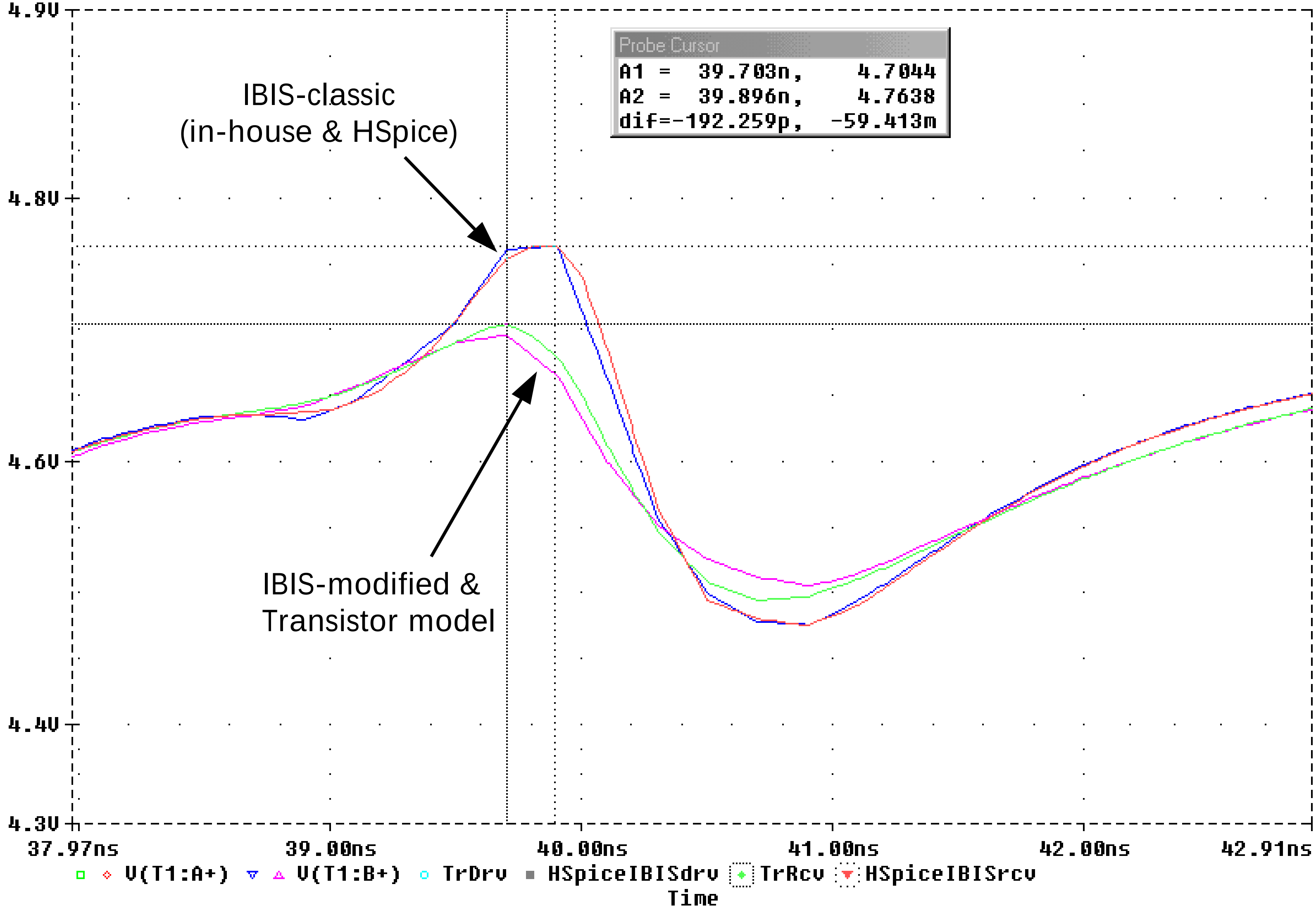



This mismatch will be explained later.

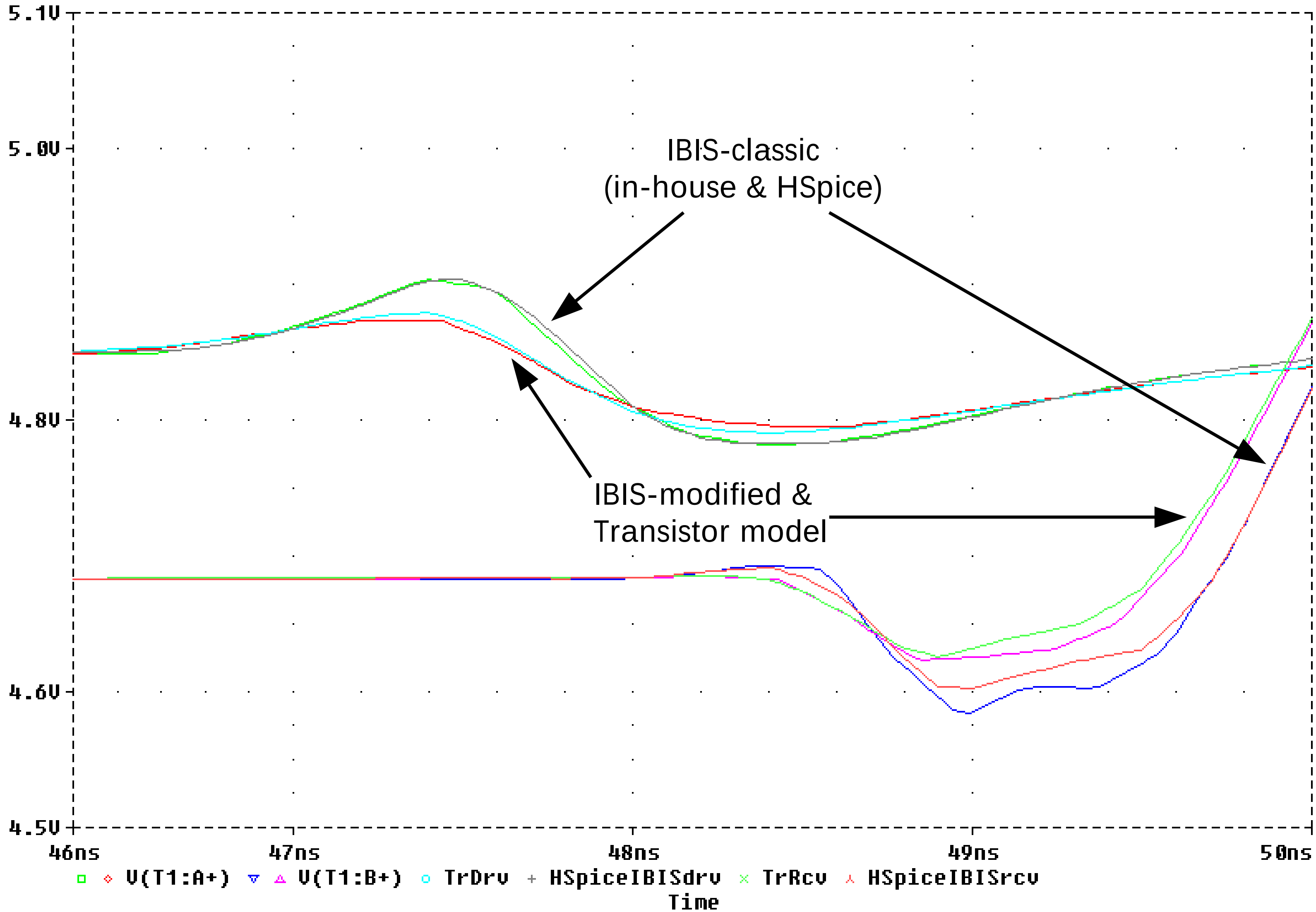
# Example 2 – particular 2



# Example 2 – particular 3



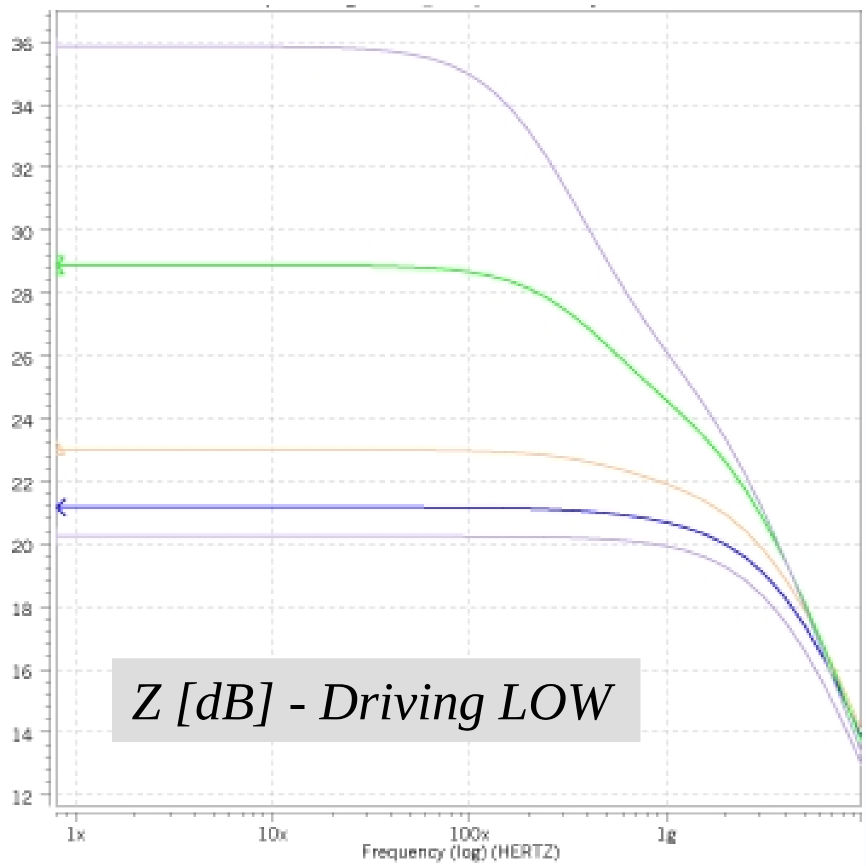
# Example 2 – particular 4

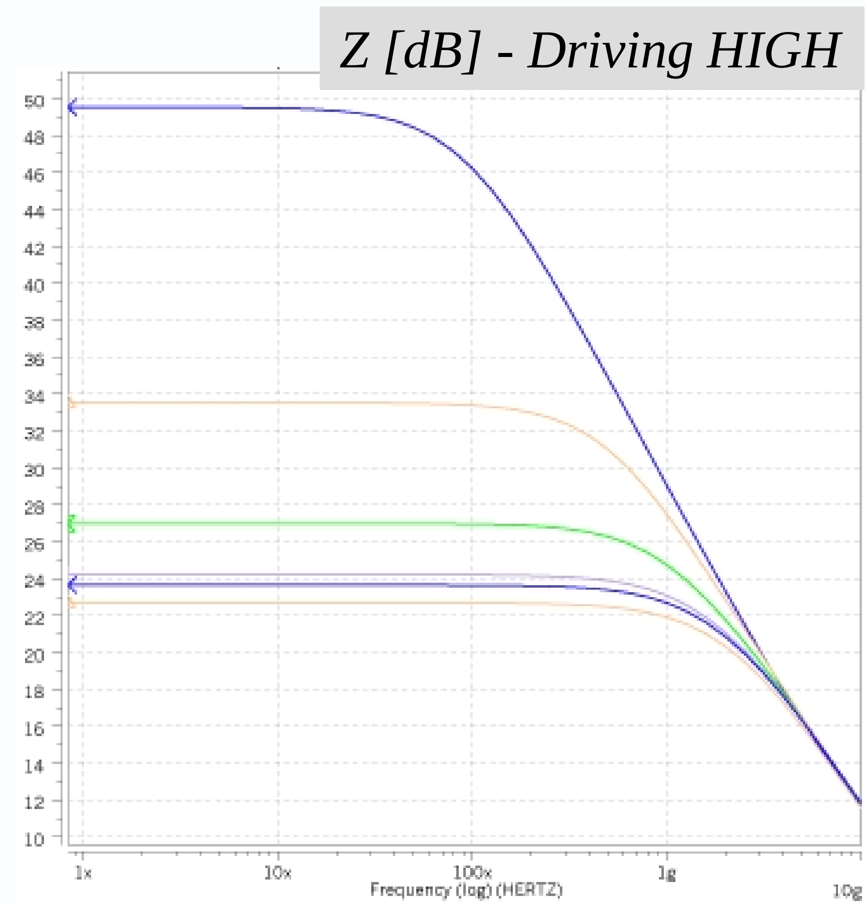


# What about other buffers ?

Do we find a similar
“frequency-signature” in nature ?

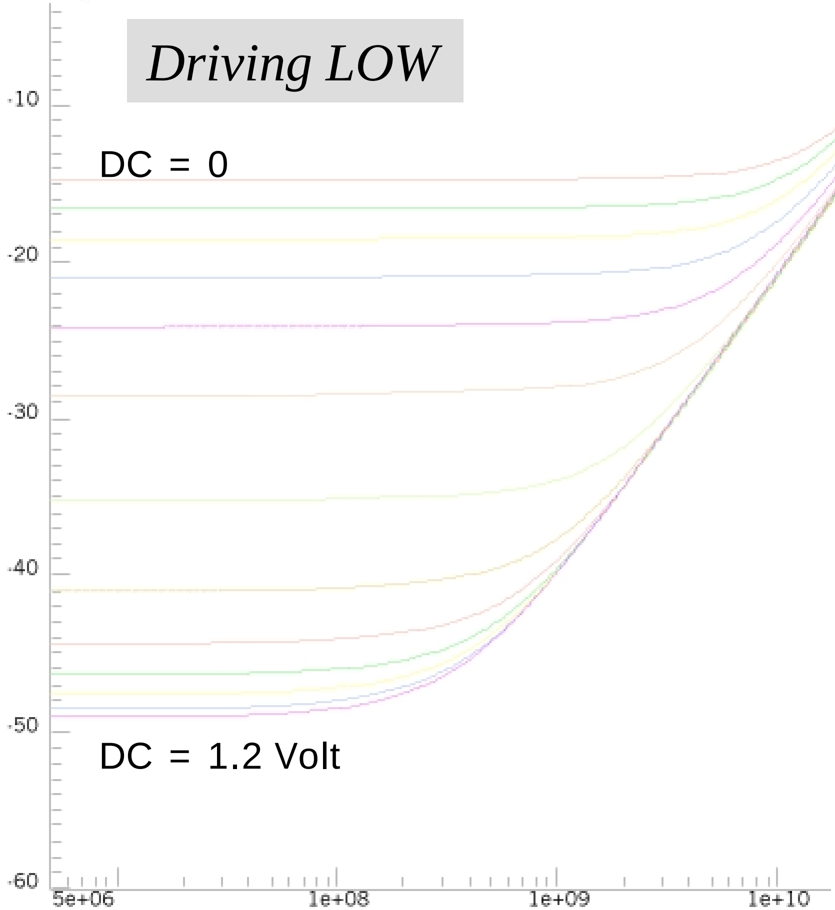
# IDT – ALVCH, 3.3 Volt buffer

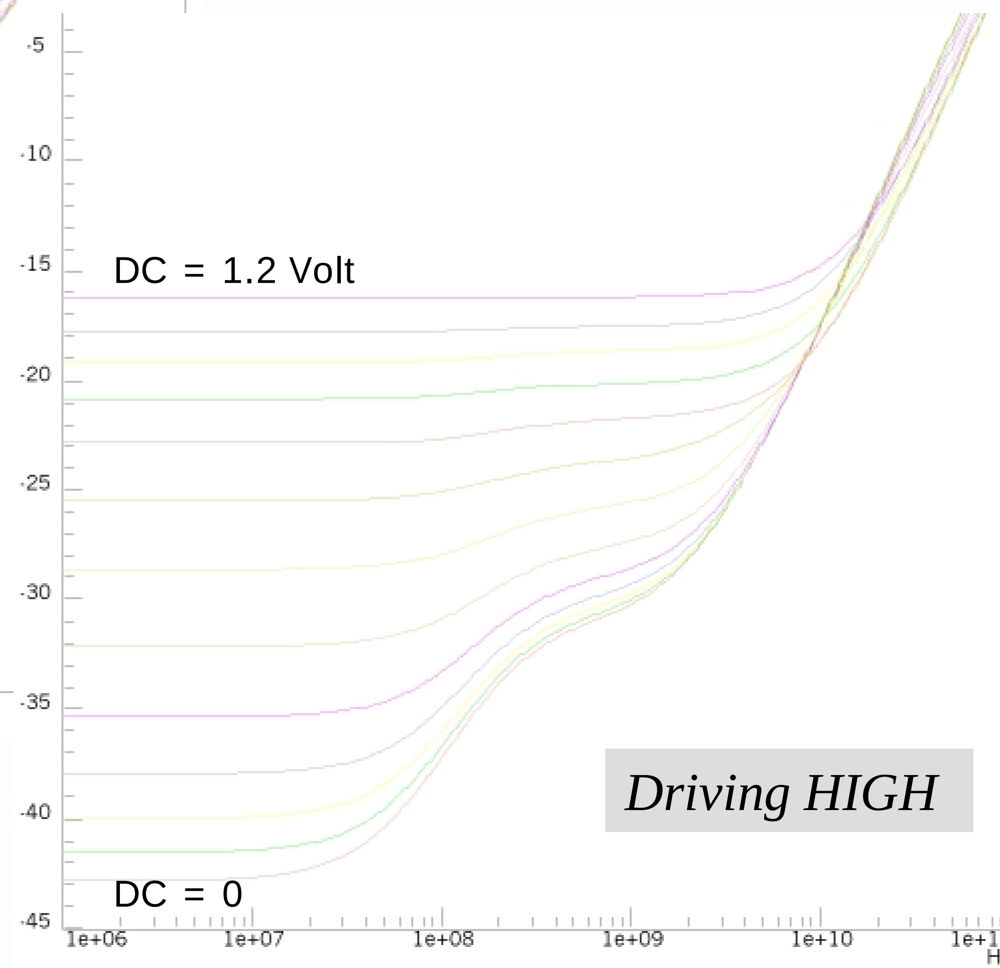


# ST-Microelectronics, 1.2 Volt buffer

$Y_{out}$ [dB] vs. *frequency*




NB: both diagrams show that the “HF-Ccomp” is non-linear

# What would change in the IBIS specification

# What would change in IBIS

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```
[Model]  modelname
pole_high  |this is pole_1 in the high-state
|[Volt]           typ [Hz]          min [Hz]      max [Hz]
  0V               6.37E7             NA            NA
  1V               5.36E7             NA            NA
  2V               1.15E8             NA            NA
...                 ...              ...           ...
  5V               2.53E8             NA            NA
|
zero_high  |this is the zero in the high-state
  0V               3.00E8             NA            NA
  1V               2.83E7             NA            NA
...                 ...              ...           ...
  5V               2.56E8             NA            NA
|
pole_high  |this is pole_2 in the high-state
  0V               9.28E8             NA            NA
...                 ...              ...           ...
|
pole_low   |this is pole_1 in the low-state
  0V               2.00E8             NA            NA
...                 ...              ...           ...
|
zero_low   |this is the zero in the low-state
  0V               2.01E8             NA            NA
...                 ...              ...           ...
|
pole_low   |this is pole_2 in the low-state
  0V               5.25E9             NA            NA
...                 ...              ...           ...
  5V               4.24E8             NA            NA
```

A possible organization of the data inside an IBIS file.

# Comments

- Six new subparameters in the keyword [model], to use according to "model-type" : *pole_in*, *zero_in*, *pole_high*, *zero_high*, *pole_low*, *zero_low*.

- To ease simulators' implementation, only three scenarios should be made possible (for each state of the buffer) :

  - none of these new sub-parameters is used
  - one *pole_xx* subparameter is used (resulting in a "non-linear & state-dependent" capacitance)
  - two *pole_xx* and one *zero_xx* subparameters are used

# Comments (2)

- Using tables of pole-frequencies and zero-frequencies the data are directly the result of the "*.pz*" SPICE command.

- It seems useless (when clamping diodes are present) to extend the bias voltage far beyond the power rails : in a normal situation, 6~8 bias entry in each table are enough.

- If the spec will ever extend to more then 2 poles and 1 zero, no addition of new keyword/subparameters is needed.

# Comments (3)

- It may be worth considering the addition of an extra new subparameter (the seventh), to take into account some empirical “derating” of the buffer performance (due to metallization and pad capacitance, which are not present in pre-layout transistor models).

Possible names could be: *C_metal* or *C_derate*.

This subparameter could be useful also when “C_comp” is used.

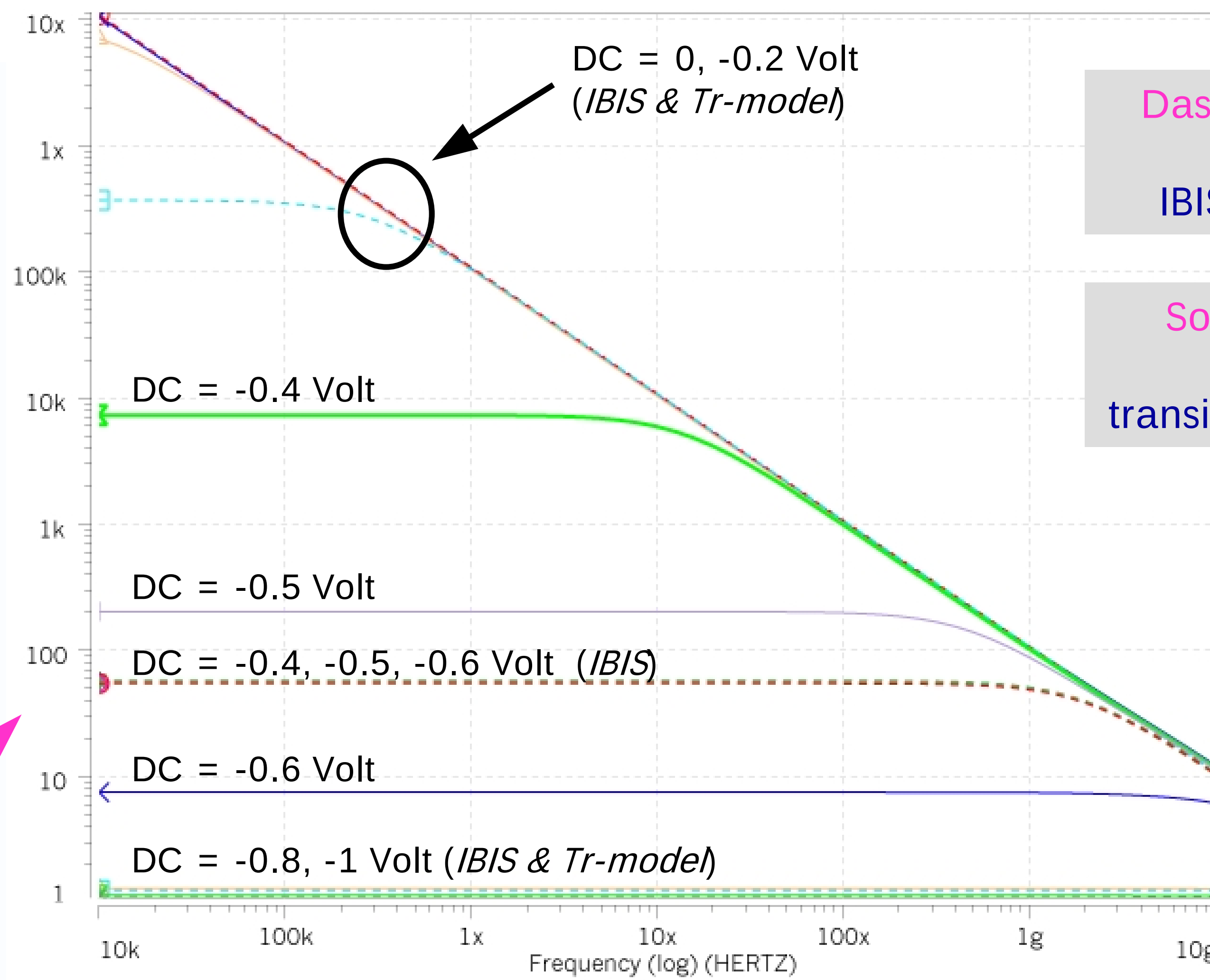
# About the quality of IBIS models

A very interesting aspect of this work is the *frequency-domain analysis* tool.

We have seen throughout the presentation that it instantly shows the fidelity of an IBIS model to the originating transistor model (in its static components).

Let's use it now to find the source of the problem we encountered on slide 22 ...

# 5-Volt CMOS input model - $|Z_{in}|$




Dashed lines are IBIS-model

Solid lines are transistor-model

This scale is in “ohm”

# Comments

From the previous image we see that at a bias of *–0.4 Volt* the IV-tables result in a (differential) conductance that is considerably lower than the 'real' one :

$$|Z_{\text{in, ibis}}| \quad = \quad 57 \text{ ohm} \qquad @ \quad DC = -0.4 \; Volt$$

$$|Z_{\text{in, tr-model}}| \; = \; \sim 7 \text{ kohm} \qquad @ \quad DC = -0.4 \; Volt$$

This indicates a lack of precision around this bias level in the IV-tables, which may be the cause of the mismatch seen in the time-domain example on slide 22 .

In fact, from the image on the next slide, it is clear that the IBIS model starts clamping earlier.

# DC current vs. Bias voltage

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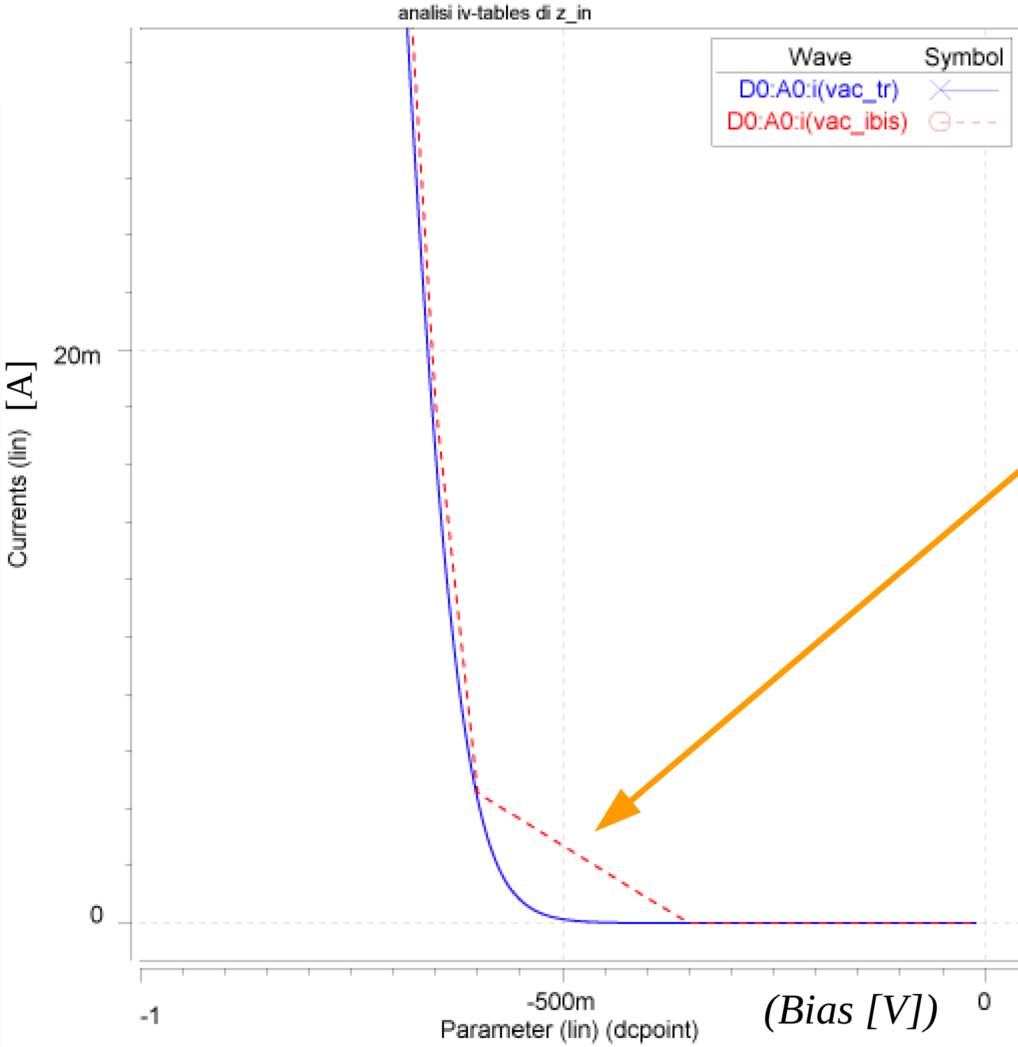



The IBIS model clamps earlier.

This is the cause of the mismatch seen on slide 22.

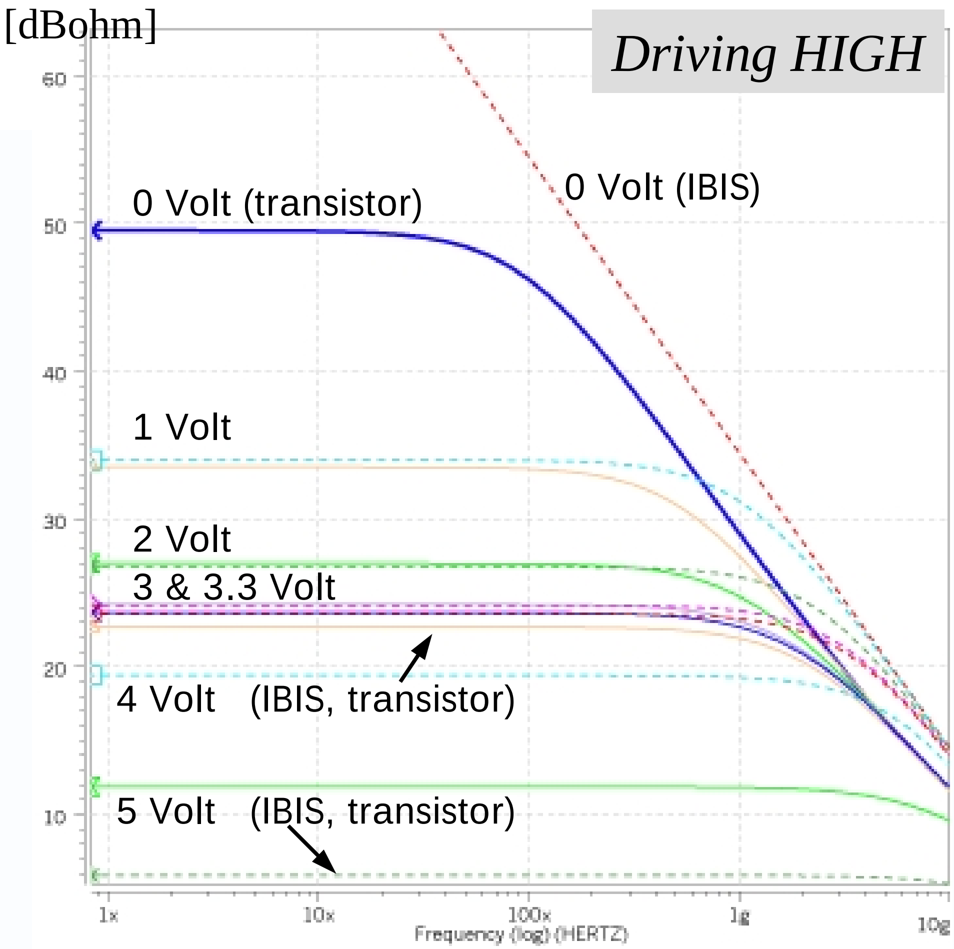
# A 3.3V buffer from the web

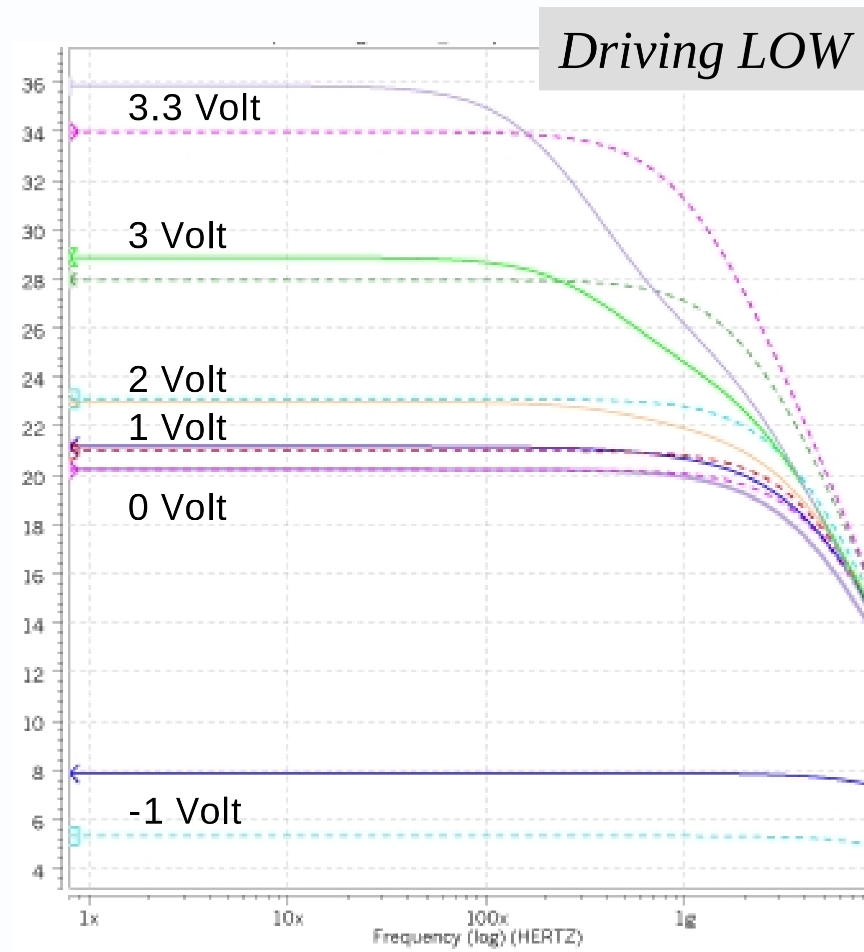
In the next two slides, the FD analysis tool is used on a 3.3V buffer model, downloaded from the web.

In less than 10 seconds of simulation, we get the three following images, where we immediately notice that :

- at some bias levels the differential resistance (I-V tables) is not very accurate;
- the value of C_comp is a little "optimistic".

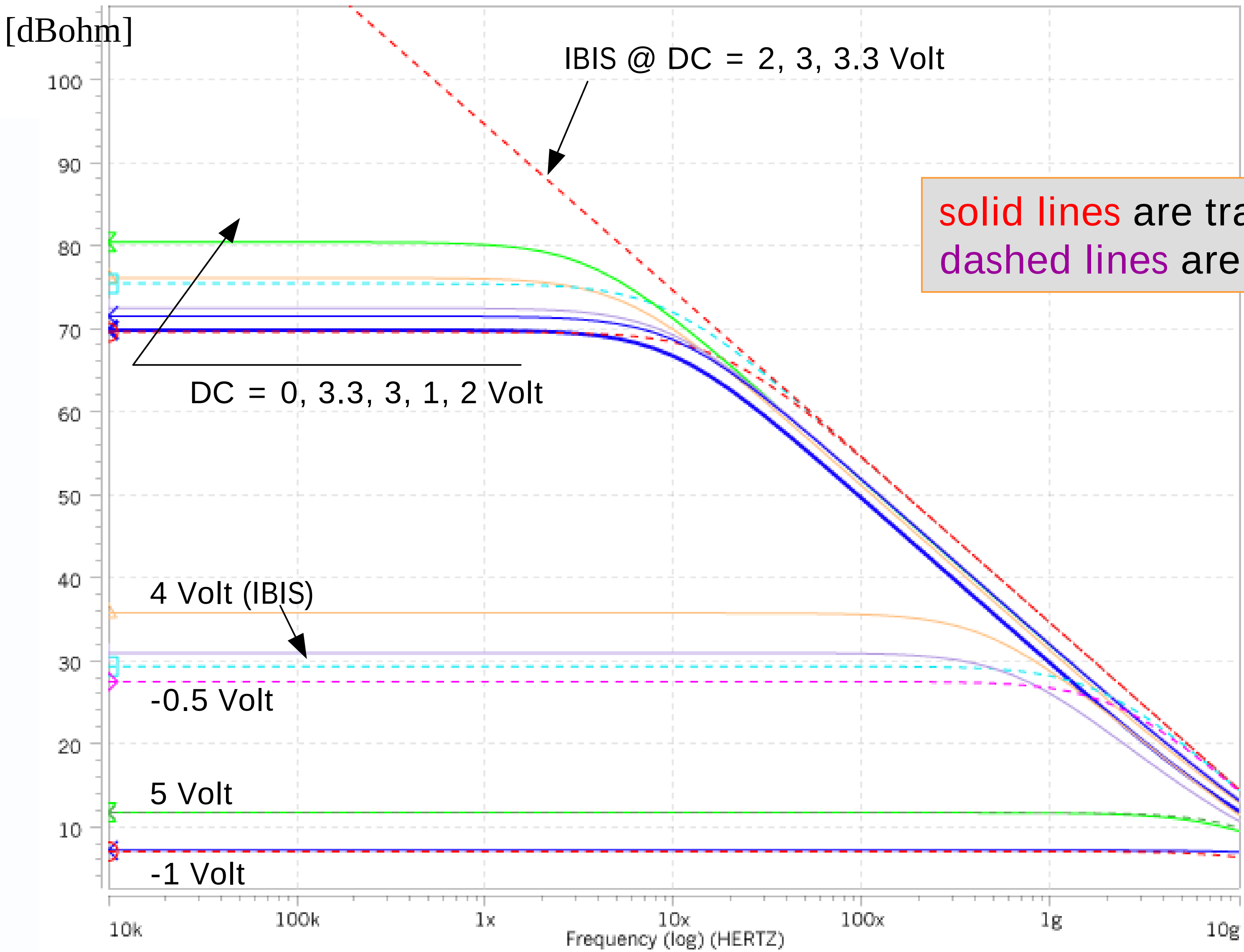
# 3.3V Output Buffer Plots




solid lines are transistor model
dashed lines are IBIS model

# 3.3V Input Buffer Plot




solid lines are transistor model
dashed lines are IBIS model

# Conclusions

# Conclusions (1)

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- The buffer impedance has been demonstrated to be non-linear also in its reactive component.

- The “pole-zero-pole” behaviour of the output impedance has been reported for three different buffers.

This was intended to demonstrate that it is a common feature.

# Conclusions (2)

- A model taking into account this behaviour of the buffer impedance has been proposed*, and a technique to automatically extract the required parameters has been outlined.

The impact on time-domain simulations has been shown for a particular  model. The improved behavioral model proved to match the simulations done with the originating transistor-model more closely, although a good matching is already achieved with the standard IBIS model.

* see also the presentation at the March 2002 IBIS-summit in Paris.

# Conclusions (3)

- In this work it is also shown how “uncertain” the determination of the parameter *C_comp* is.

A major advantage of the improved model is the clear definition of the parameters substituting C_comp. This should ease the production of IBIS models of a better quality level.

# Conclusions (4)

- The frequency domain approach shown in this work proves to be very powerful, and it may be used to increase the overall quality of IBIS models.

  e.g., when producing a new IBIS model it may be efficiently used to quickly check the accuracy of its static part (*IV-tables* & *C_comp*).

- Inclusion of the "enhanced non-linear C_comp" in the IBIS specification will force model-makers to run frequency domain analysis. Thus, it will indirectly improve the overall quality of IBIS models.

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