Information
and Communication
Networks

IBIS-models today, their parameters and their accuracy

Eckhard Lenski Siemens AG

IBIS summit meeting DAC 2002

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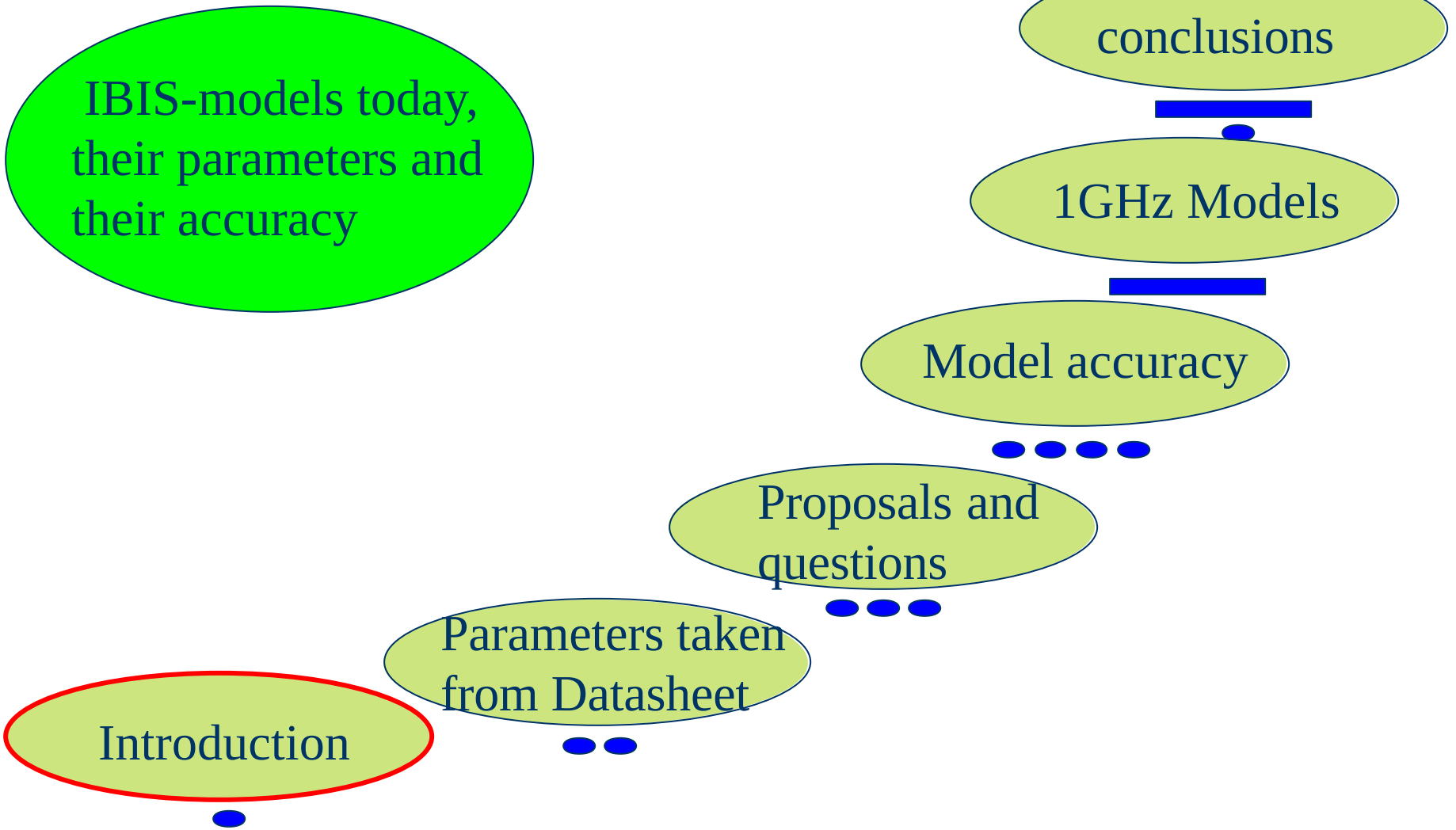

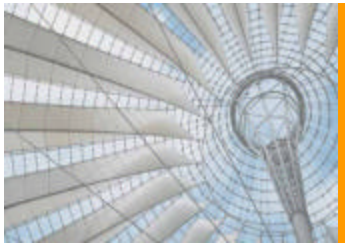

Introduction

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ICN WN OP TDC TC 3 Modeling group

Behavioral models since 1993

Model-sources

- measurements 1%
- HSPICE 40%
- IBIS 50%
- Databook 9%

Library with more than 1500 models (of IOs)

Models for new technologies (LVDS , CAN , PCML , ...)

Datasheet definitions

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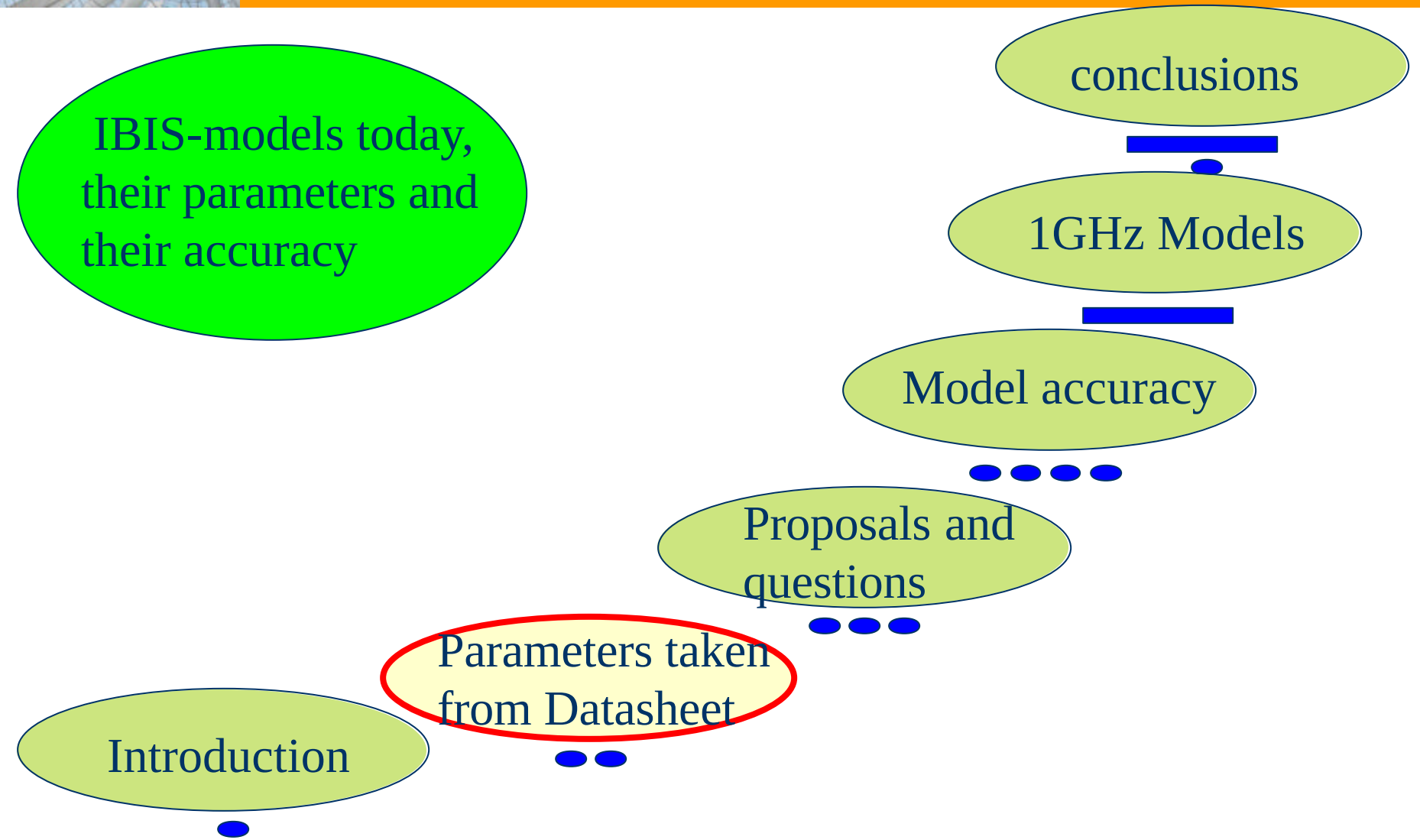

Over-undershoot examples

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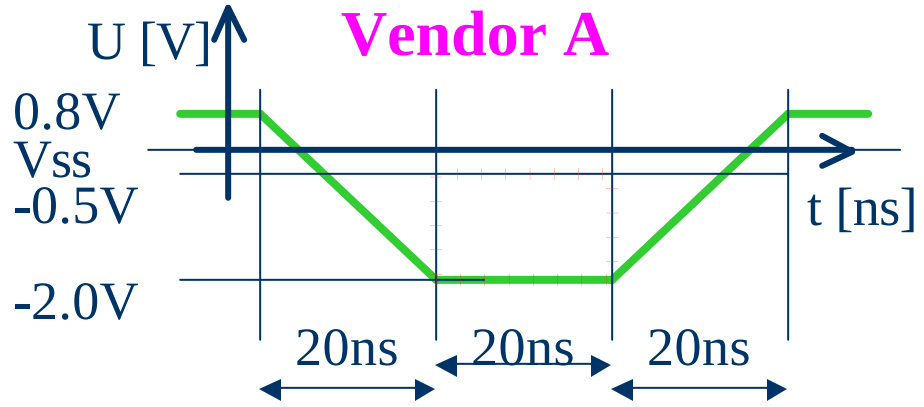

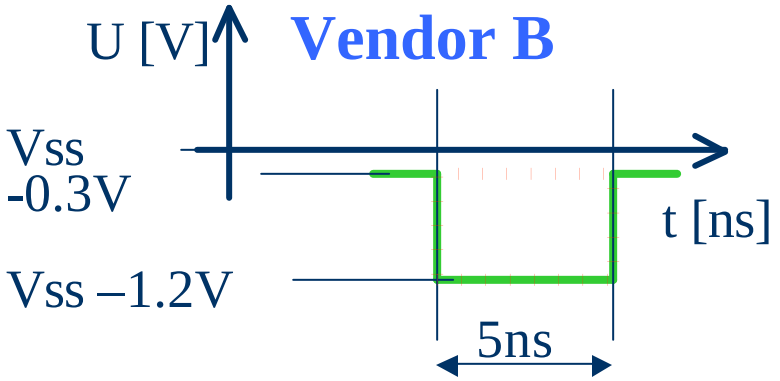

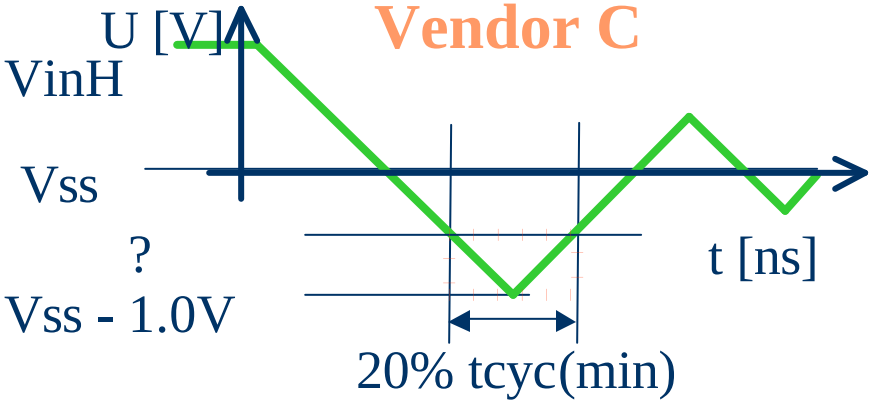

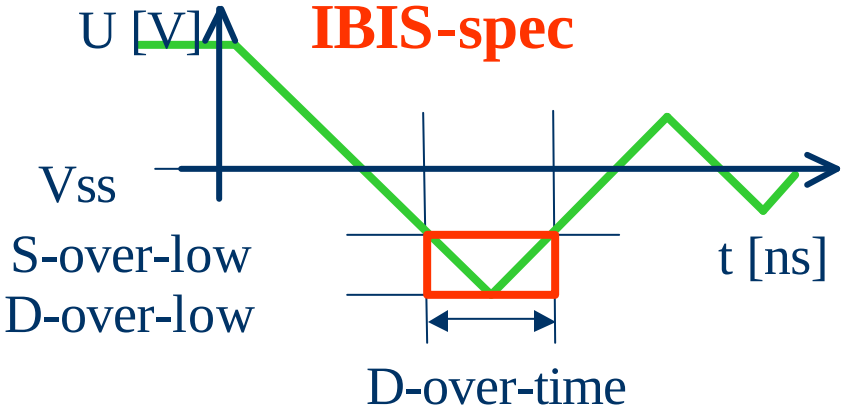

Use dc. cond. for static-over and max. rat. for dynamic-over values

Schmitt-Trigger

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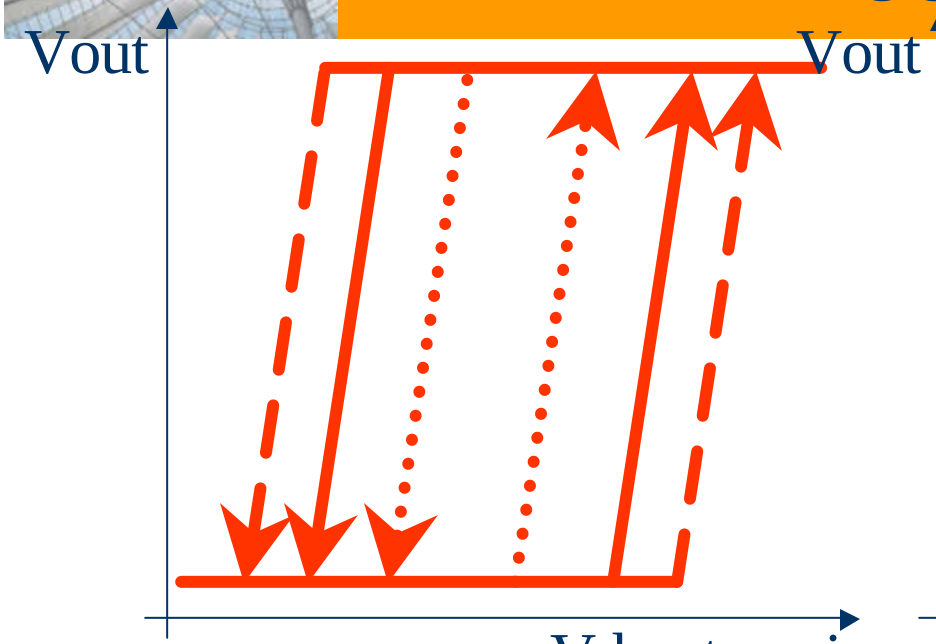

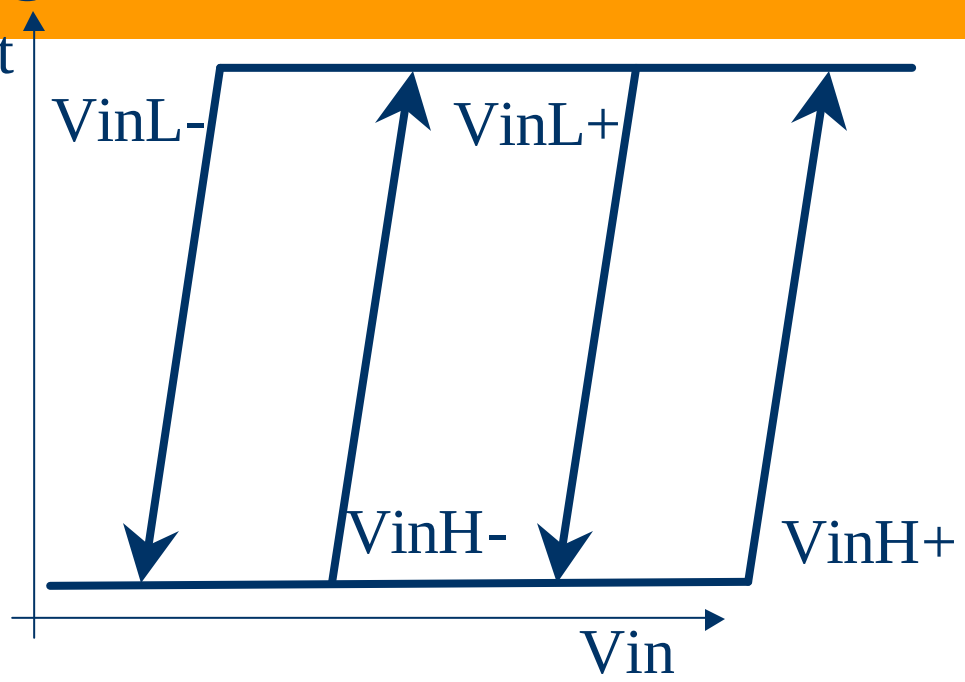

	Min		Max
Negative trigger voltage	0.8	1.25	1.7
Positiv trigger voltage	1.3	1.85	2.4
Hysteresis voltage	0.2	0.6	1.0

Use values of trigger voltages, don‘t use hysteresis

Proposal and questions

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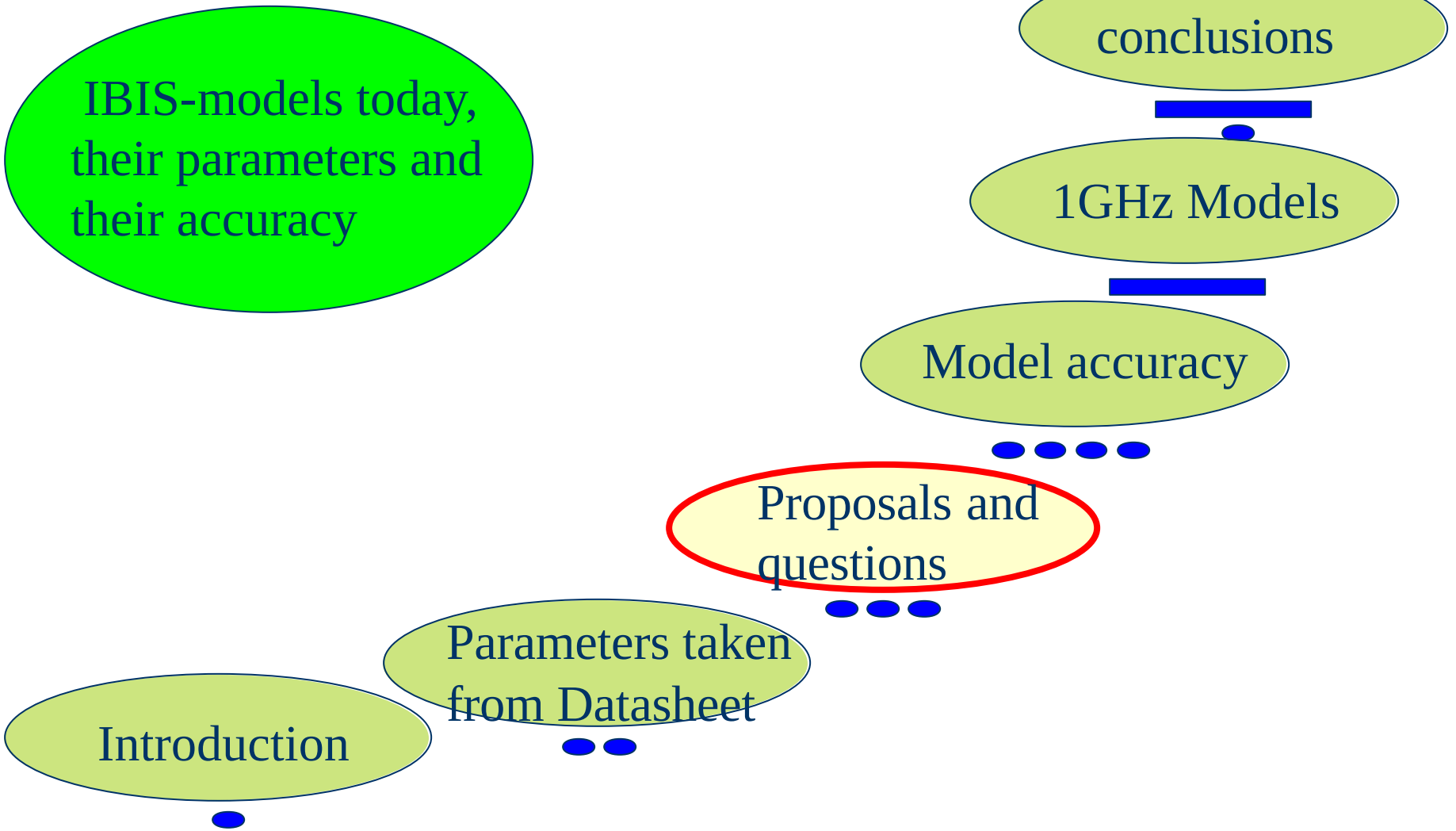

Differential model selector -1

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Schematic

Not all pins shown

Pinfile

Not all pins shown

1	Control	ALVC_REC-XXX-1_IN	1	Control	ALVC_REC-XXX-1_IN
2	Eclpos	PECL_REC-XXX-2_IN	2	ttl-in	TTL_REC-XXX-4_IN
3	Eclneg	PECL_REC-XXX-3_IN	3	Nc	NC
4	1A1	ALVC_IO-XXX-1_BI	4	1A1	ALVC_IO-XXX-1_BI
…..			…..		

```
[Diff Pin]  inv_pin  vdiff    tdelay_typ tdelay_min tdelay_max
 2           3       150mV    0ns        0ns        0ns       | for Ecl only
```

Differential model selector -2

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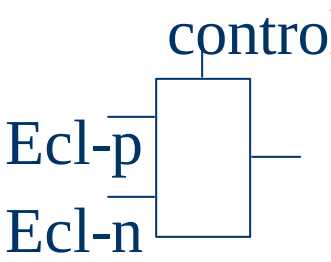
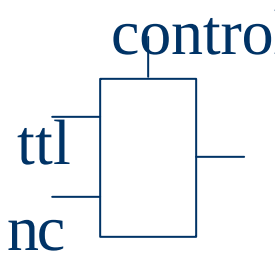
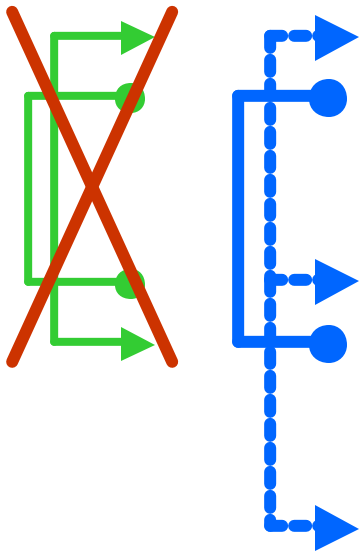
1	Control	ALVC_REC-XXX-1_IN
2	pos	YYYY_REC-XXX-5_IN
3	neg	ZZZZ_REC-XXX-6_IN
4	1A1	ALVC_IO-XXX-1_BI

…..







[Model Selector] YYYY_REC-XXX-5_IN
PECL_REC-XXX-2_IN
TTL_REC-XXX-4_IN

[Model Selector] ZZZZ_REC-XXX-6_IN
PECL_REC-XXX-3_IN
NC

[Diff Pin]
2 3 …..

Create two components (pinfiles)

Receiver with three ranges

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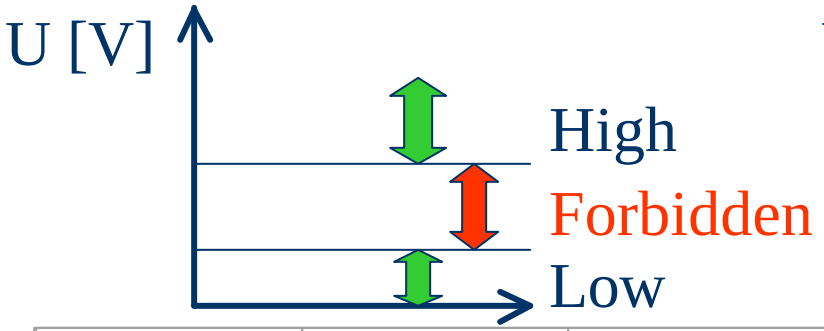
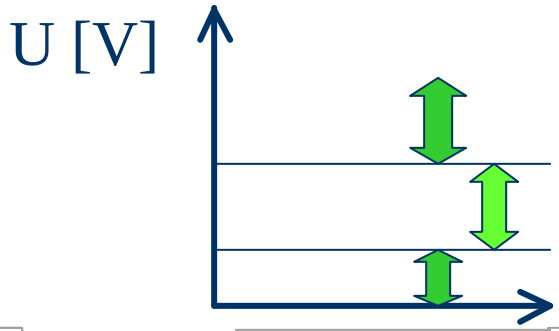


VinH	2.0V	Vcc+0.3 V
VinL	-0.3V	0.8V



Vin-range3	2.2V	Vcc + 0.3V
Vin-range2	1.0V	2.0V
Vin-range1	-0.3V	0.8V

What to do ?

A	VinL-12	-0.3V	0.8V
	VinH-12	1.0V	2.0V
B	VinL-13	-0.3V	0.8V
	VinH-13	2.2V	Vcc + 0.3V
C	VinL-23	1.0V	2.0V
	VinH-23	2.2V	Vcc + 0.3V

In IBIS-X
➔ if-then-else-loop

Input with series resistor

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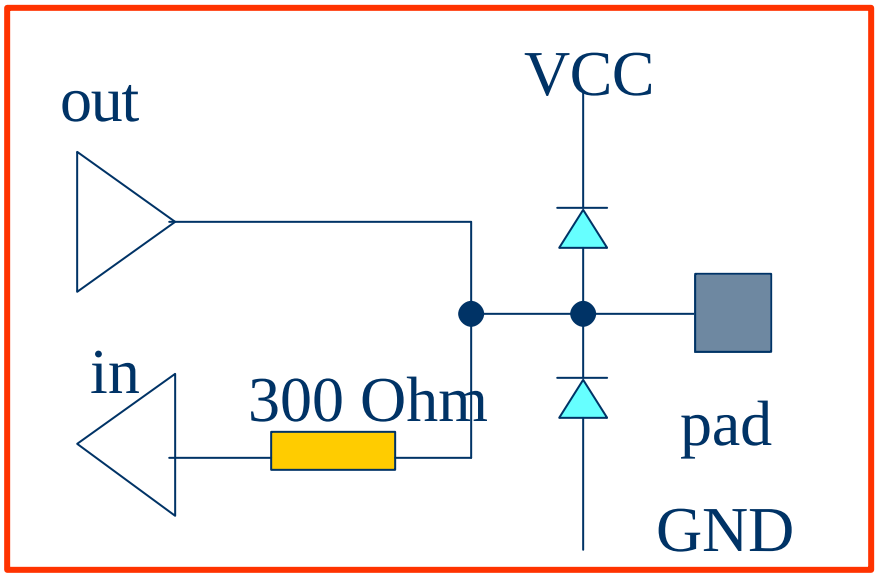
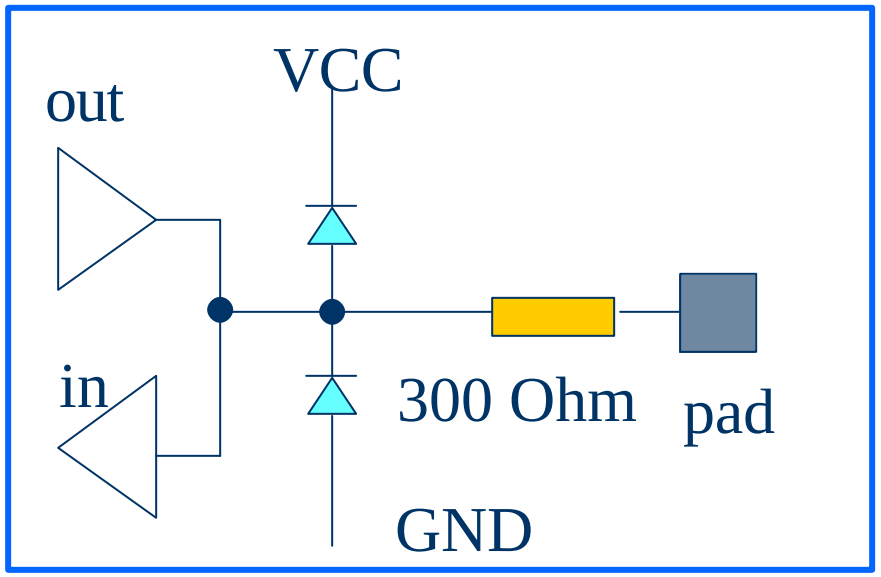
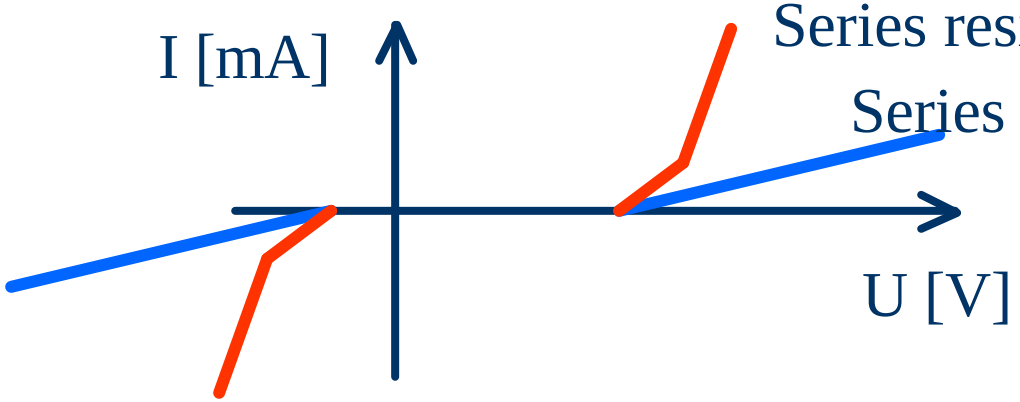




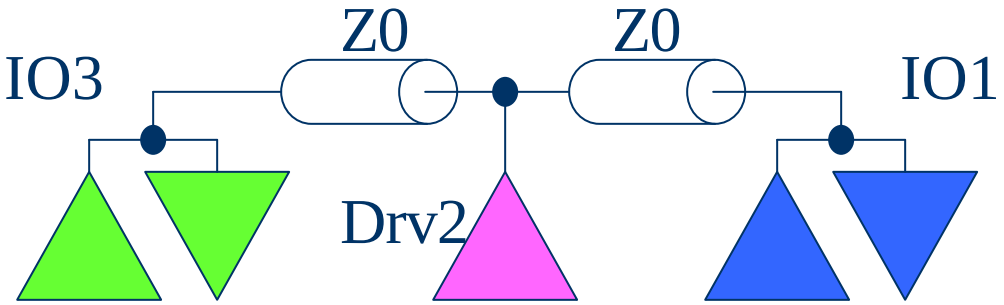


Series resistor not visible in clamp-curves

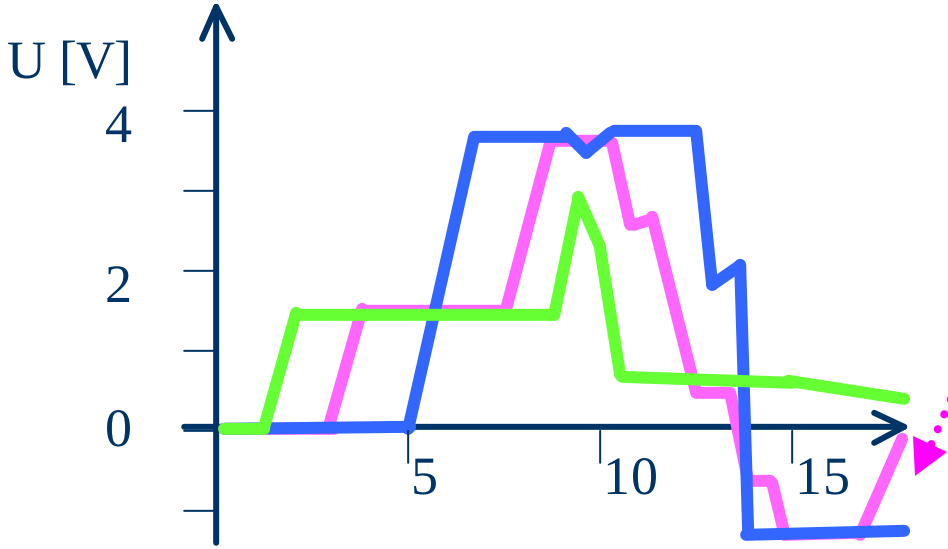
Series resistor visible in clamp-curves

Put in package-model !?!
Resistor needed at all ?

Over-undershoot for driver



IO3 driving
Drv2 3-state
IO1 receiving



Undershoot at Drv2

Over-Undershoot parameter needed also for drivers

What is an accurate model ?

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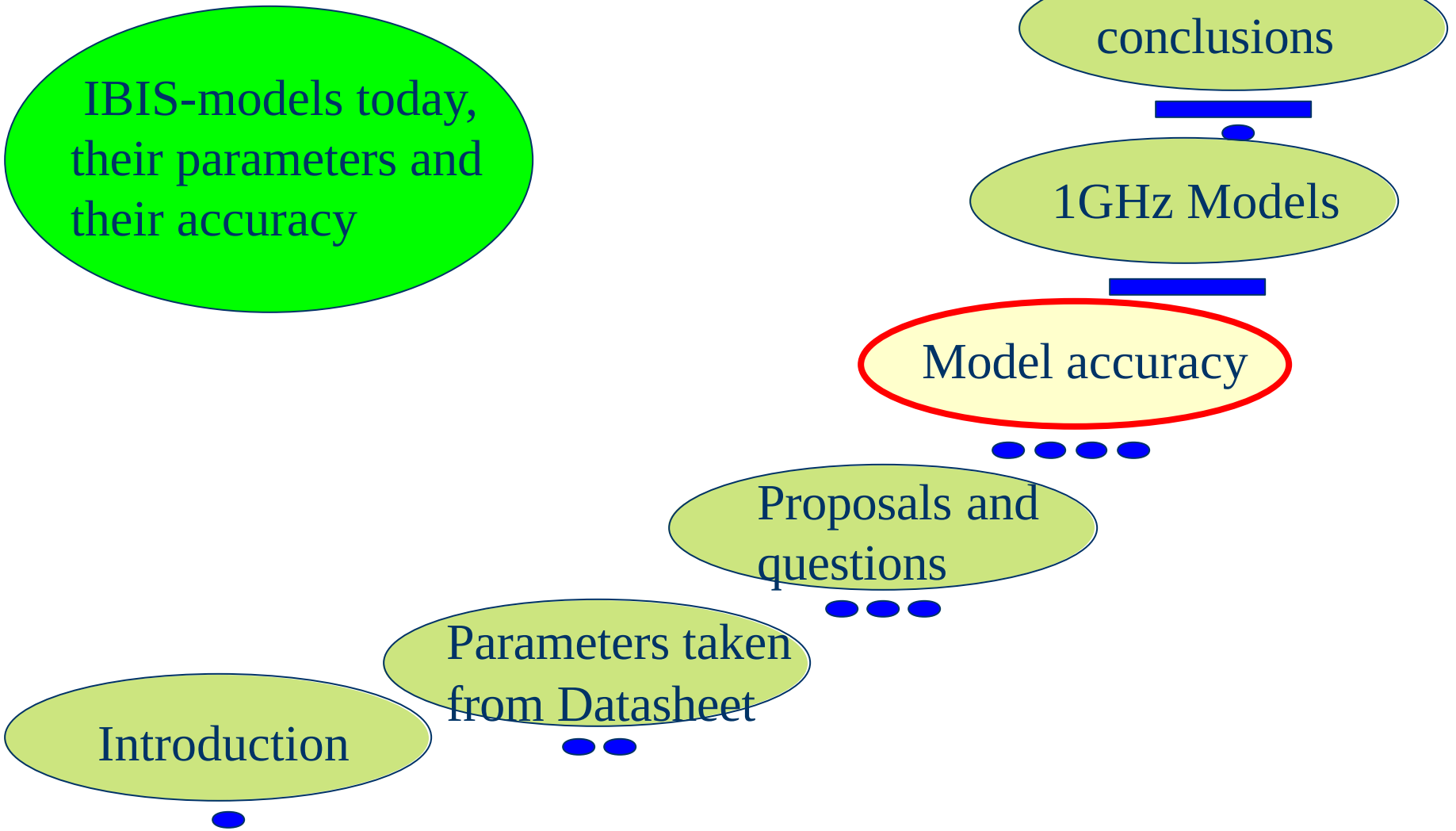
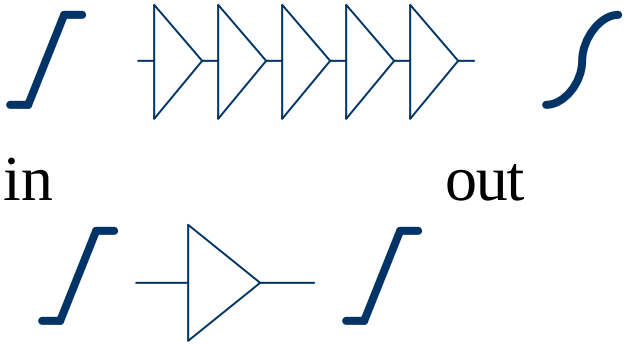
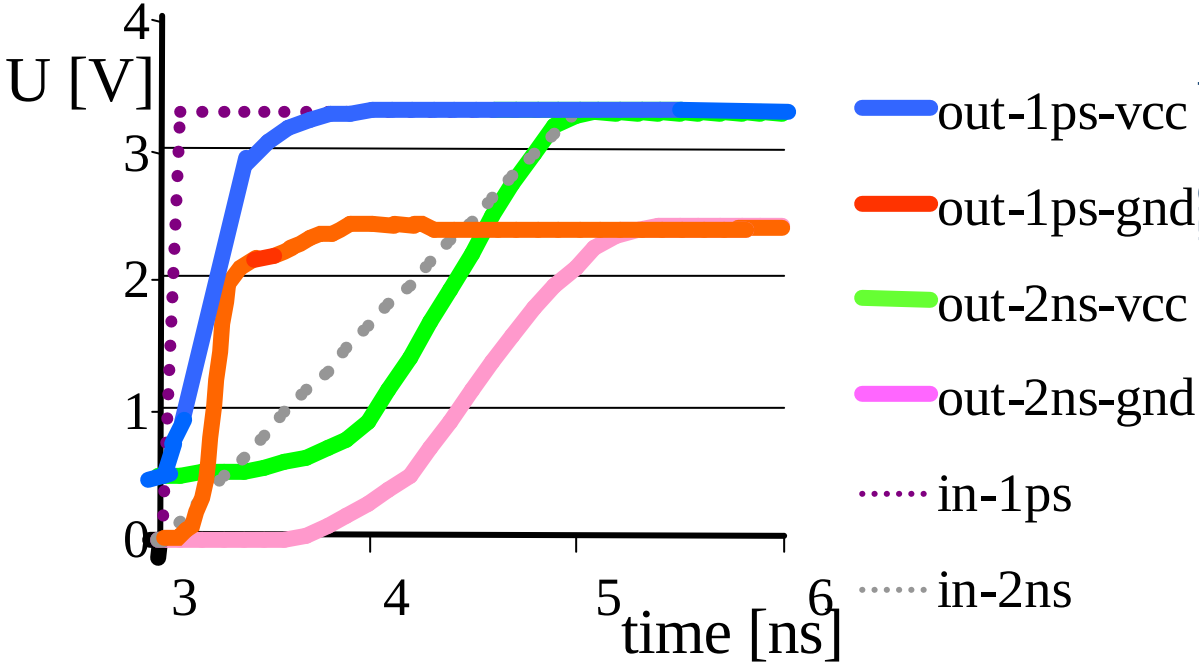


Stimulus form, number of stages

number of stages





Stimuli form

Use 5 or more stages and a stimulus of 1ps

Starting points of waveform

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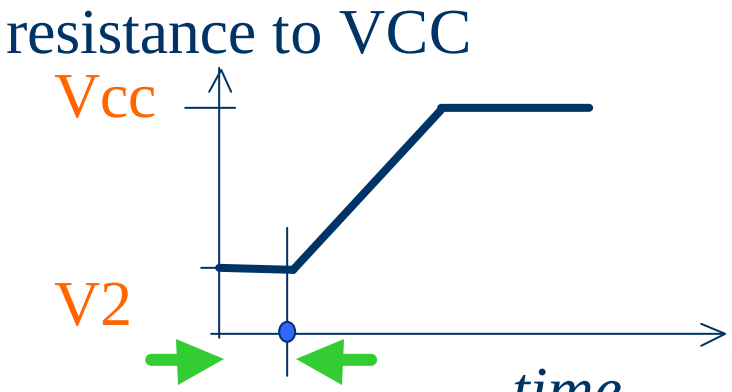

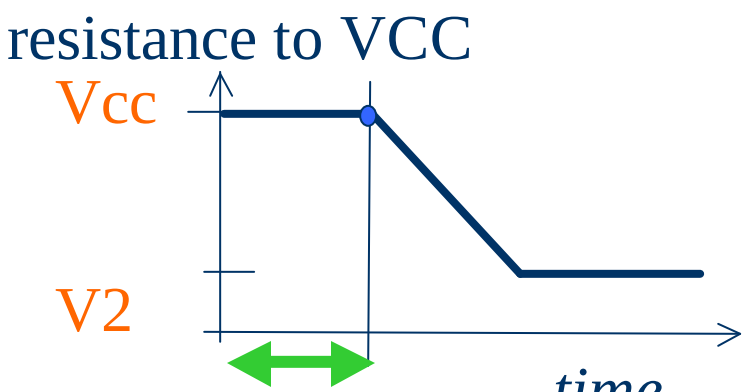

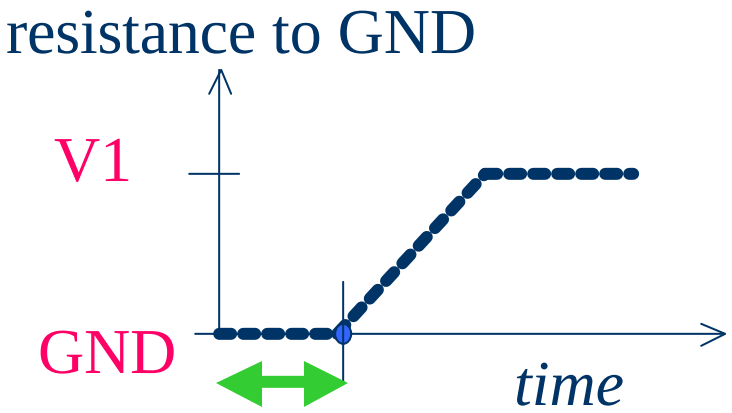

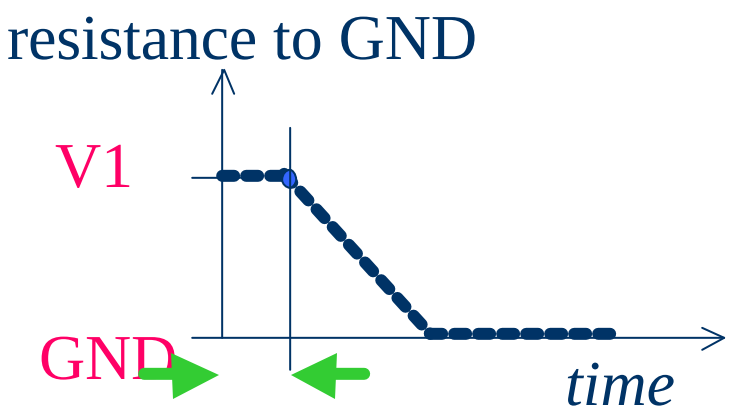

"Lead-in-time" (described in ibis-4); how much is allowed ?

Conditions for min-typ-max models

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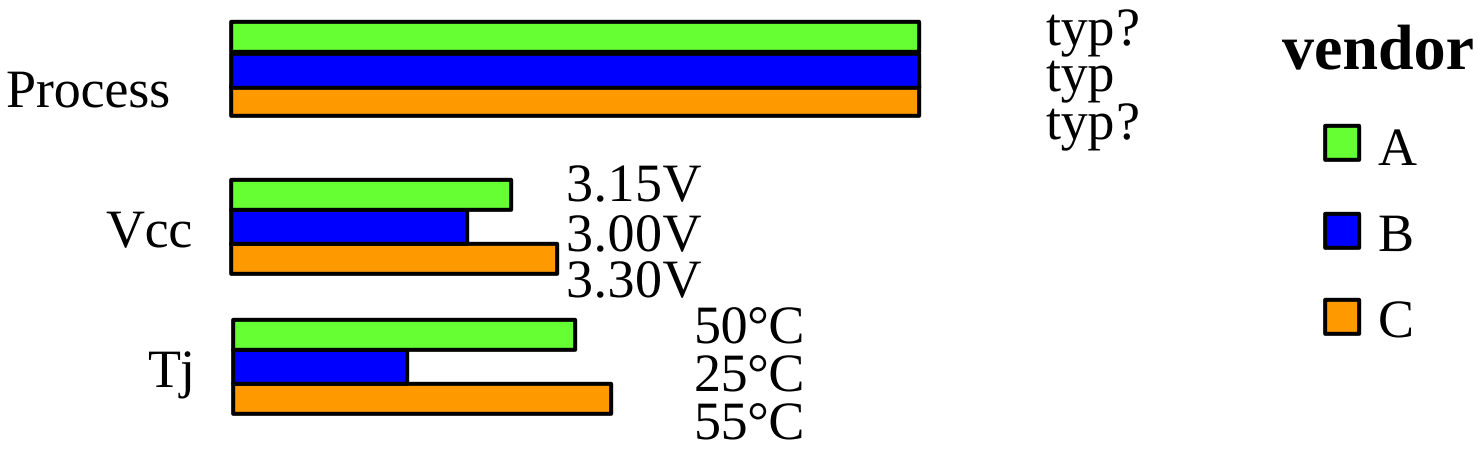
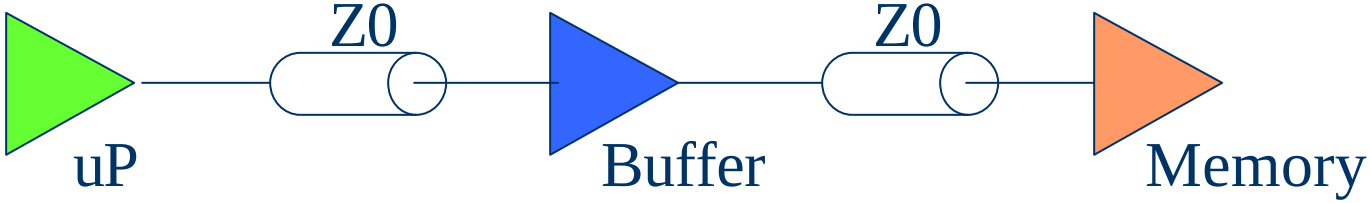
Example : typical model parameters from 3 vendors





How to make a reasonable simulation ?

Timestep for waveforms

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[Ramp]
dV/dt_r 1.14V/0.30ns
R_load = 50.00

[Rising Waveform]
R_fixture = 50.00
V_fixture = 0.000
....

0.40nS	1.58mV
0.60nS	-5.84mV
0.80nS	0.0834V
1.00nS	0.76V
1.20nS	1.51V
1.40nS	1.76V

....

different timestep for simulation and printing

smaller value of dt_r or dt_f

Timestep for printing should be

$$\frac{dt\_r}{10}$$

(= 30ps)

1 GHz Models

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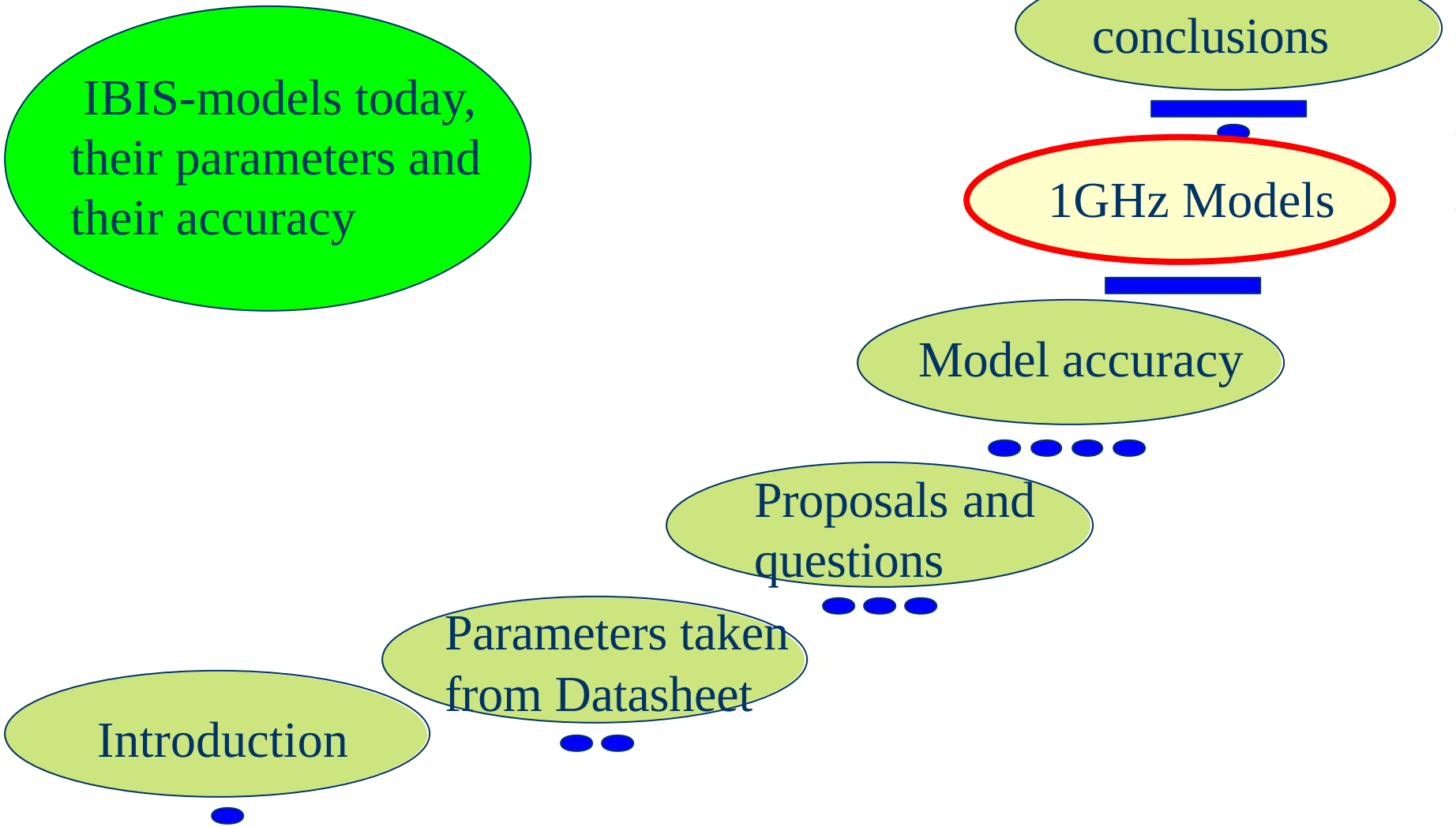

Definition

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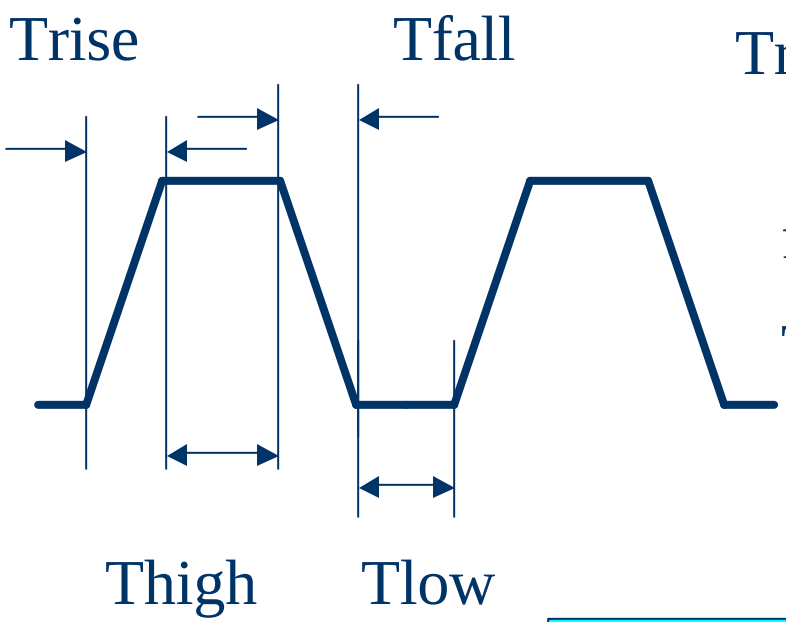


Trise = Tfall = Thigh = Tlow = Tperiod/4

f = 1 / Tperiod = 1 GHz

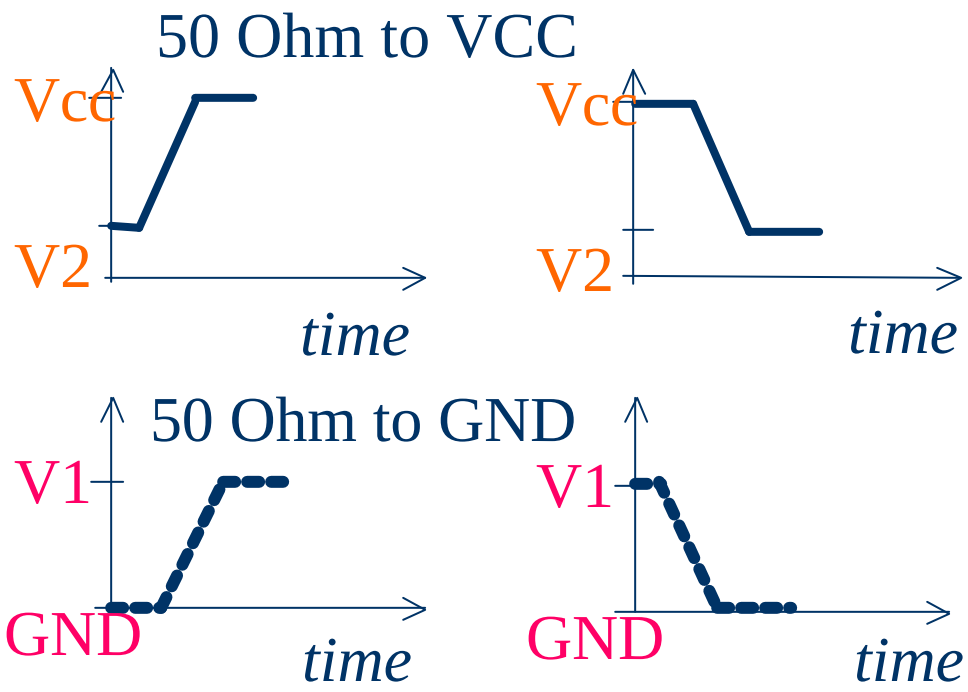
Trise = 250ps

We have to separate in

- IO-Model

- Package model

IO-model



V-t-waveforms :

Look the same for
1ns or 100ps

Models with rise-falltime of 250ps like LVDS, PECL and even CMOS show good results , but without package model

Package model -1

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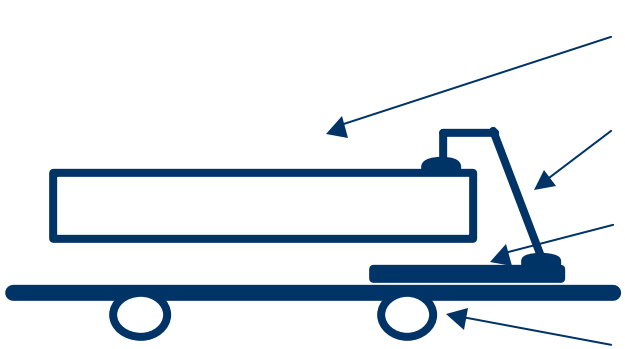
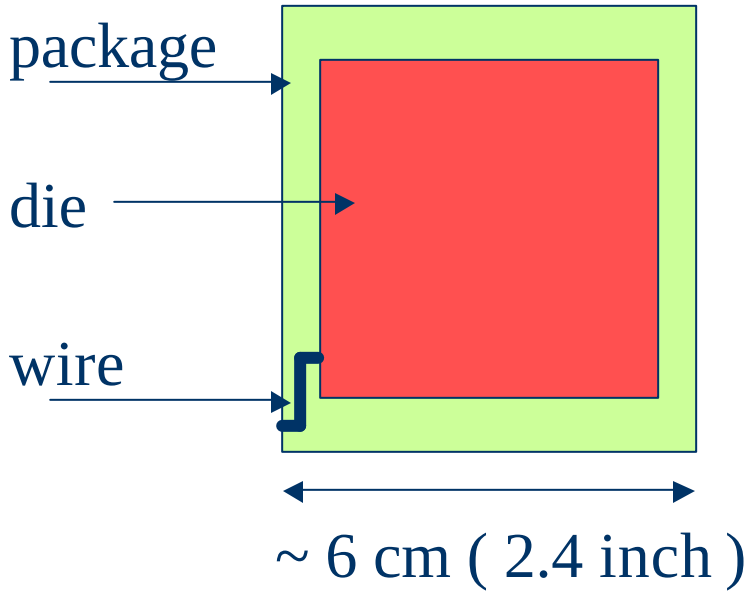
Schematic of BGA-Package





EPBGA with 1600 pins
wire length up to 2.5 cm (1 inch)

Package model -2

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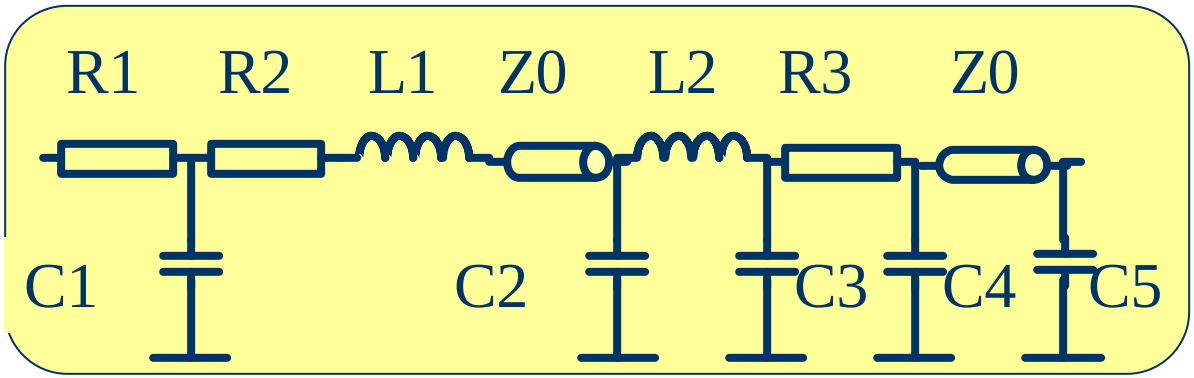
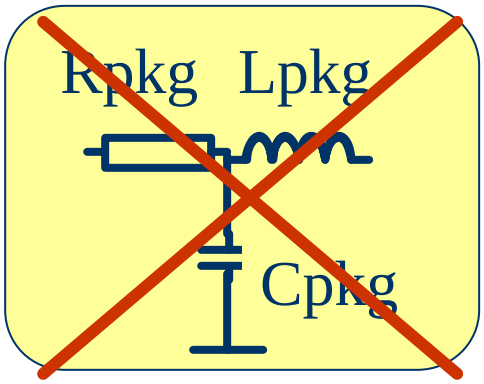
Correlation between package parameters and risetime

Crit. Line delay = Tr / 5	Risetime	Crit. Line length
Prop. Delay 5ns/m (1.52 ns/feet)	1 ns	4 cm (1.57 inch)
	250 ps	1 cm (0.39 inch)





Packages used with model rise-falltimes < 250ps must be modeled as (coupled) transmission lines

Conclusions

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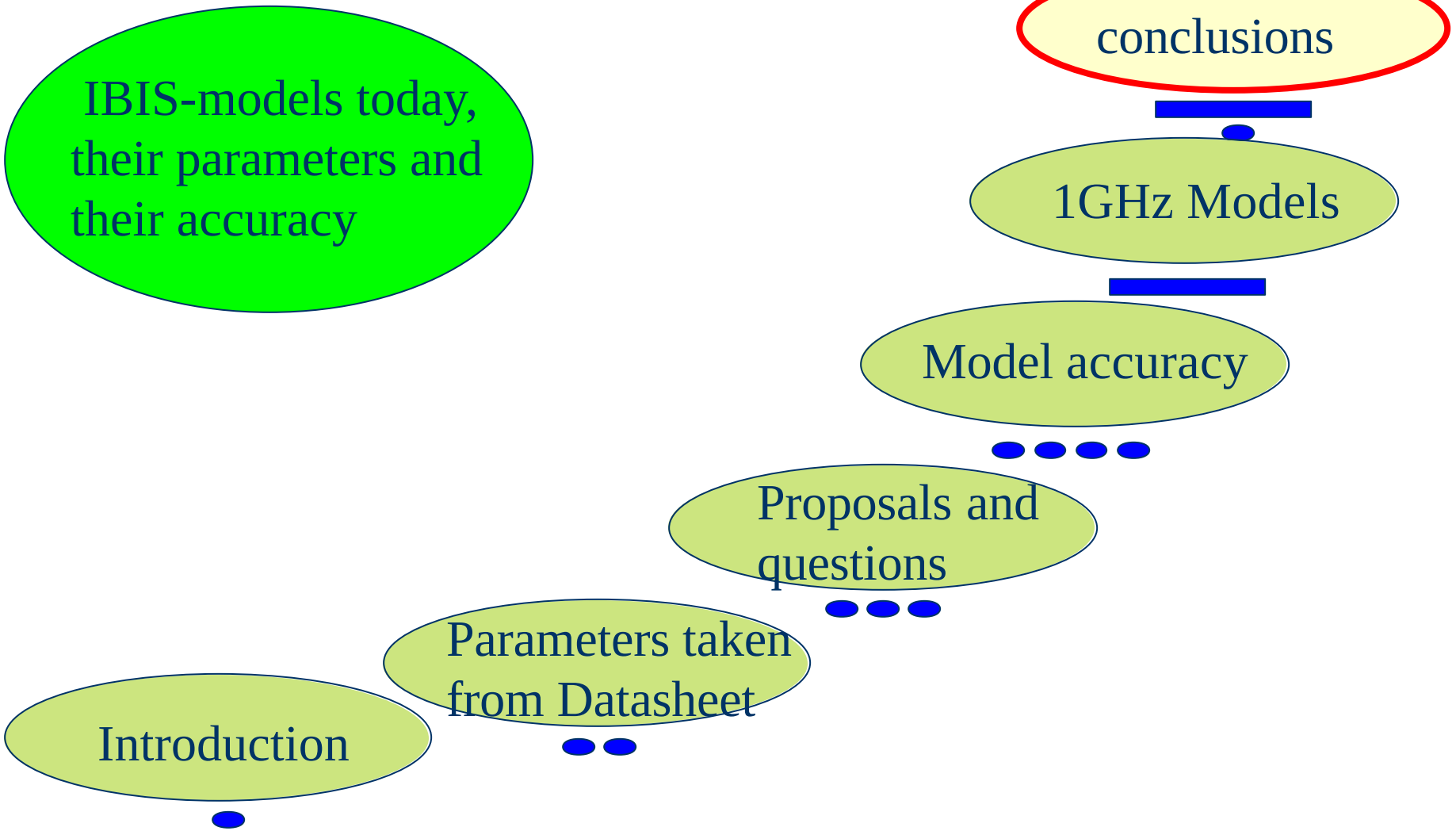

Summary

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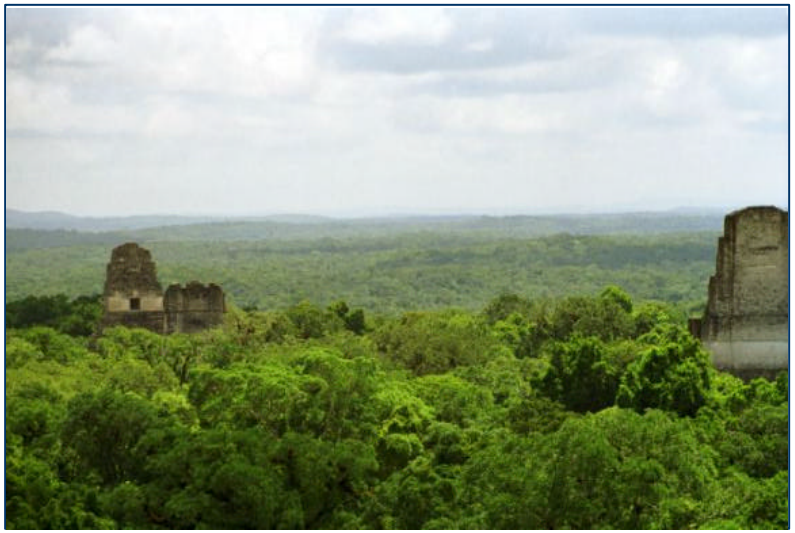
- many missing parameters can be taken out of the datasheet
- IBIS-X and/or IBIS-4 could help
- clarify the conditions how to create a model
- IBIS models work well up to 1GHz

It‘s getting clearer

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