Multi-Lingual Modeling Applications and Issues

Bob Ross
June 13, 2002

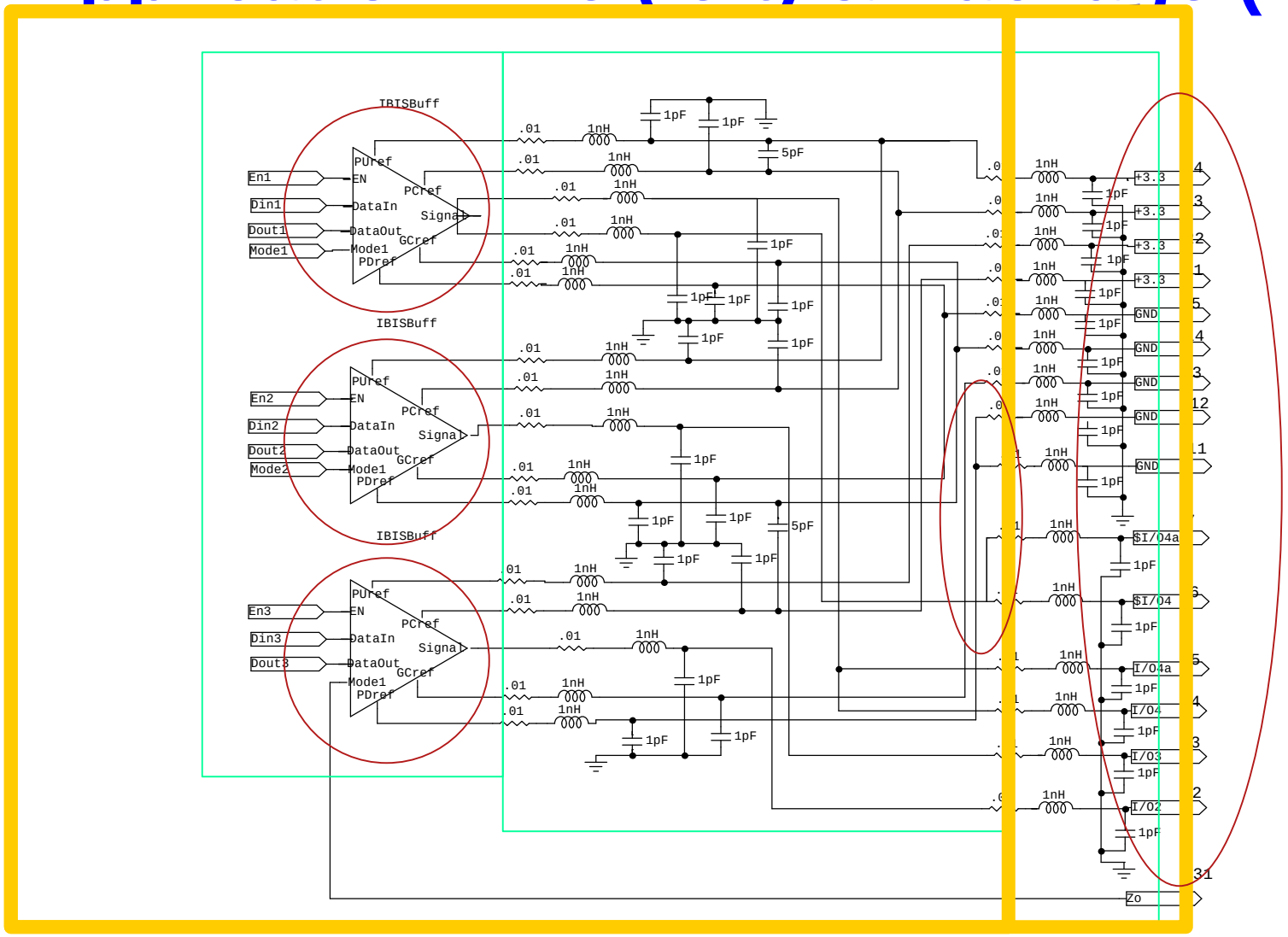
IBIS Summit Meeting
New Orleans, Louisiana

Mentor Graphics®

Benefits of Multi-Lingual Support

- Model advances beyond IBIS
  - True differential buffers, current buffers
  - SCSI driver/terminator advances
  - More detailed over-clocked buffer detail
  - SSO effects and gate modulation
  - Code based modeling
- Die interconnect advances
  - Die interconnect and complex package modeling
  - External voltage rail, power integrity interactions
  - External buffer strength control
- Closer digital and analog analysis (AMS)

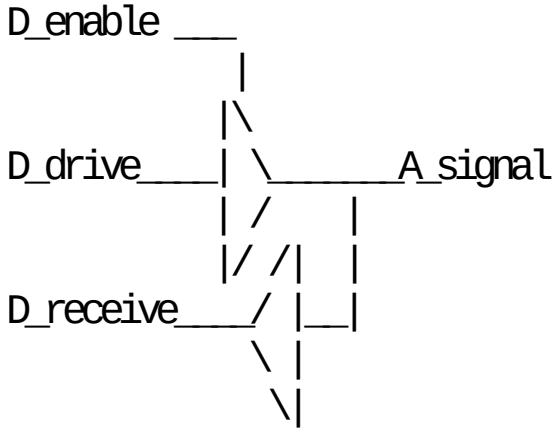
Application: Die (left) & Package (right)

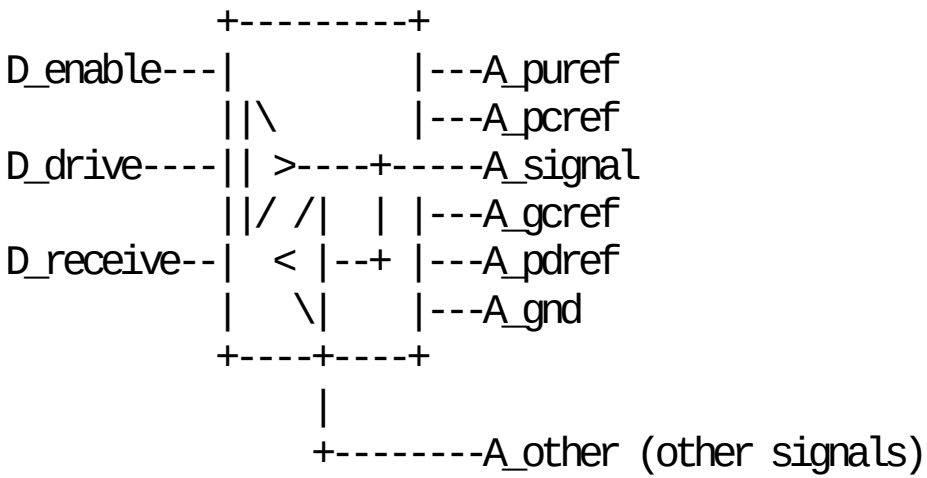


Why/How Multi-Lingual Modeling?

- **Leverages existing IBIS, Spice, VHDL-AMS, Verilog-AMS**
  - **Still use IBIS where appropriate**
  - **Extension uses IBIS for Pinout, Pkg., Info. & Spec.**
  - **Executes external code files**
- **Multi-lingual EDA tools from many companies**
  - **Mentor, Cadence, Synopsys (Avanti), …**
- **Faster response to industry - IBIS & few keywords**
  - **[External Model]: Buffer level external models**
  - **[External Circuit]: Die circuitry**
  - **[Node Declarations], [Circuit Call]: Interconnects**

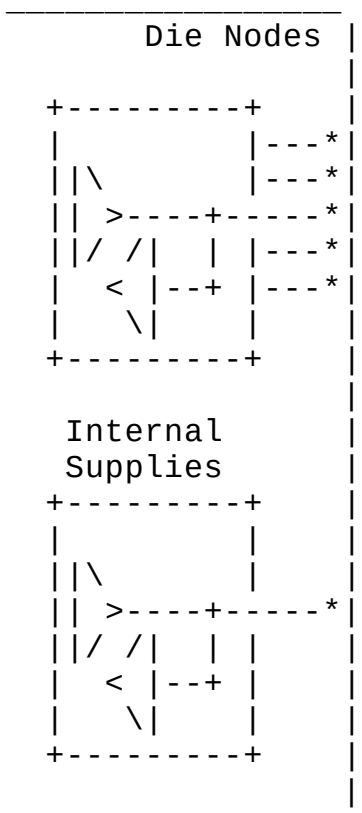
Digital (logic) and Analog Ports and Reference Models for I/O Buffers





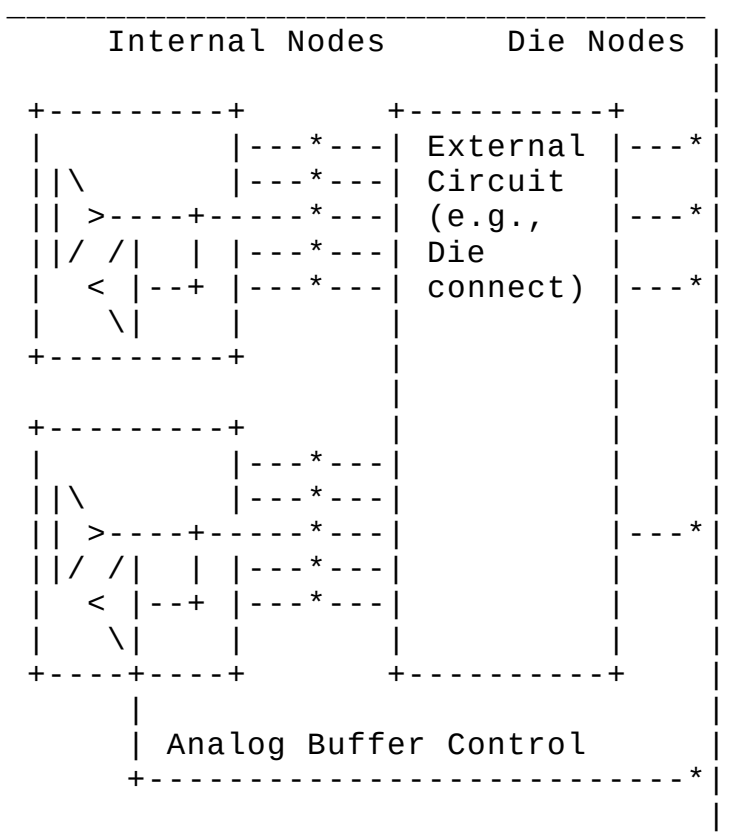
Reference Voltages:
A_puref, A_pcref, A_pdref, A_gcref, A_gnd

Existing IBIS or [External Model]s



- [External Model] under [Model] <model_name>
- [External Model]
  - Language <selection>
  - Corner <typ,min,max files and model names>
  - Ports <analog and digital port list>
  - D_to_A <digital signals to Spice ramps>
  - A_to_D <Spice thresholds to digital signals>
- Internal or external reference supplies
- Direct connection or interconnection syntax

Controlled Model & [External Circuit]



- [External Circuit] <circuit_name>
  - Language <selection>
  - Corner <typ, min, max files, names>
  - Ports <port list>
- [External Model] and [External Circuit] connected using internal and die nodes:
- [Node Declarations]
  - <internal node list>
- [Circuit Call] <model or circuit name>
  - Port_map <port to node mapping>
  - Cell_port <die node>

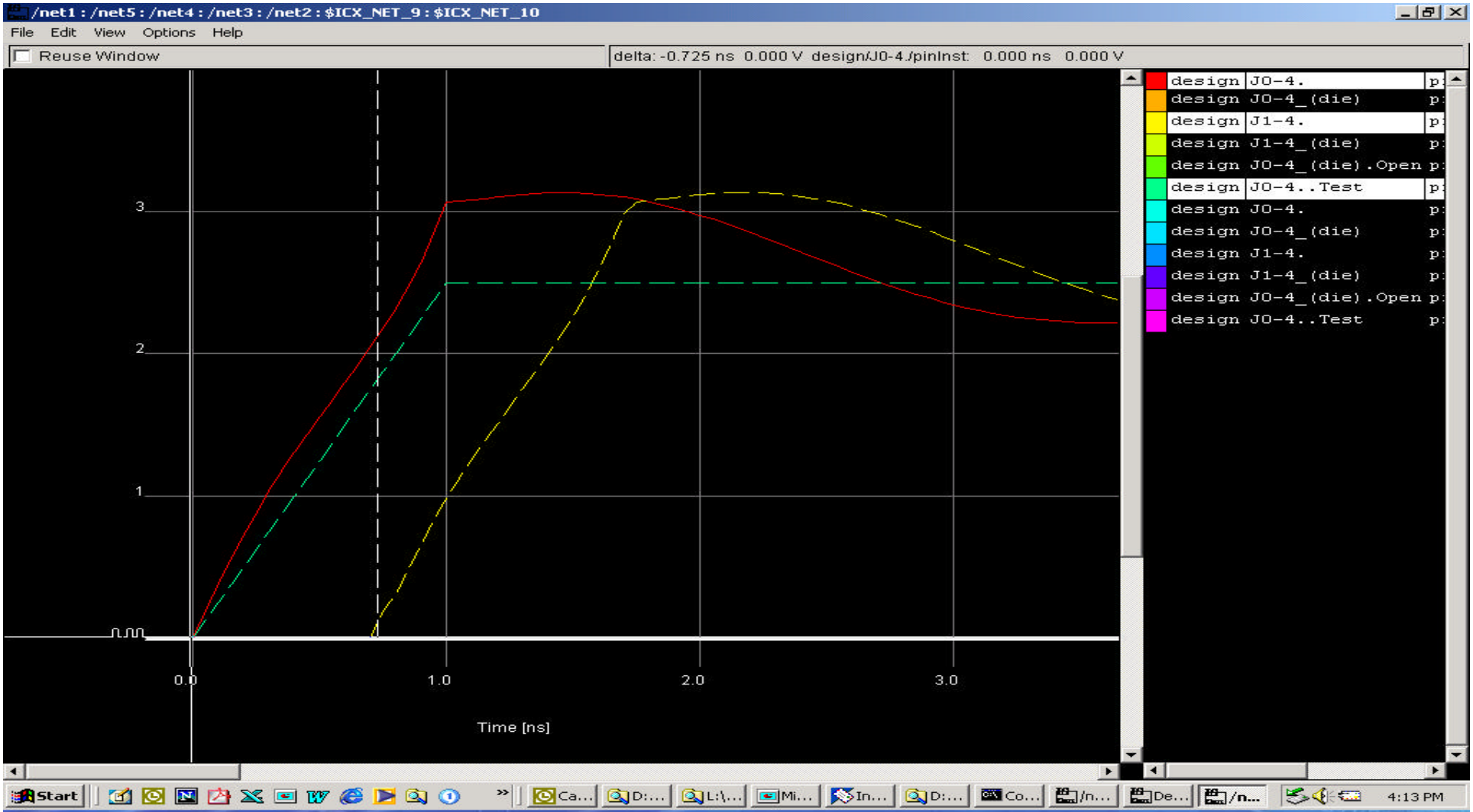
Proposal Includes More

- True and single-ended Differential buffers
- Series elements
- Predefined signal names support all combinations
  - IBIS [Model] to die nodes (existing standard)
  - IBIS [Model] through [External Circuit]
  - [External Model] to die nodes
  - [External Model] through [External Circuit]
  - [Circuit Call] required for last three cases, optional for first, but its usage overrides conflicting IBIS connections

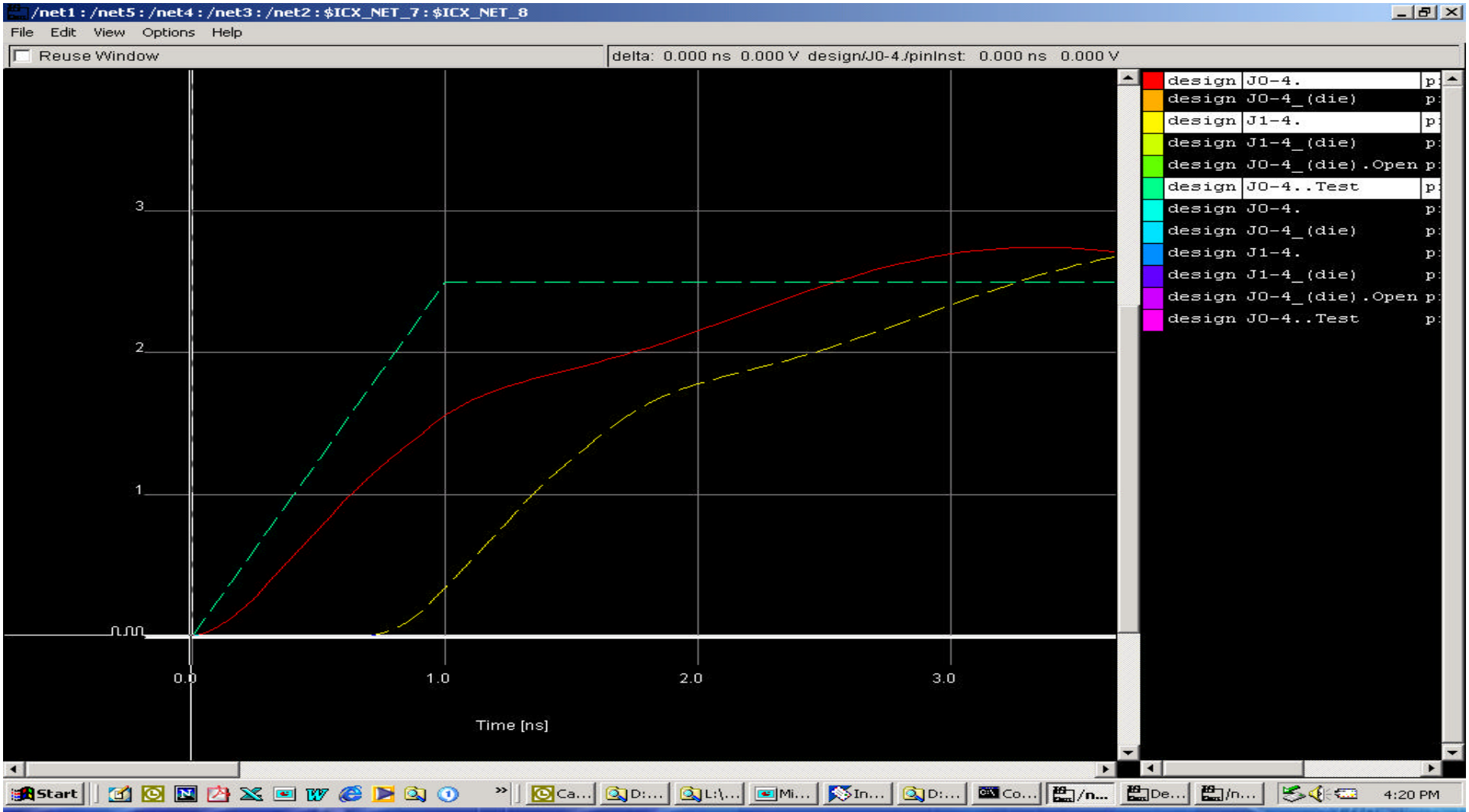
Two Examples

- **SSO Impact on Timing with Lossy Die Power Net**
  - **Opposite phase adjacent drivers: power burst, less delay**
  - **In phase adjacent drivers: power droop, more delay**
- **Integrated Circuit Electromagnetic Model (ICEM) from Europe**
  - **Core noise model for statistical currents drawn by internal clocks added to power nets for EMI current distributions**

Adjacent Drivers Out of Phase

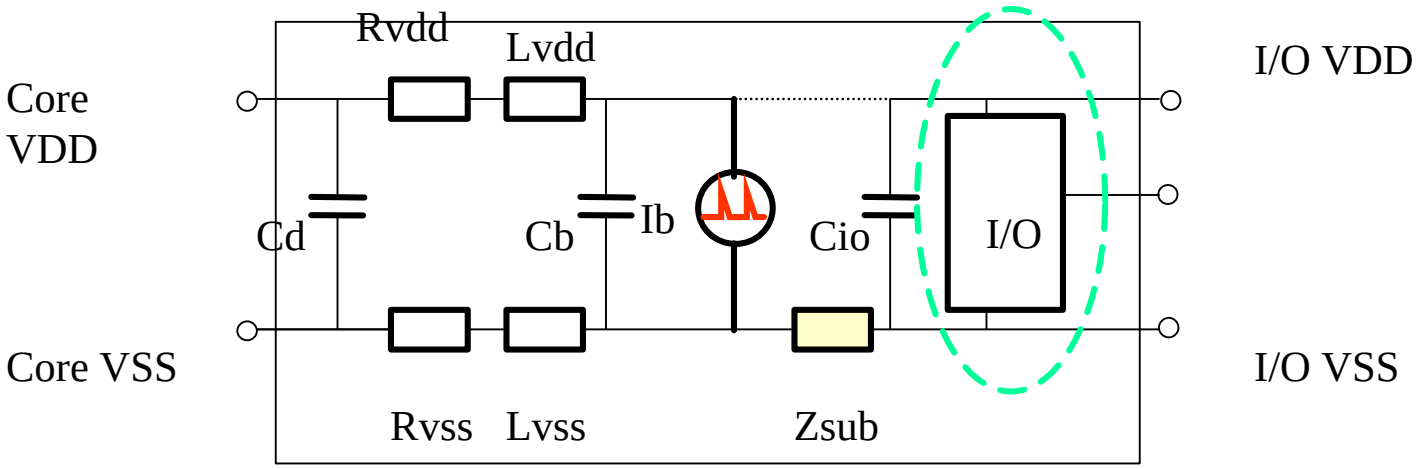


Adjacent Drivers In Phase



5. Emission Model with IOs

Add IBIS I/O data



Zsub: basically a 1-10W serial resistance

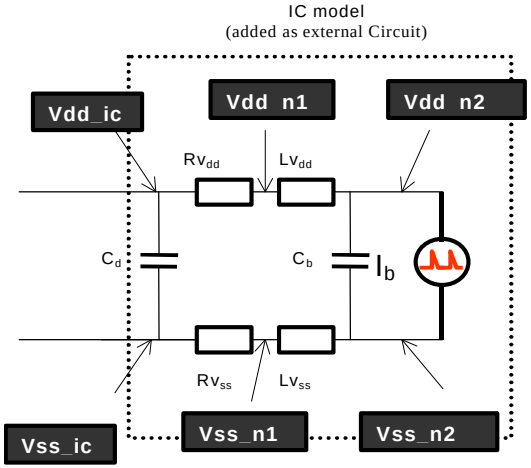
Cio : decoupling capacitance for IO supply

IO block: reuse of IBIS

Enclosure of ICEM in D60 IBIS file

```
[External Circuit]  ICEM
Language   Spice
| Corner      corner_name     file_name    circuit_name (.subckt name)
Corner        Typ             icem_d60.spi  icem_typ
Corner        Min             icem_d60.spi  icem_min
Corner        Max             icem_d60.spi  icem_max
|
| Ports are in same order as defined in Spice
Ports    vdd_ic vss_ic
|
[End External Circuit]
```

SPICE File "icem_d60.spi"




```
----------icem_d60.spi----------------
*
* Typical values for ICEM D60
*
.SUBCKT icem_typ vdd_ic vss_ic
RVDD Vdd_ic Vdd_n1 2
LVDD Vdd_n1 Vdd_n2 2.2n
Cd Vdd_ic Vss_ic 3.2n
Cb Vdd_n2 Vss_n2 50p
Ib Vdd_n2 Vss_n2 PULSE(0.01 0.4 10ns 1.0ns 1.0ns 0.01ns 31.25ns)
.ENDS icem_typ
-----------------------------------
```

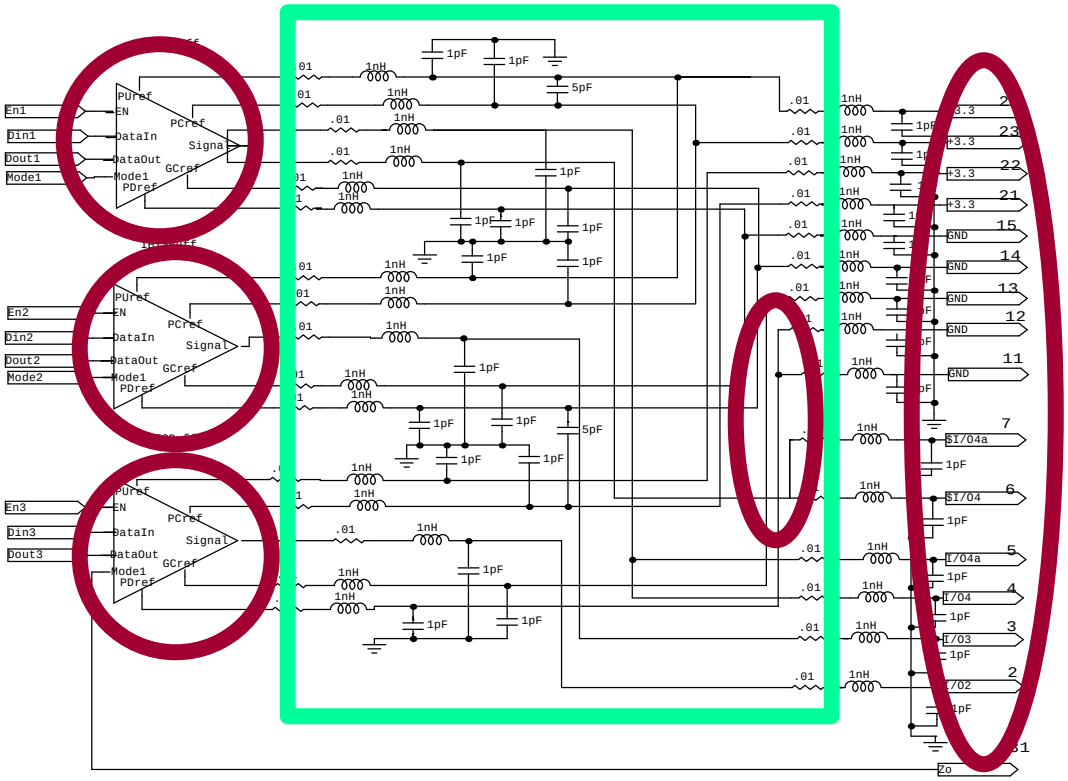
Some Issues and Discussions

- **Why [External Model] and [External Circuit]?**
  - **Several syntax differences**
- **Why [Node Declarations]?**
  - **Supports variable declarations in some languages**
- **Format of tables and names?**
  - **Up for review and discussion**
- **Cell_port usage**
  - **Associate displaced model to pins**
- **Interaction with other keywords**
  - **Rules can be made more exclusive**

Implementation/EDA Vendor Issues

- How to isolate nets of interest
  - Small set of dedicated models
  - Method of selecting nets of interest
- Control of stimulus
  - Through interconnection with other nets in analysis
  - Built in generators
  - Controlled in sync. with a model as an [External Model]

What's Next?



- **BIRD75.1 to describe details are now being reviewed**
- **Planned for vote and IBIS Version 4.1 release**