

IBIS Algorithms Revisited

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(Also presented June 5, 2003)



Previous Work

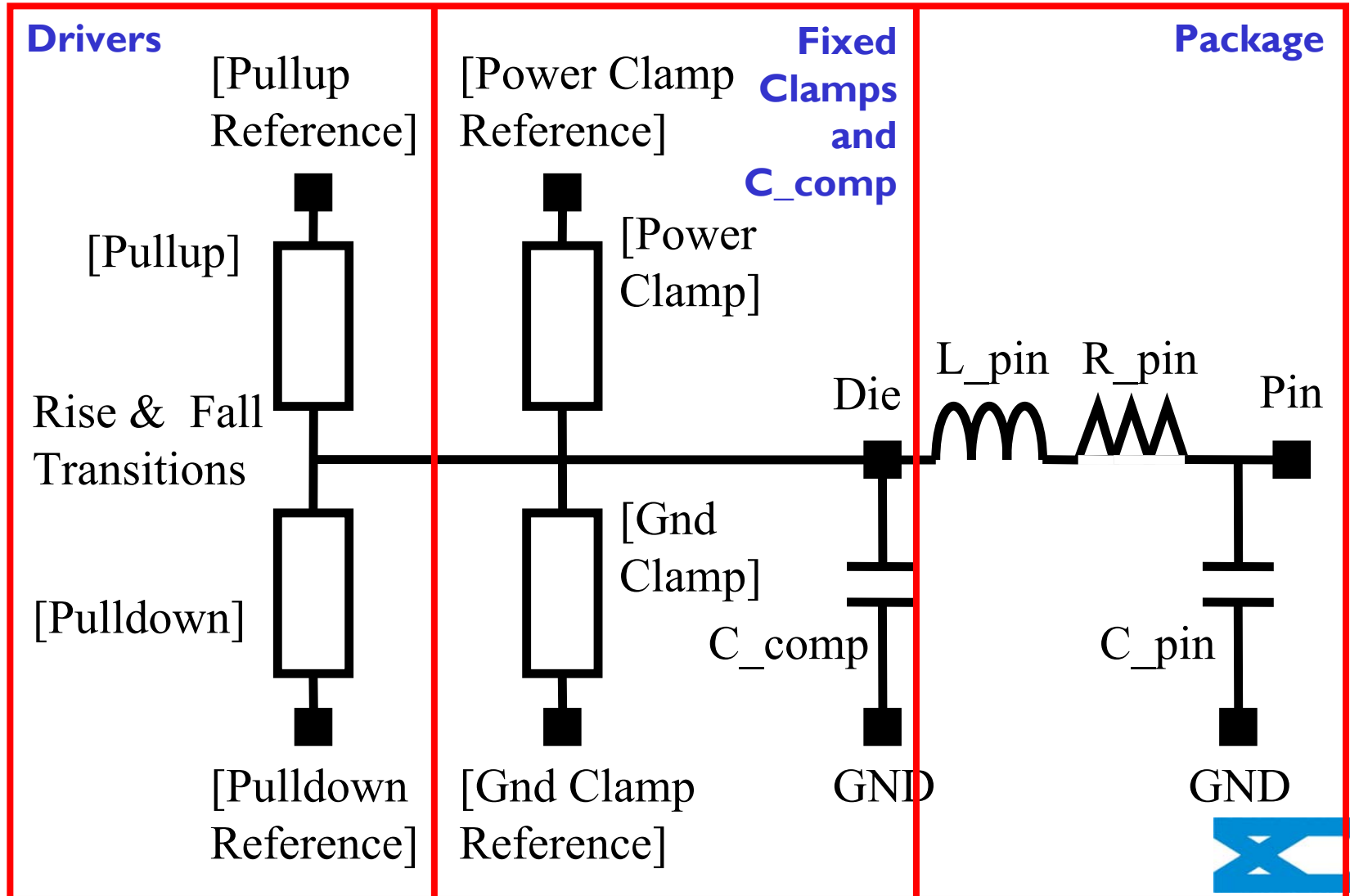
- Based on early prototype work
- Updated from hand-drawn foils given in June 1997 and presentation in Oct. 1998
- Presented at SPI 2003 in Siena, Italy



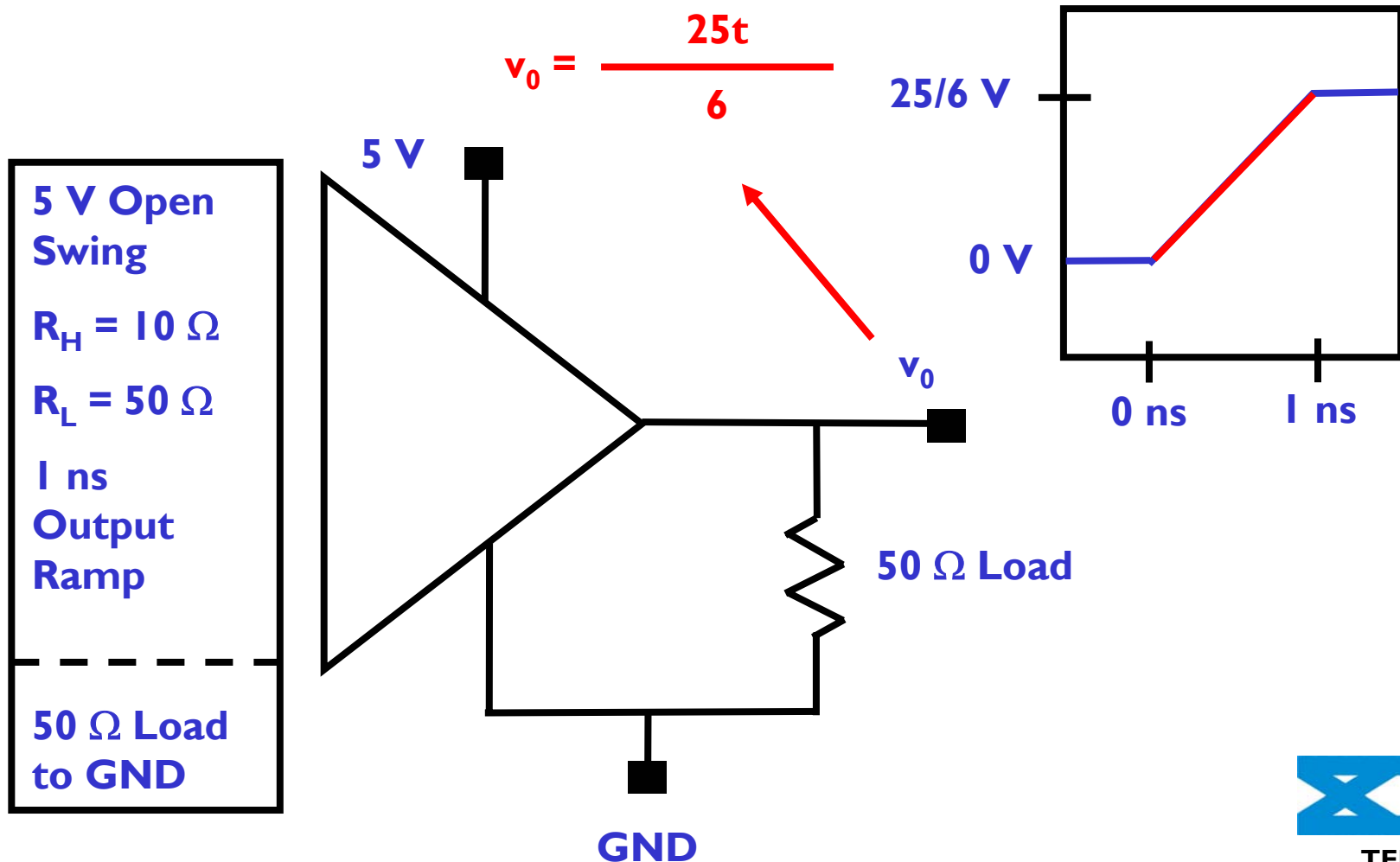
IBIS Algorithms

- IBIS data AND how processed
 - Older approaches give different solutions
 - Two-waveform algorithm gives good solutions
- Other algorithms
 - Multiple tables and dynamic interpolation
 - I/O Interface Model for Integrated Circuit (IMIC) for transistor multiple I-V and capacitance-V table interpolation
 - Radial based functions (RBF)

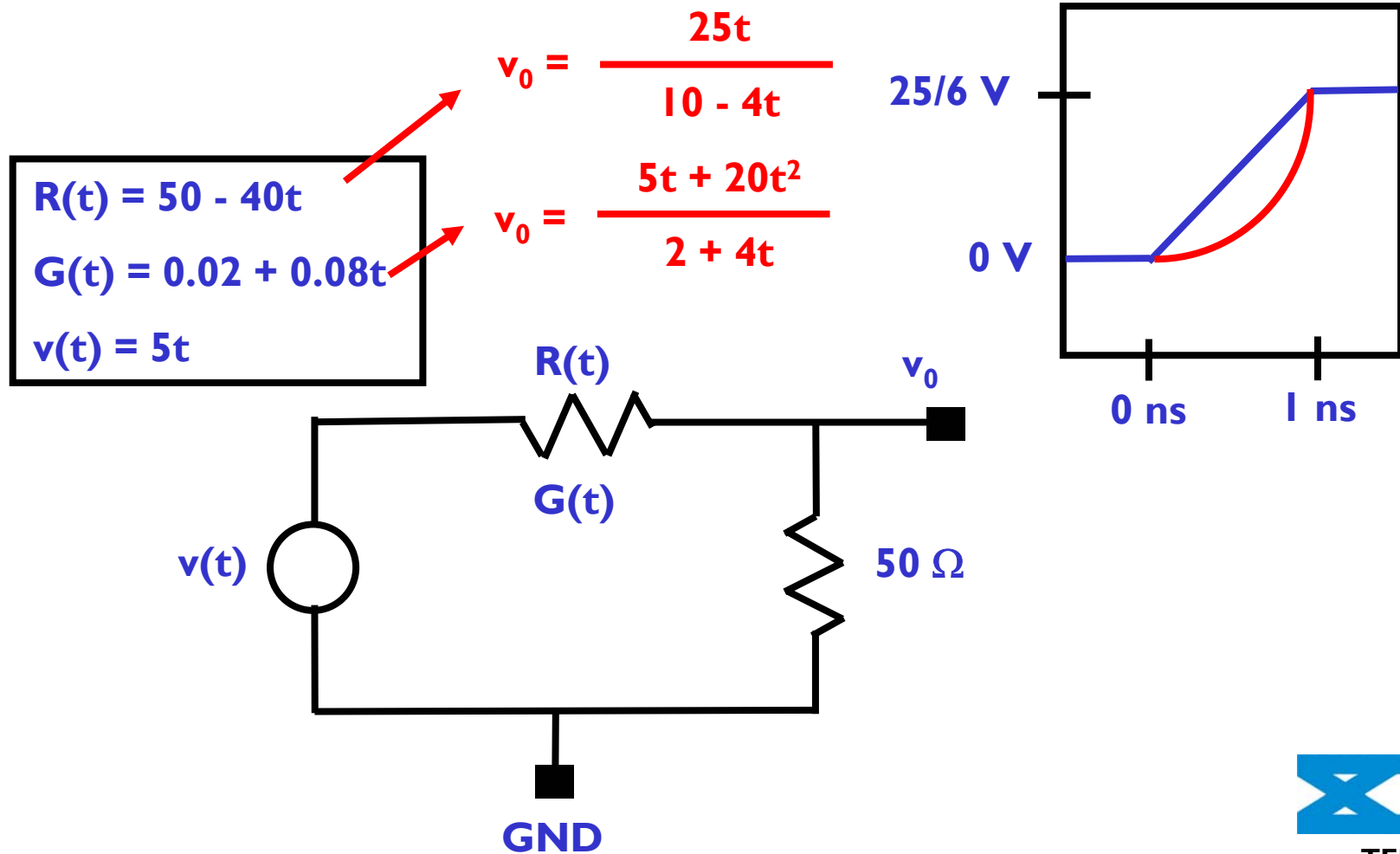
General IBIS Buffer Model



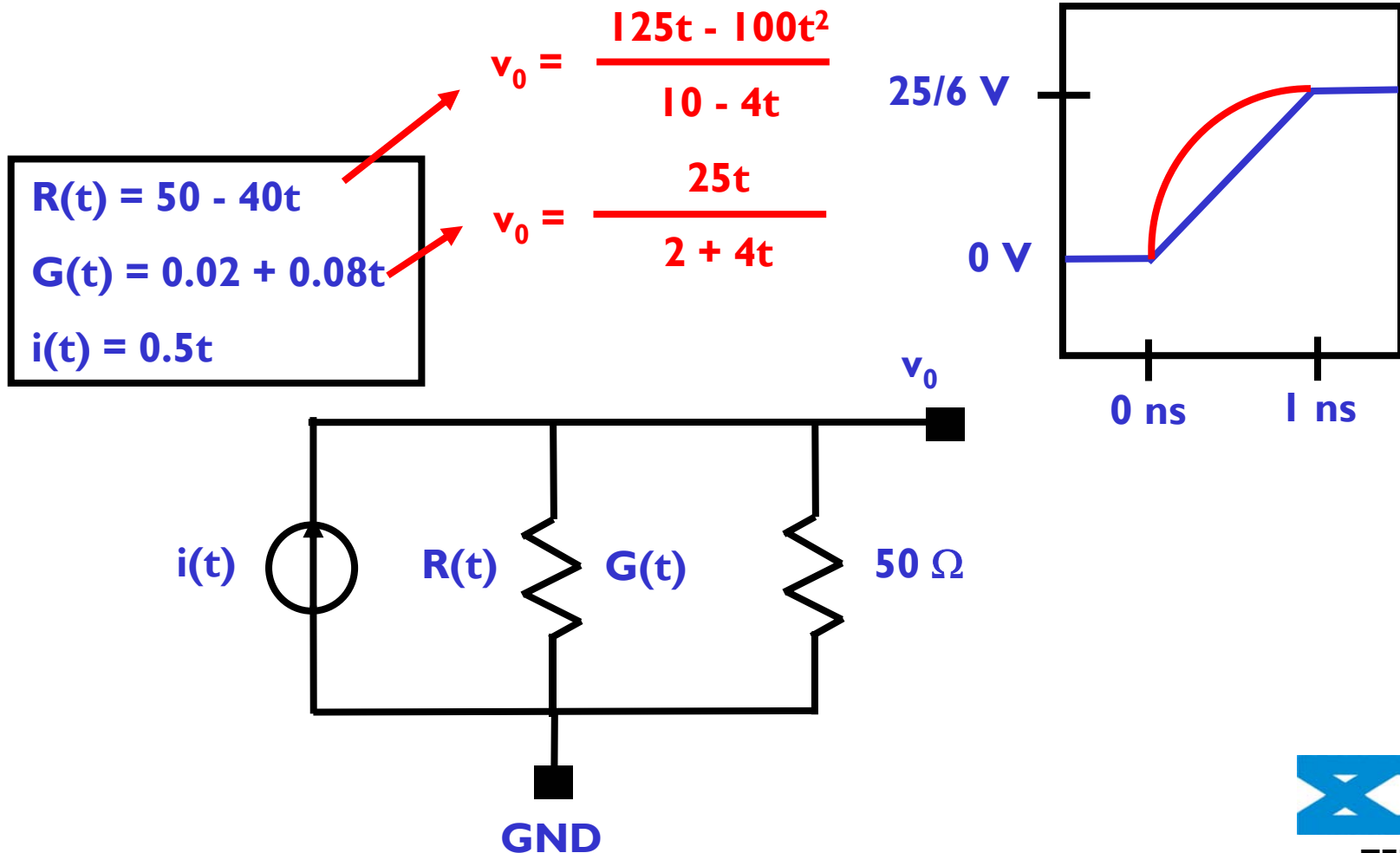
Example - Ideal CMOS Buffer



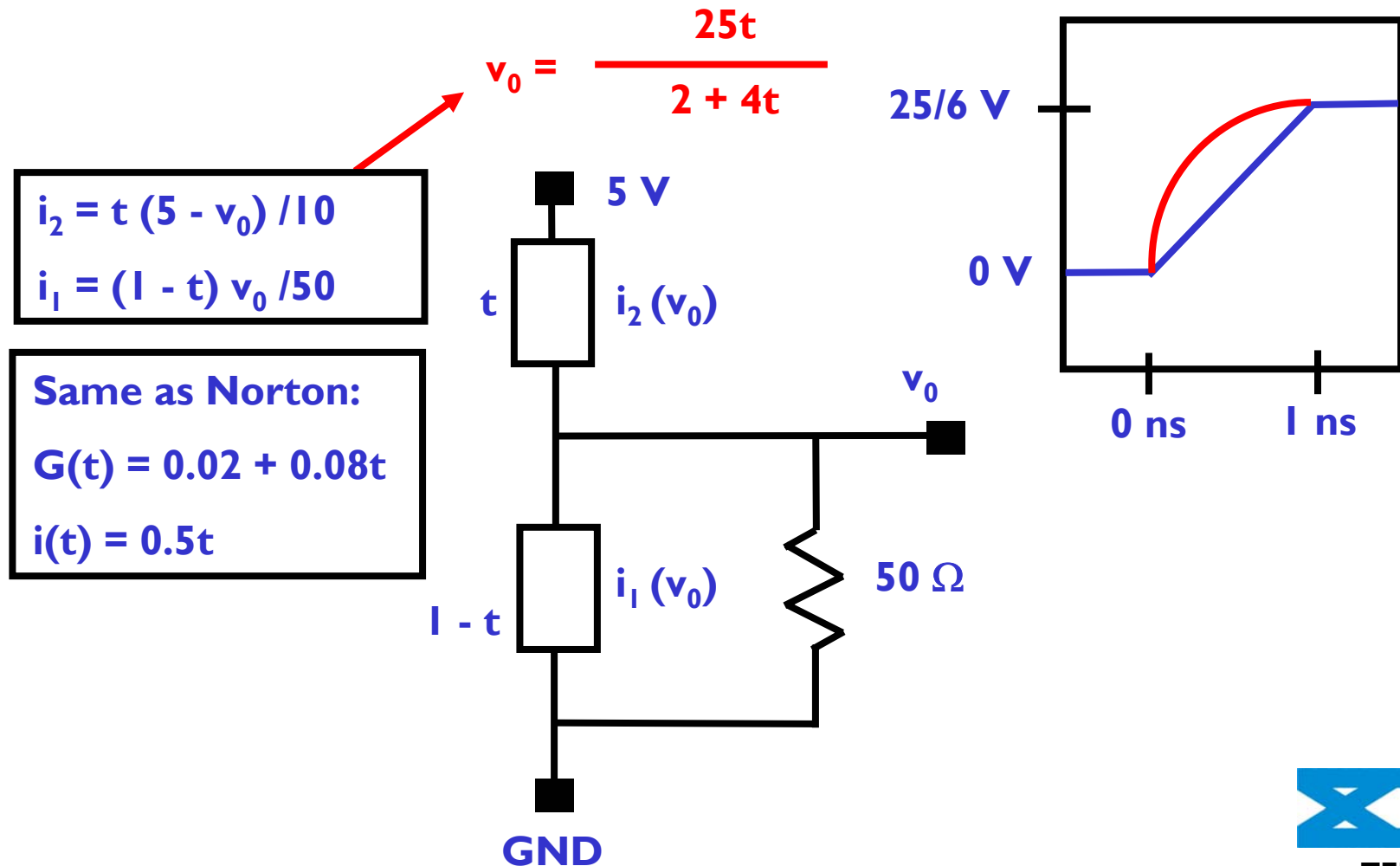
Thevenin Linear Z Transitions



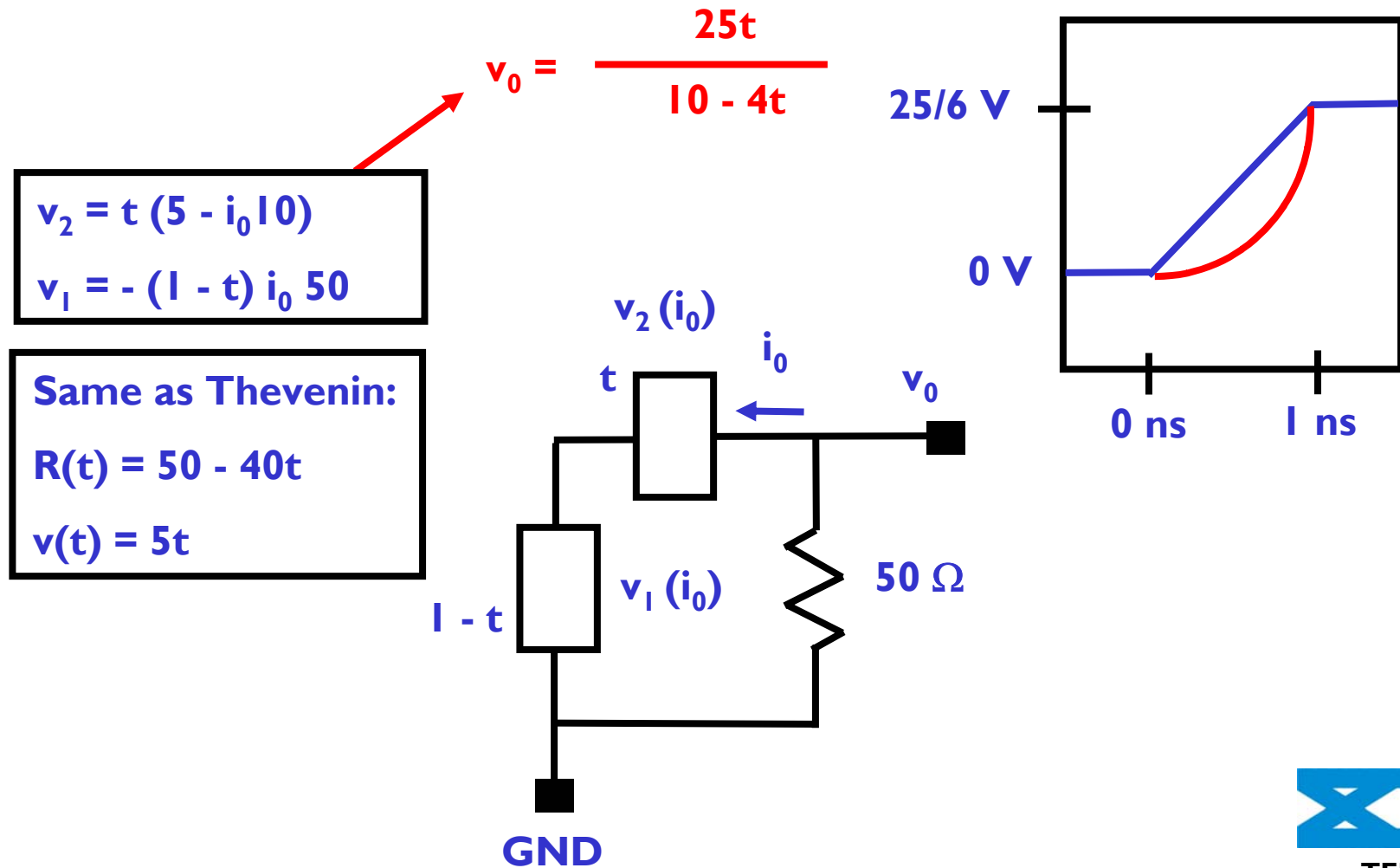
Norton Linear Y Transitions



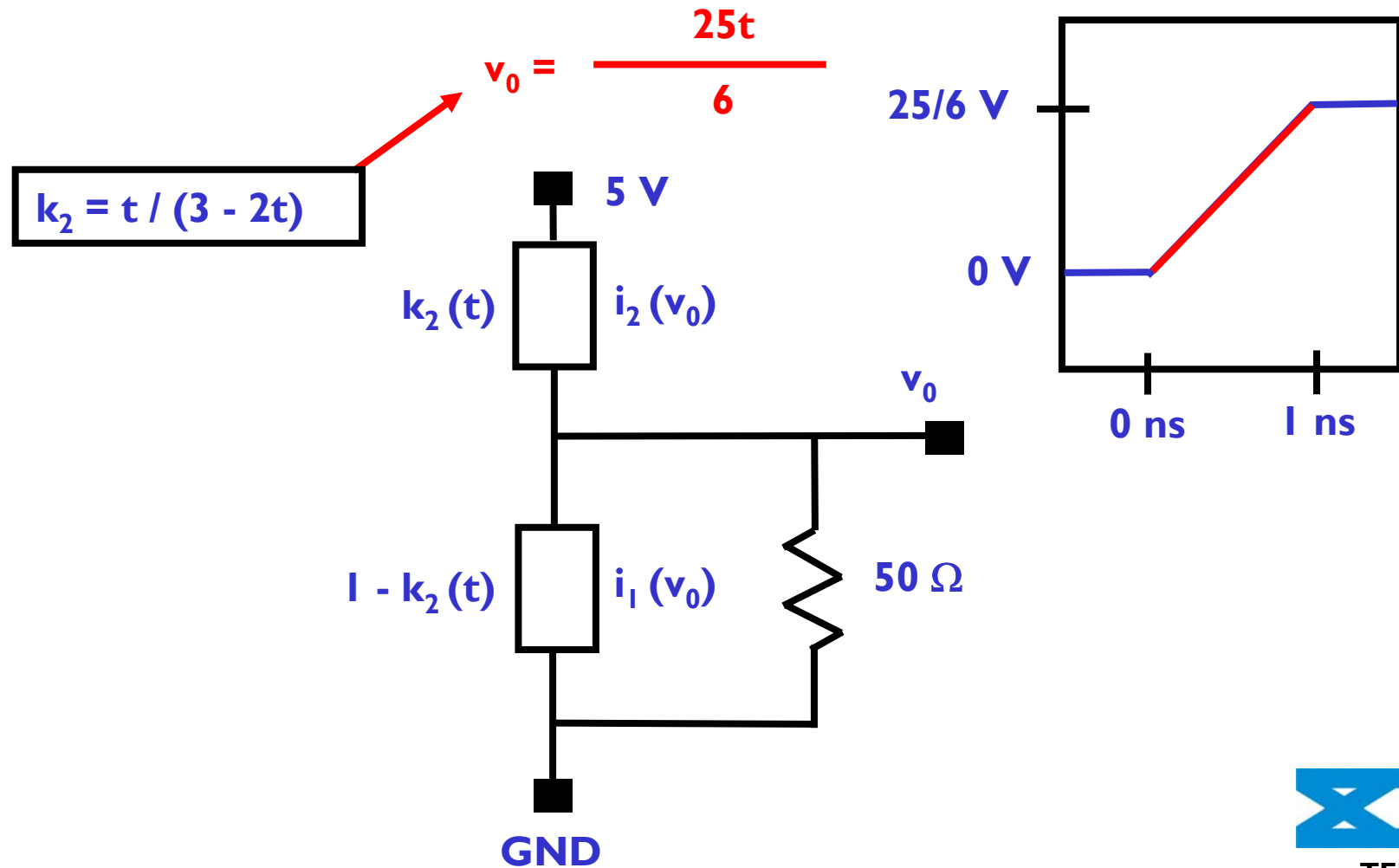
IBIS Linear Table Multipliers



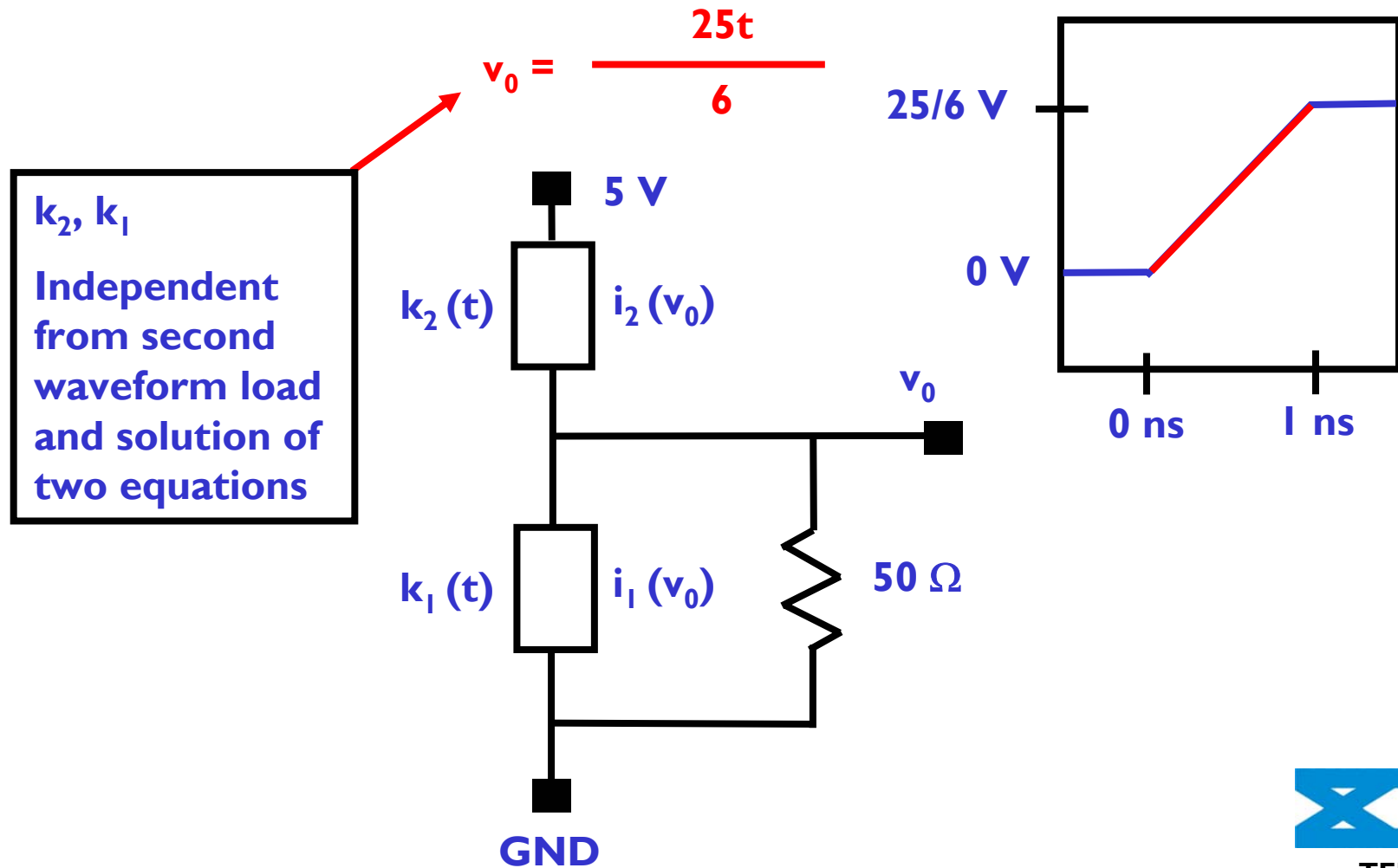
Dual IBIS Linear Table Multipliers



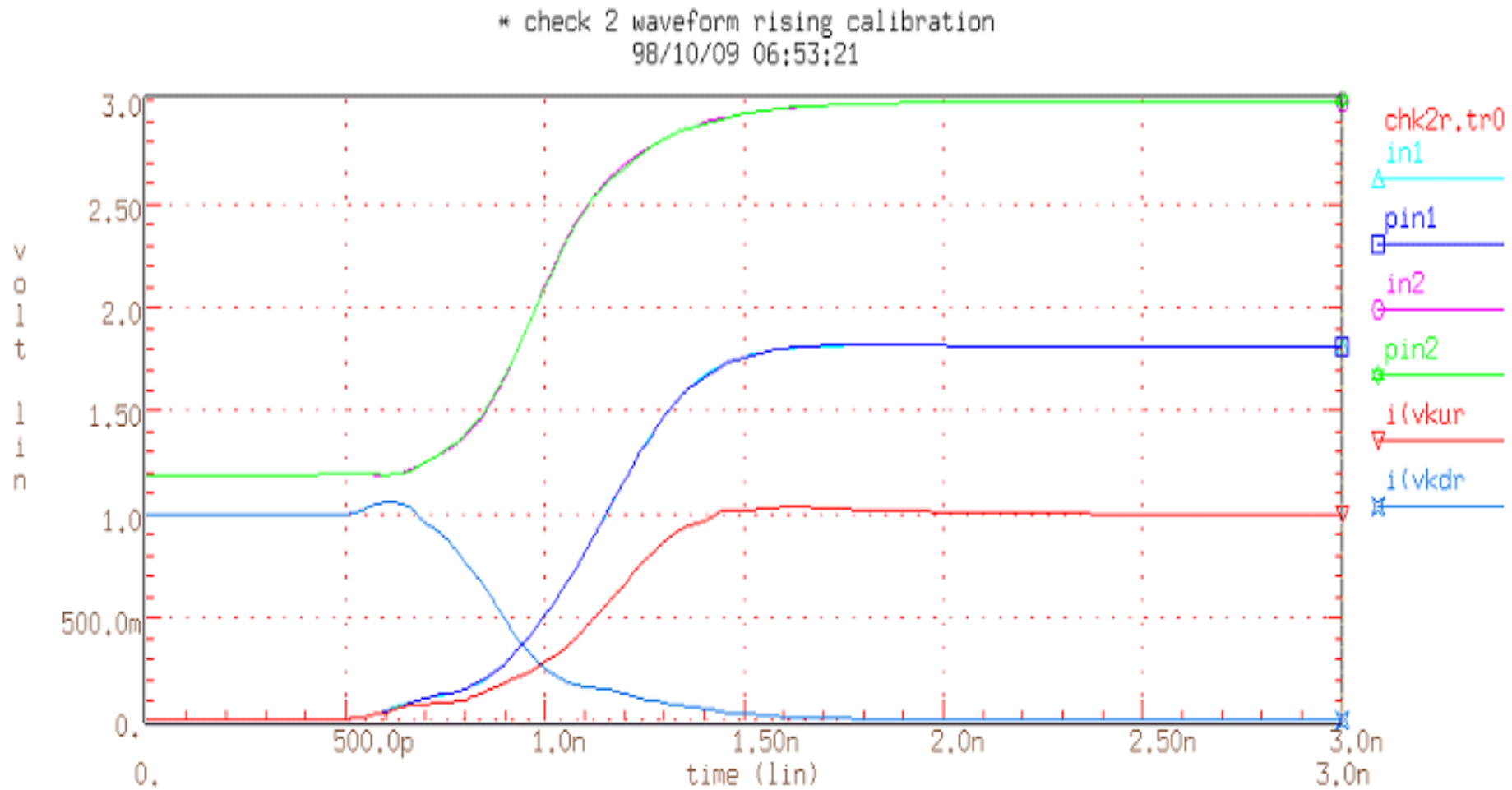
Dependent IBIS Table Multipliers



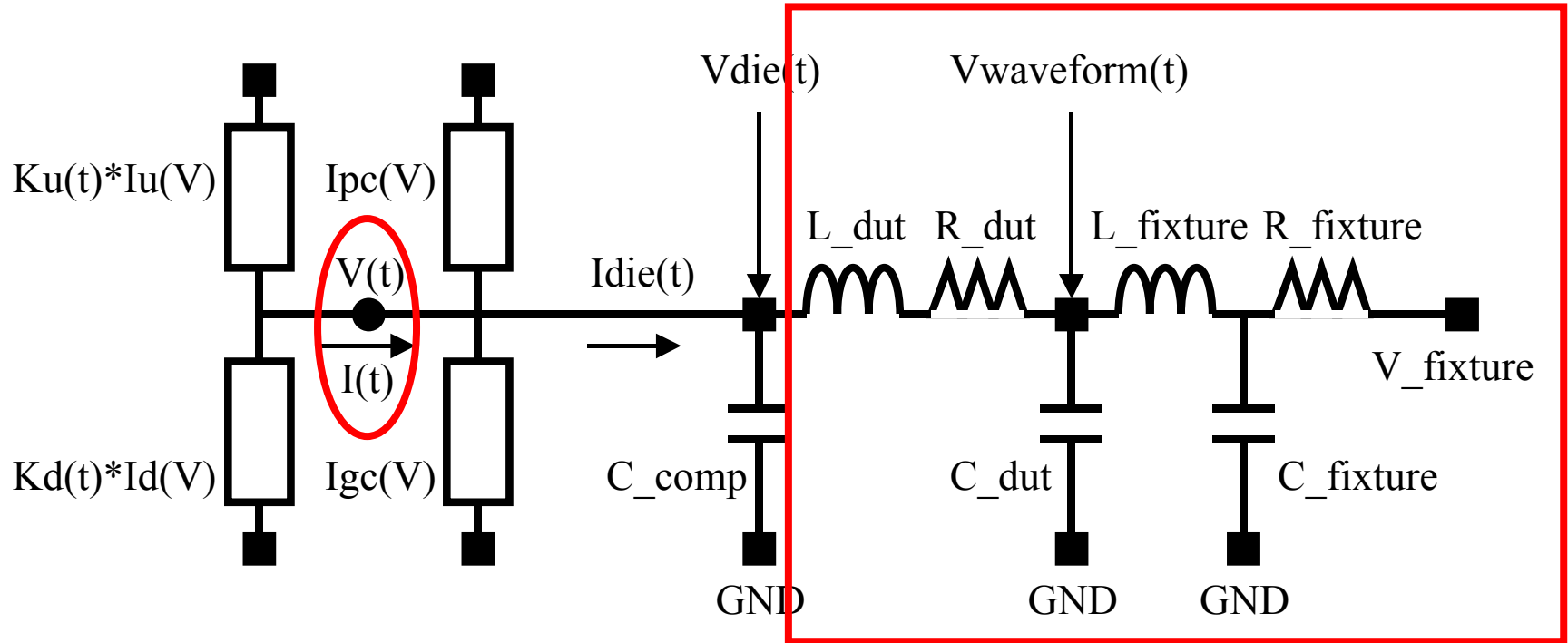
Independent IBIS Table Multipliers



Actual Waveforms and Multipliers

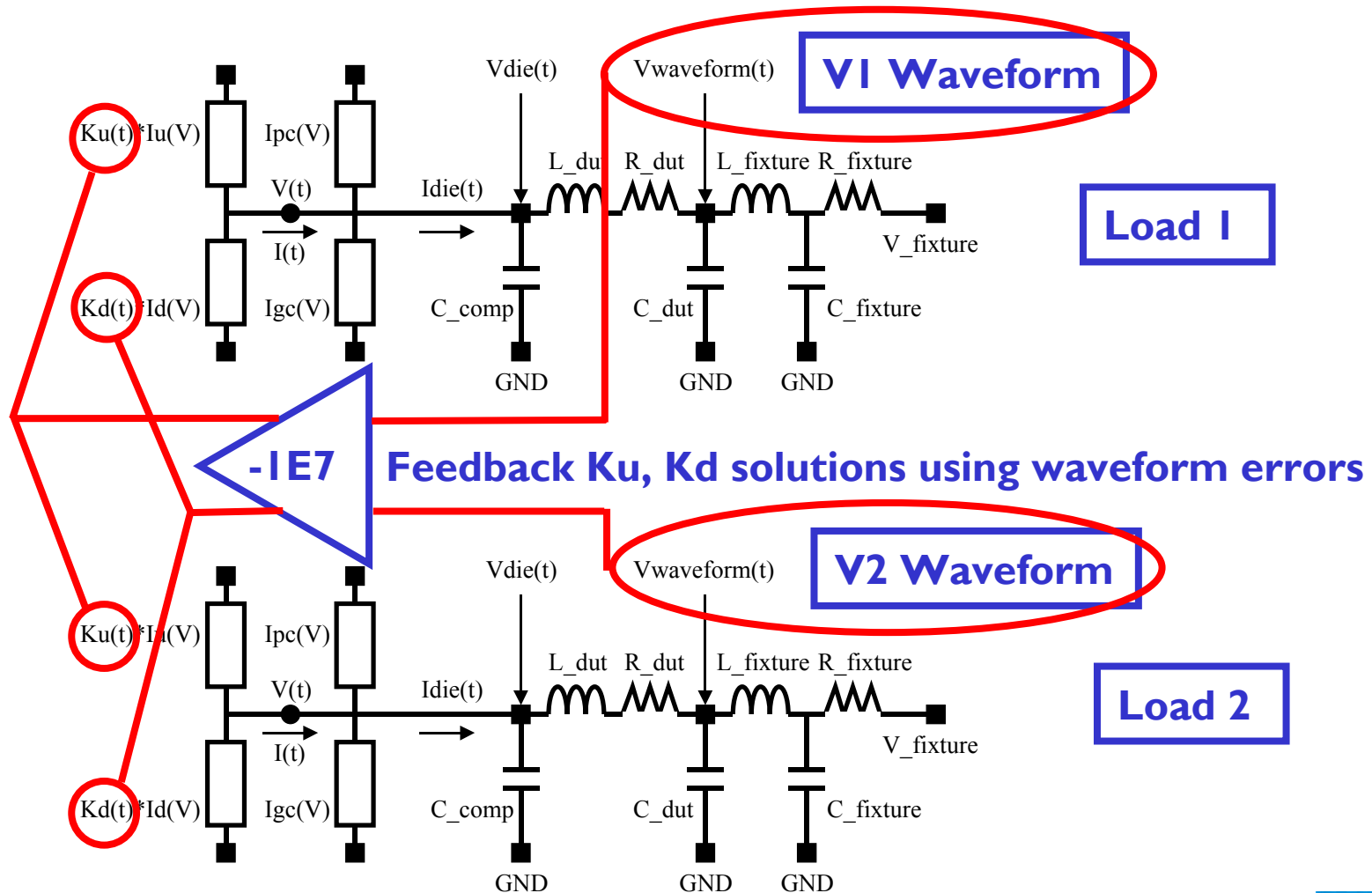


Generalized Test Load



**$V(t)$ and $I(t)$ can be
calculated from load
information**

SPICE Prototype for $K_u(t)$, $K_d(t)$



Feedback SPICE Circuit For Two Non-linear/Table Equations

```

*
* FEEDBACK TABLE ADJUSTMENT ..... VVV
GDET      NDET  GND  CUR=' ( I (VDN2) *I (VUP1) -I (VDN1) *I (VUP2) ) / (1E7) '
VDET      NDET  GND  0
*
GKUR      NKU    GND
+ CUR=' ( (V(IN2) -V(PIN2)) *I (VDN1) - (V(IN1) -V(PIN1)) *I (VDN2) ) /I (VDET) '
VKUR      NKU    GND  0
*
GKDR      NKD    GND
+ CUR=' ( (V(IN1) -V(PIN1)) *I (VUP2) - (V(IN2) -V(PIN2)) *I (VUP1) ) /I (VDET) '
VKDR      NKD    GND  0

```

Kur

Kdr

- $V1(t)/Z(t) = Ku(t)*Iu(V1(t)) + Kd(t)*Id(V1(t))$
- $V2(t)/Z(t) = Ku(t)*Iu(V2(t)) + Kd(t)*Id(V2(t))$

Part of SPICE Encoded IBIS Prototype

```

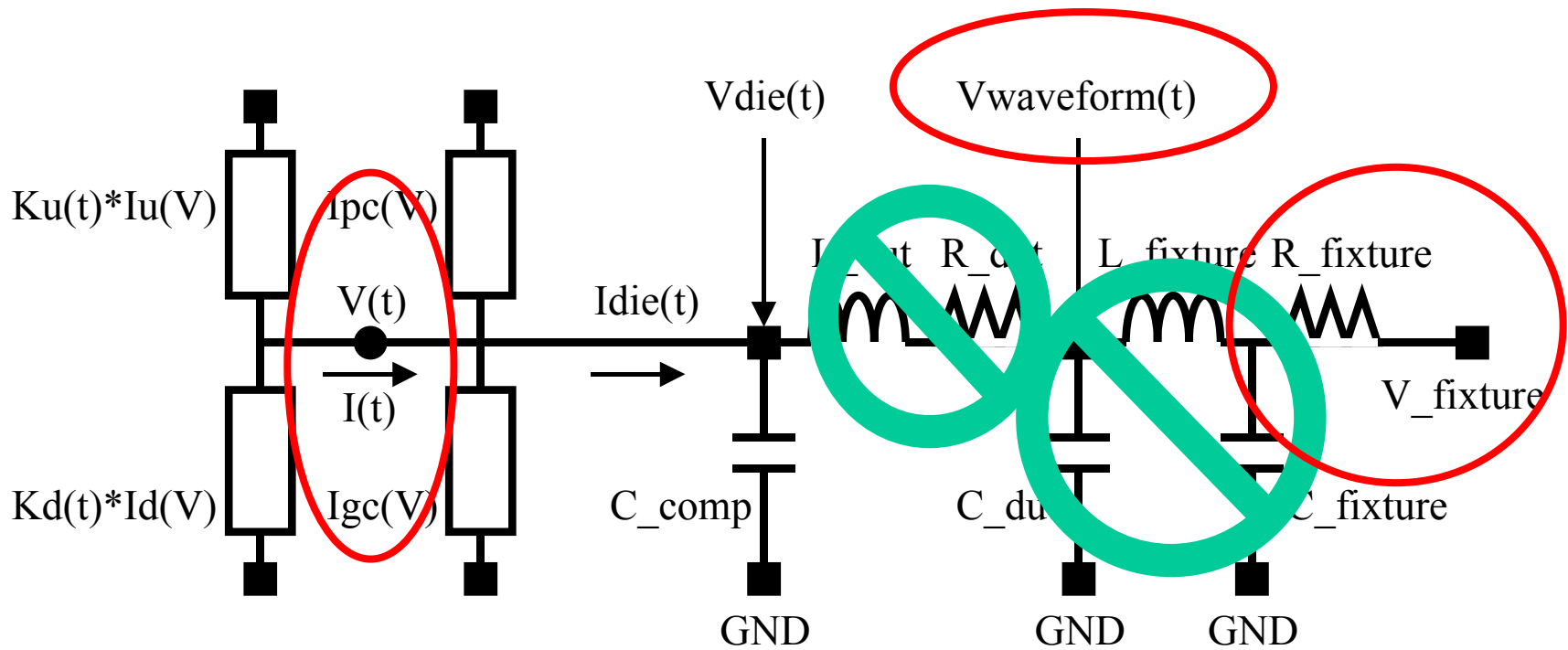
* HIGH SIDE
XUP      OUT1  VCC  NU1          PULLUP
VUP      NU1   VCC  0
GUP      OUT1  VCC  CUR=' -I (VUP) * ( I (VKUR) * I (VON) + I (VKUF) * (1-I (VON) ) ) '
XPC      OUT1  VCC          POWER_CLAMP
*
* LOW SIDE
XDN      OUT1  GRD  ND1          PULLDOWN
VDN      ND1   GRD  0
GDN      OUT1  GRD  CUR=' -I (VDN) * ( I (VKDR) * I (VON) + I (VKDF) * (1-I (VON) ) ) '
XGC      OUT1  GND  GND_CLAMP
*
* C_COMP AND DUT PACKAGE
XCAP     OUT1  GRD          C_COMP
XPKG     OUT1  GRD  PIN1      PACKAGE
*
* LOAD
TLOAD    PIN1  GRD  PIN9      GRD  Z0=50 TD=1N
RLOAD    PIN9  GND  50G
*
* VOLTAGE CONTROL (AMPLITUDE (0 TO 1), PULSE WIDTH & PERIOD)
VPULSE   STEP  GRD  0  PULSE (1 0 0P 1P 1P 5N 10N)

```

Kur, Kdr

Kuf, Kdf

Recommended Test Load, Industrial usage



Recommended Loads:

50 Ω to V_{cc}

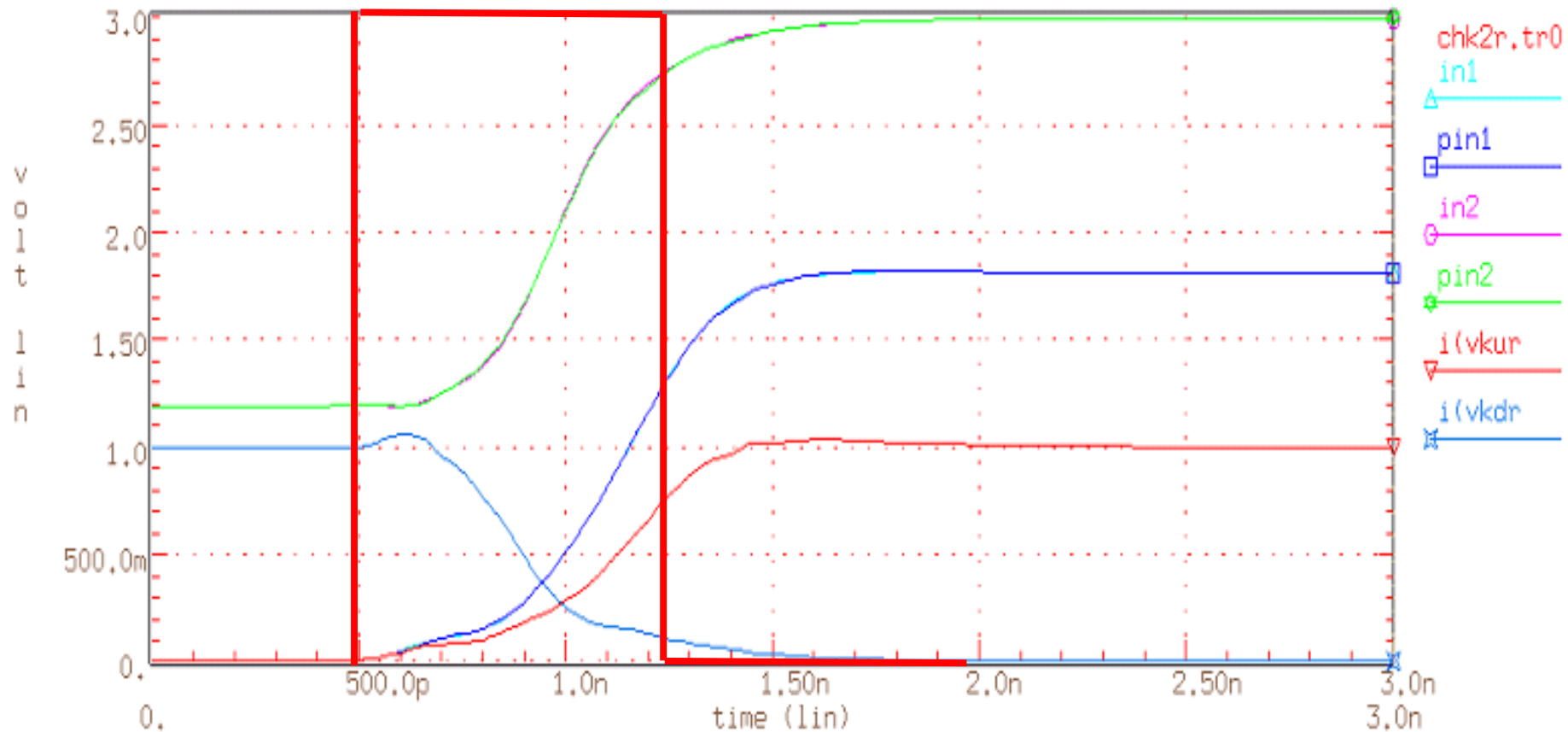
50 Ω to Gnd

Problems and Limitations

- Ground, power currents a function of the model, may not be accurate
 - Gate modulation effects
 - Could be fixed with more tables or parameters
- Timing to internal buffer nodes
- Frequency dependent impedance models
- Delay timing errors with over-clocking - shown next

Over-clocking Problem with IBIS, No Simple Solution for Delays

* check 2 waveform rising calibration
98/10/09 06:53:21



Conclusions

- Well constructed IBIS models and good algorithms yield accurate results
- However, there are limitations