Case study of IBIS V4.1 by JEITA EDA-WG

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JEITA EDA-WG
A. Itoh, T. Watanabe, N. Matsui

JEITA ; Japan Electronics and Information Technology Industries Association

Outlines

1. JEITA EDA-WG Activities
2. Case study of IBIS V4.1
3. EMI Model

1. JEITA EDA-WG Activities

Objectives of JEITA EDA

EDA Model for

Digital Consumer Electronics

Cellular Phone, LCD TV, Digital Camera/Video, DVD Recorder

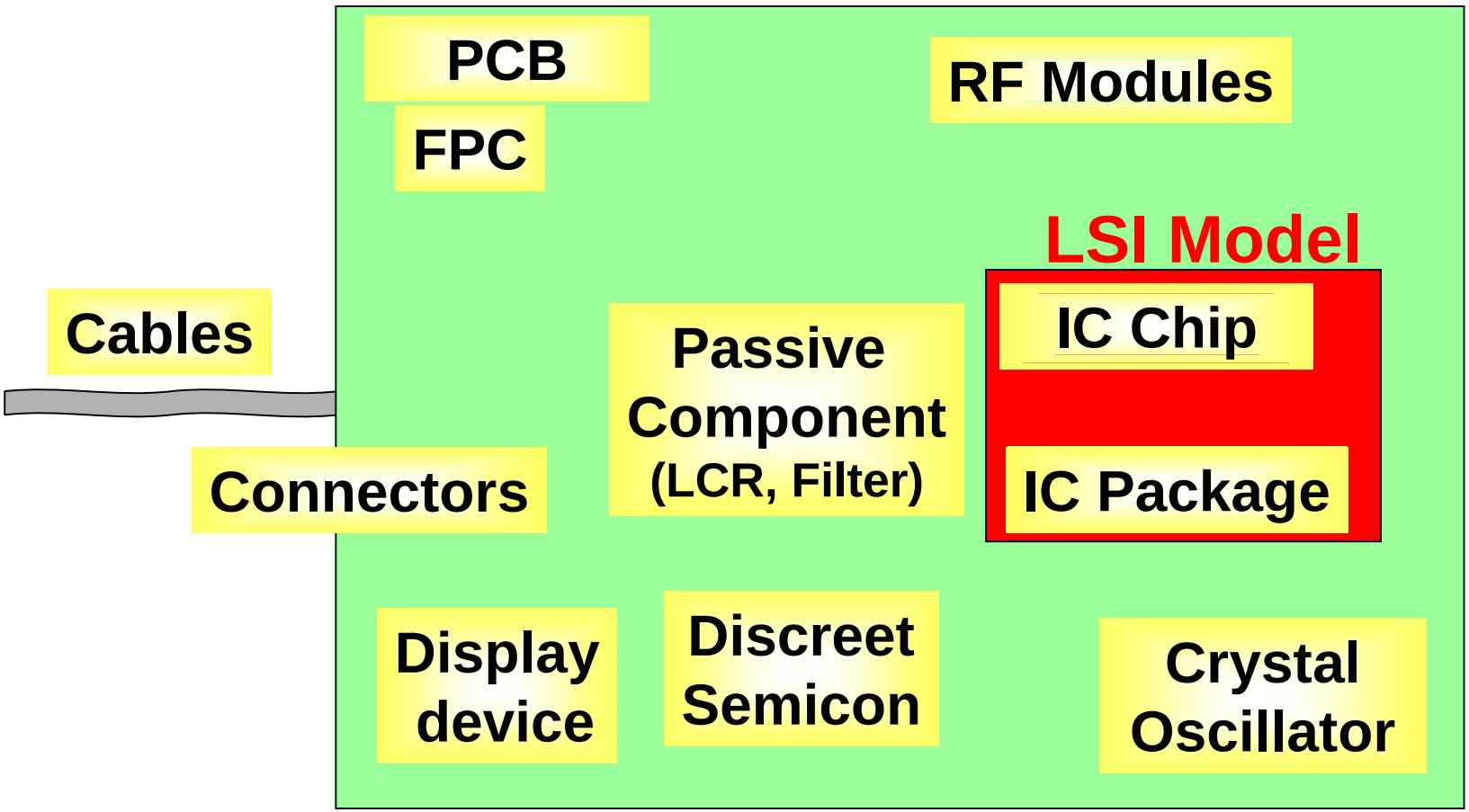
(Digital , RF, and Analog circuits)

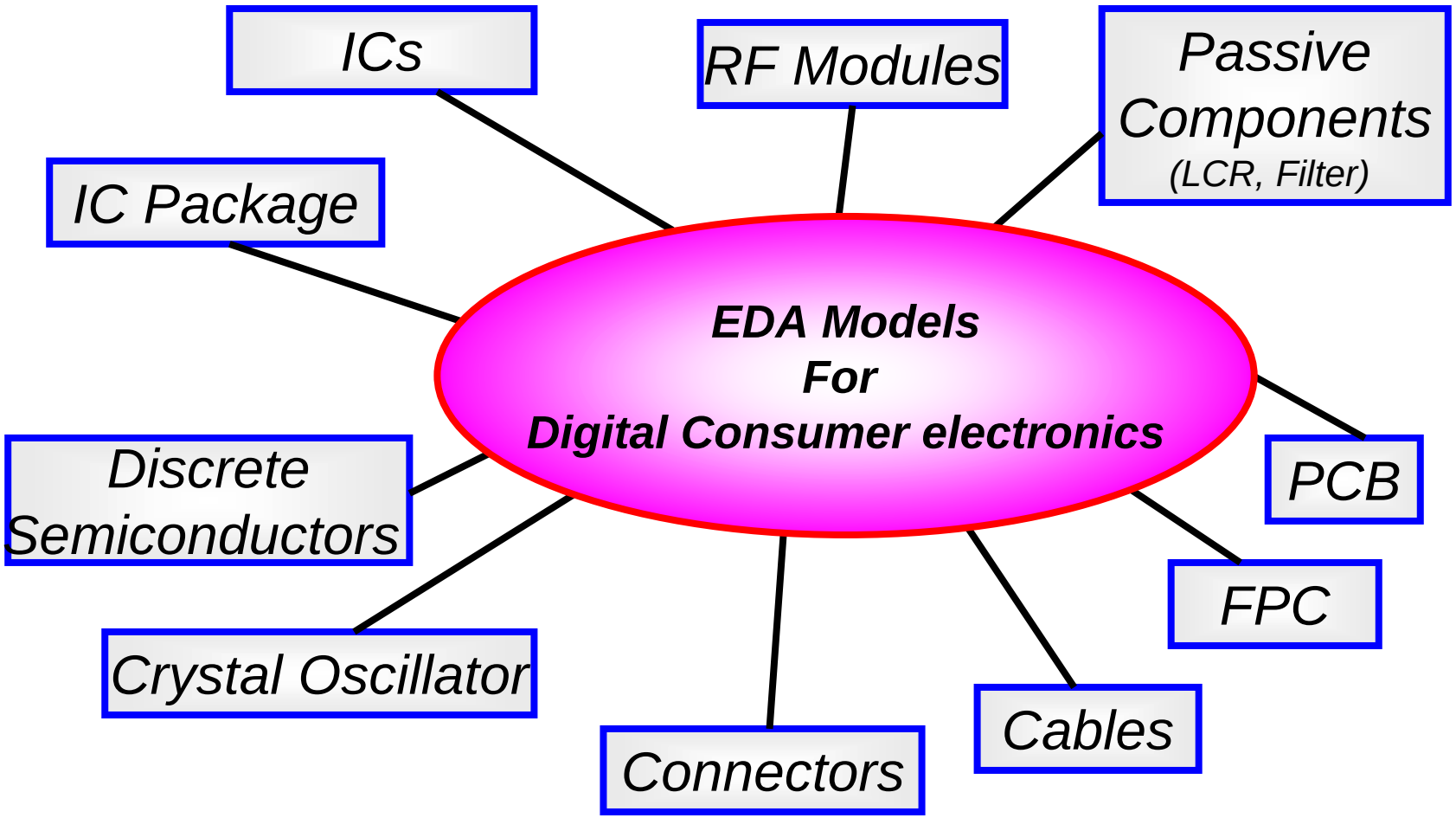
Auto Mobile Electronics ?

(Motor Drive, EMC)

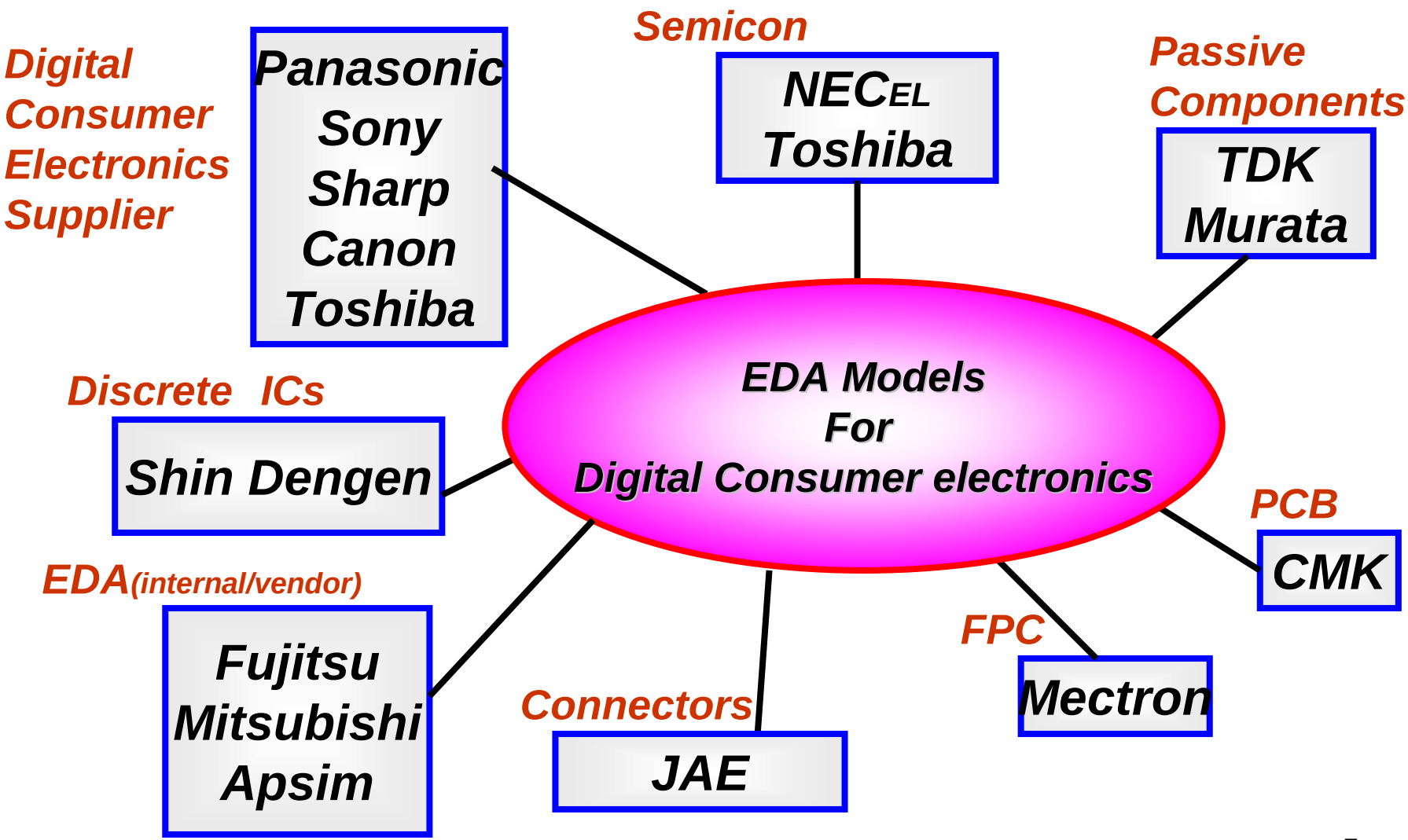
< Applicability of IBIS V4.1 >

EDA Model for SI, PI and EMI Simulation





JEITA EDA-WG Member

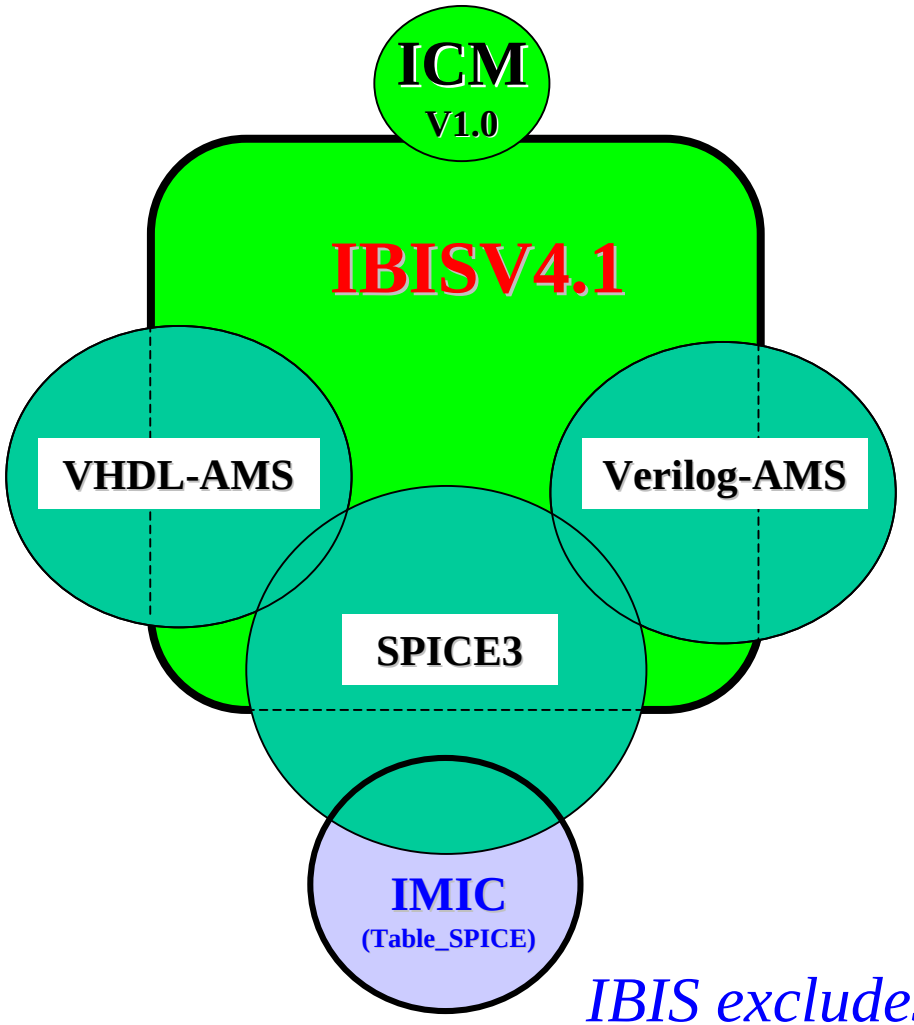


2. Case study of IBIS V4.1

Summary of investigation of IBIS V4.1

	IBIS				Comments
	V3.2	V4.1 SPICE	V4.1 *AMS	ICM	
ASIC/SOC for EMI/SSO		✓	(✓)		Accurate models need the internal gates for EMI/SSO. IBIS V4.1 SPICE discloses process parameters.
Power Semiconductor OpAMP		✓	(✓)		IBIS V4.1 SPICE discloses process parameters.
DSP, AD/DA, Xtal	✓	✓	✓		I/O for SI can be described in V3.2. Inside needs *AMS.
Passive Components	(✓)	✓	(✓?)	✓	Can describe LCRK models ICM describes S-parameters
Package, Module, PCB	(✓)	✓	(✓?)	✓	IBIS 4.1 SPICE can't describe S-parameters or lossy coupled transmission line. ICM can't include discrete components. SiP and PWRGND modeling.
Connector, Cable, FPC		(✓)	(✓)	✓	ICM can't include discrete components.

Understanding of IBIS V4.1



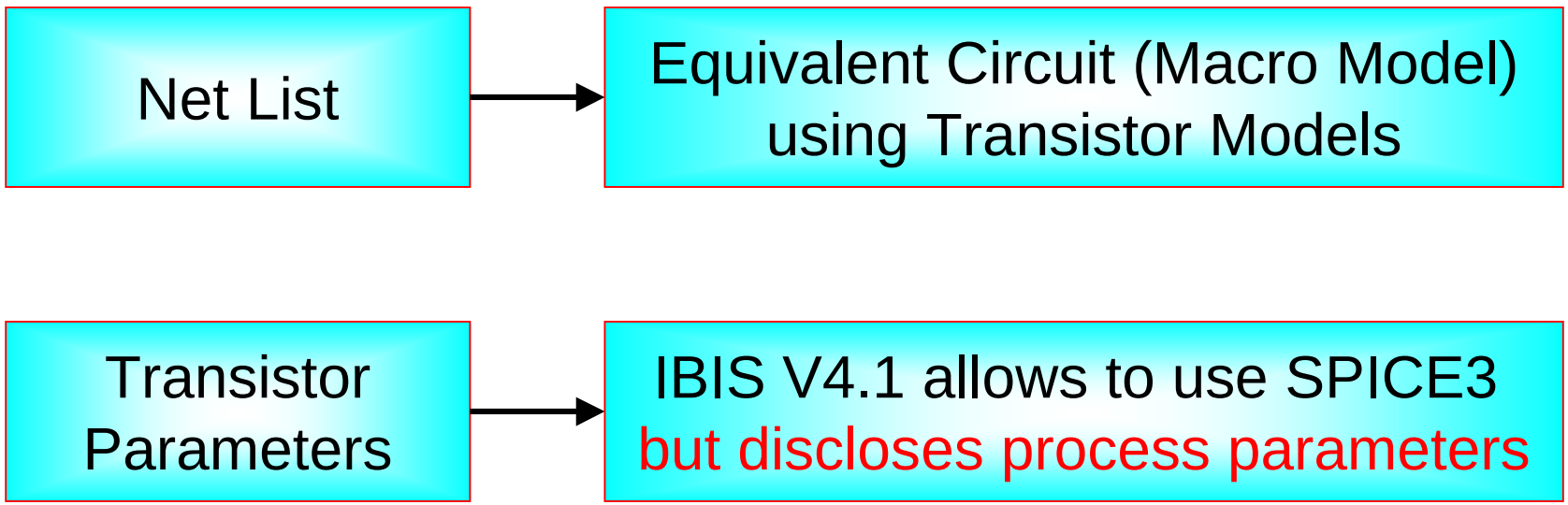
IBIS

- [Component]
  - [Node Declarations]
  - [Circuit Call]
- [Model]
  - Model_type
  - [External Model]
- [External Circuit]

IBIS excludes IMIC

How to describe SPICE transistor model in IBIS 4.1 without disclosing proprietary information

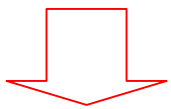
Models described in SPICE transistors have flexibility.



IMIC (Table_SPICE) allows to hide the transistor parameters, but IBIS V4.1 excludes IMIC.

How to hide transistor model parameters in IBIS V4.1 SPICE description without losing accuracy

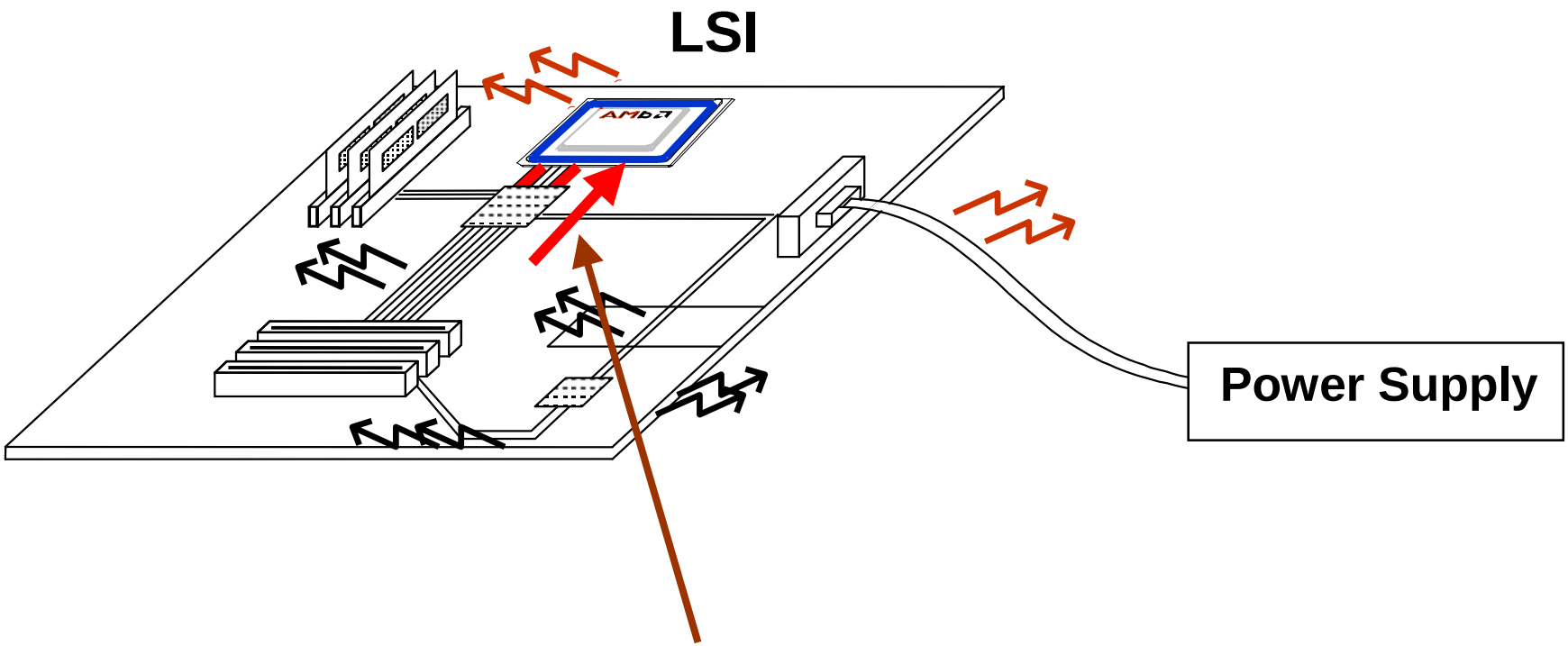
IMIC (Table_SPICE) allows to hide the transistor parameters, but IBIS V4.1 excludes IMIC.



Need to have a bridge from IMIC to IBIS V4.1 SPICE 3 without disclosing the original SPICE transistor parameters.

3. EMI Model (NEC/APSIM)

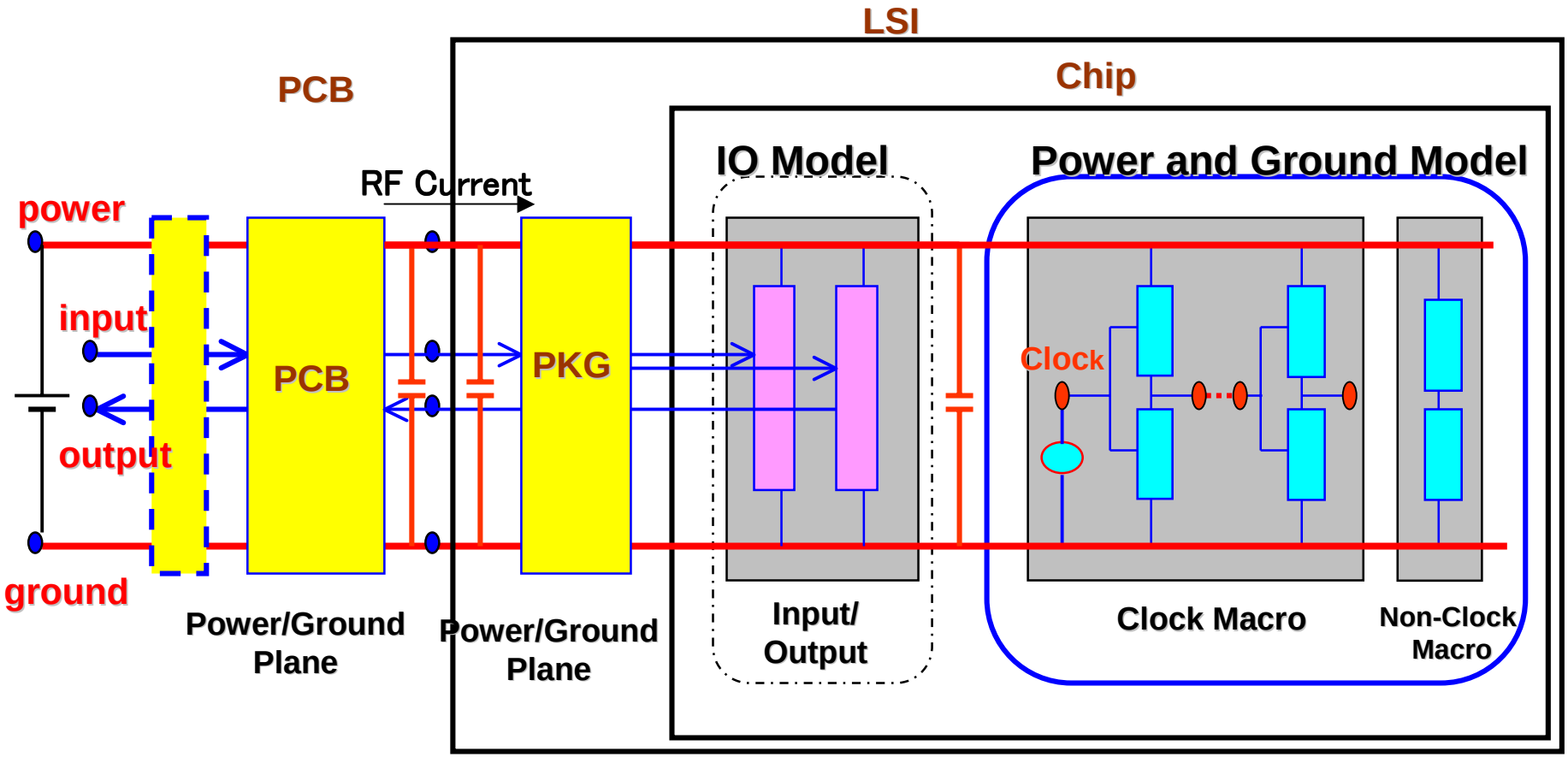
LSI Model for EMI Simulation



RF Current of LSI

1. Measurement; IEC61967-6.Magnetic Probe Method
2. Simulation Model; EMI Model for LSI

EMI Simulation for PCB



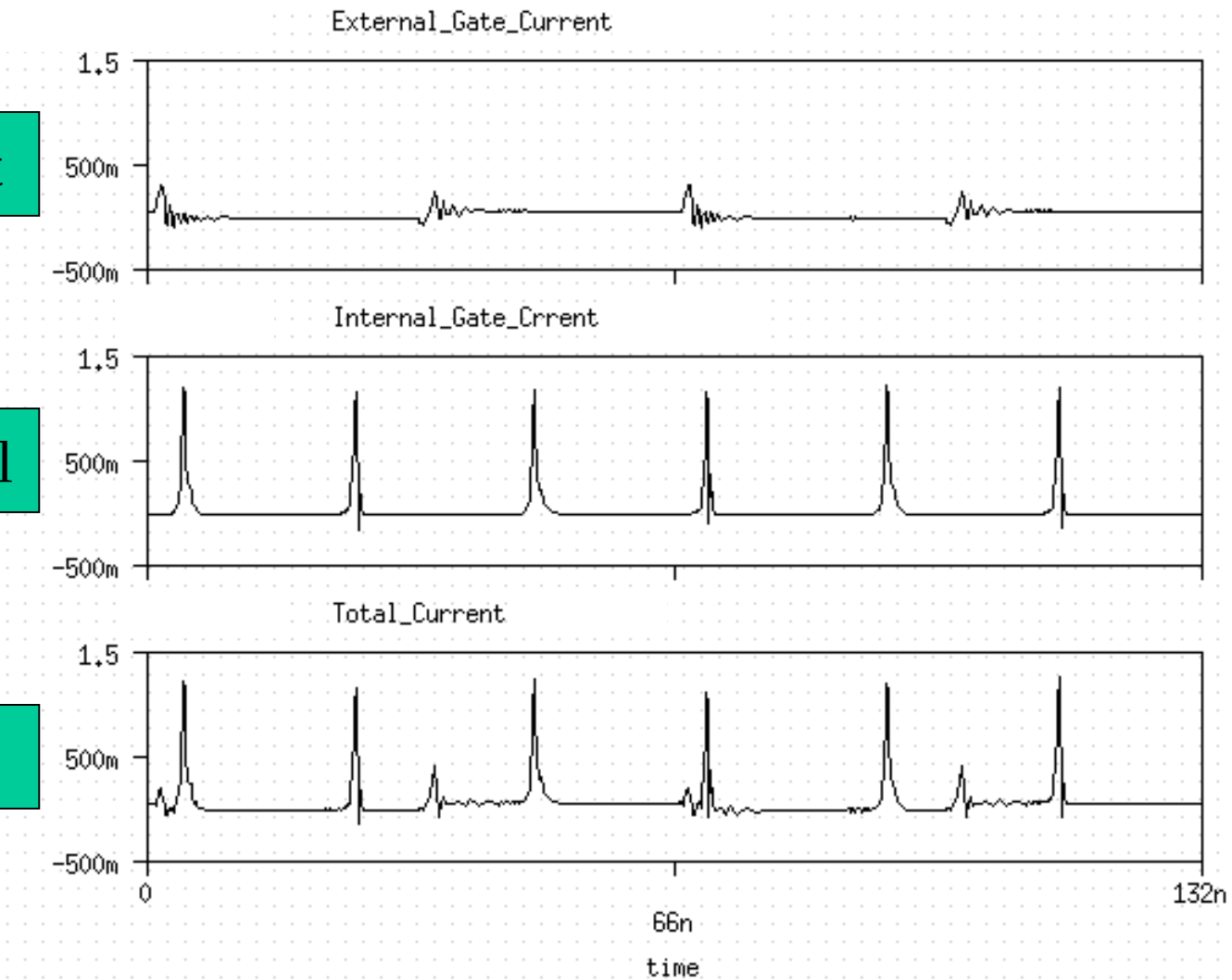
EMI simulation needs the internal gates power/ground model with loading effects in time/frequency domain.

Current Waveforms of 32-bit LSI

Output

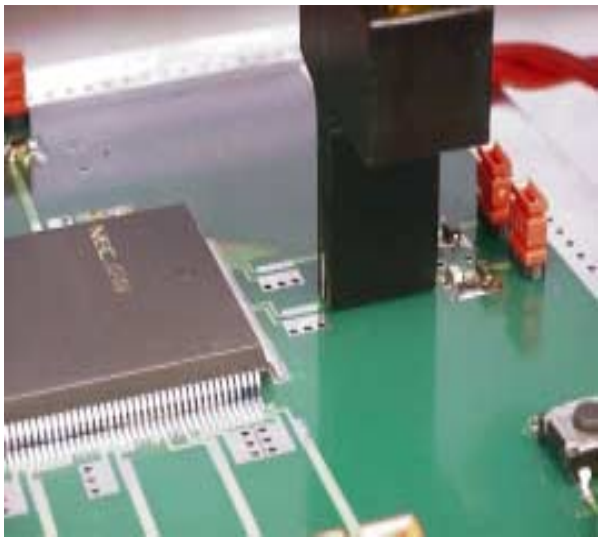
Internal

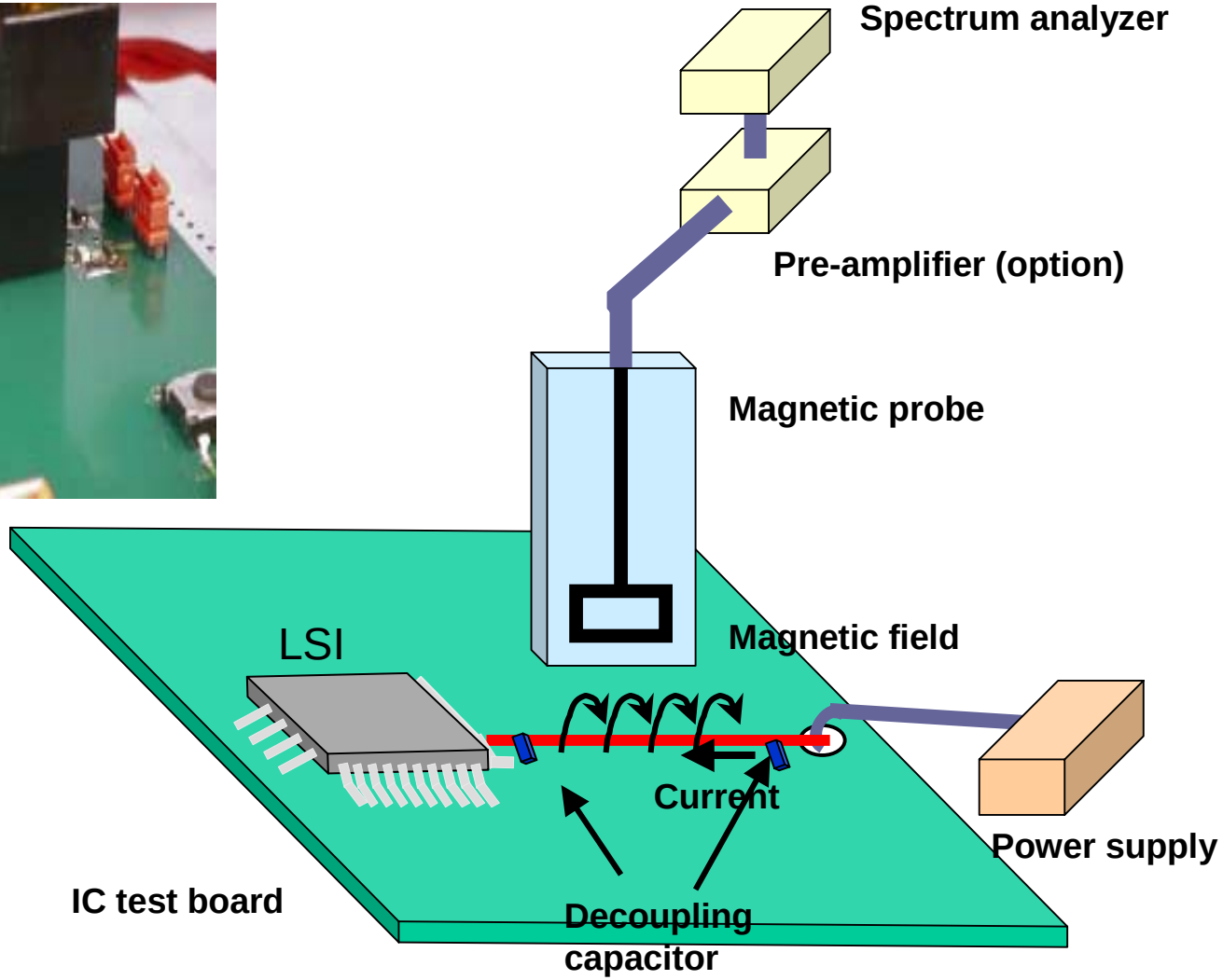
Total



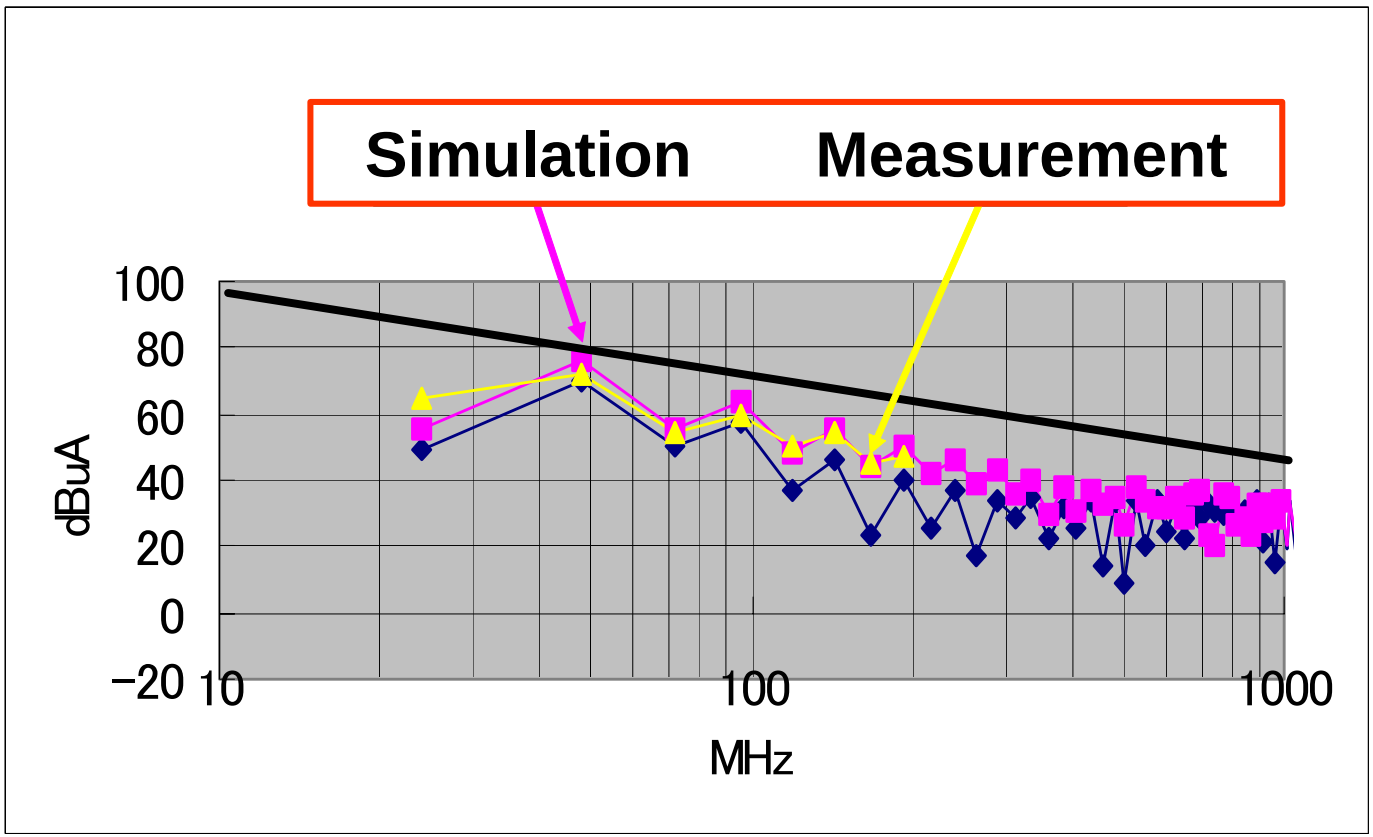
Measurement

IEC61967-6. Magnetic Probe Method



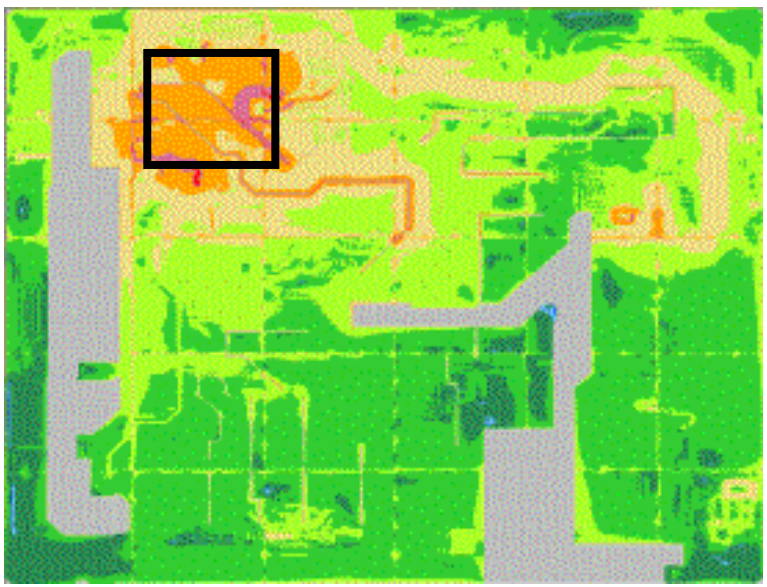


Simulation VS Measurement

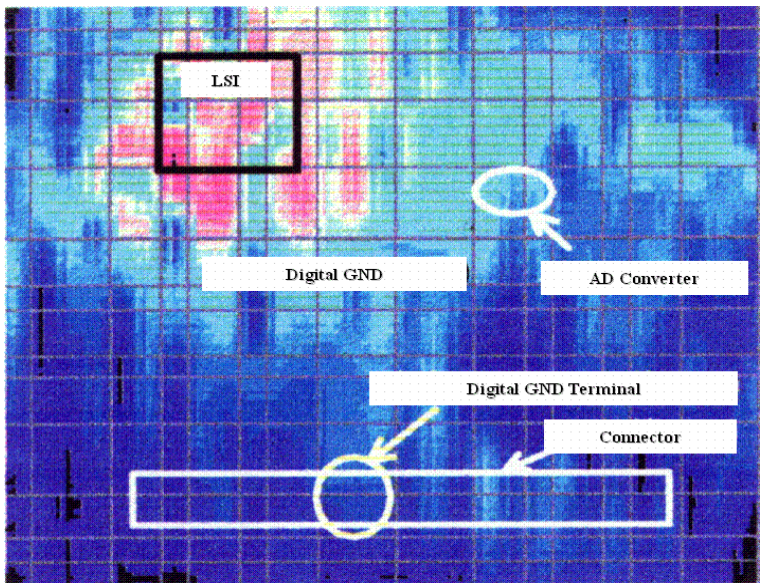


Current/Magnetic Field Distribution

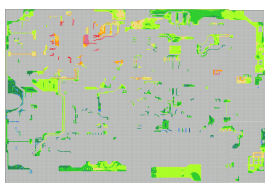
Simulation

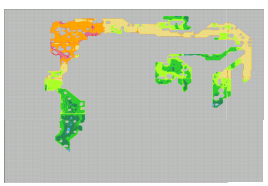


Measurement



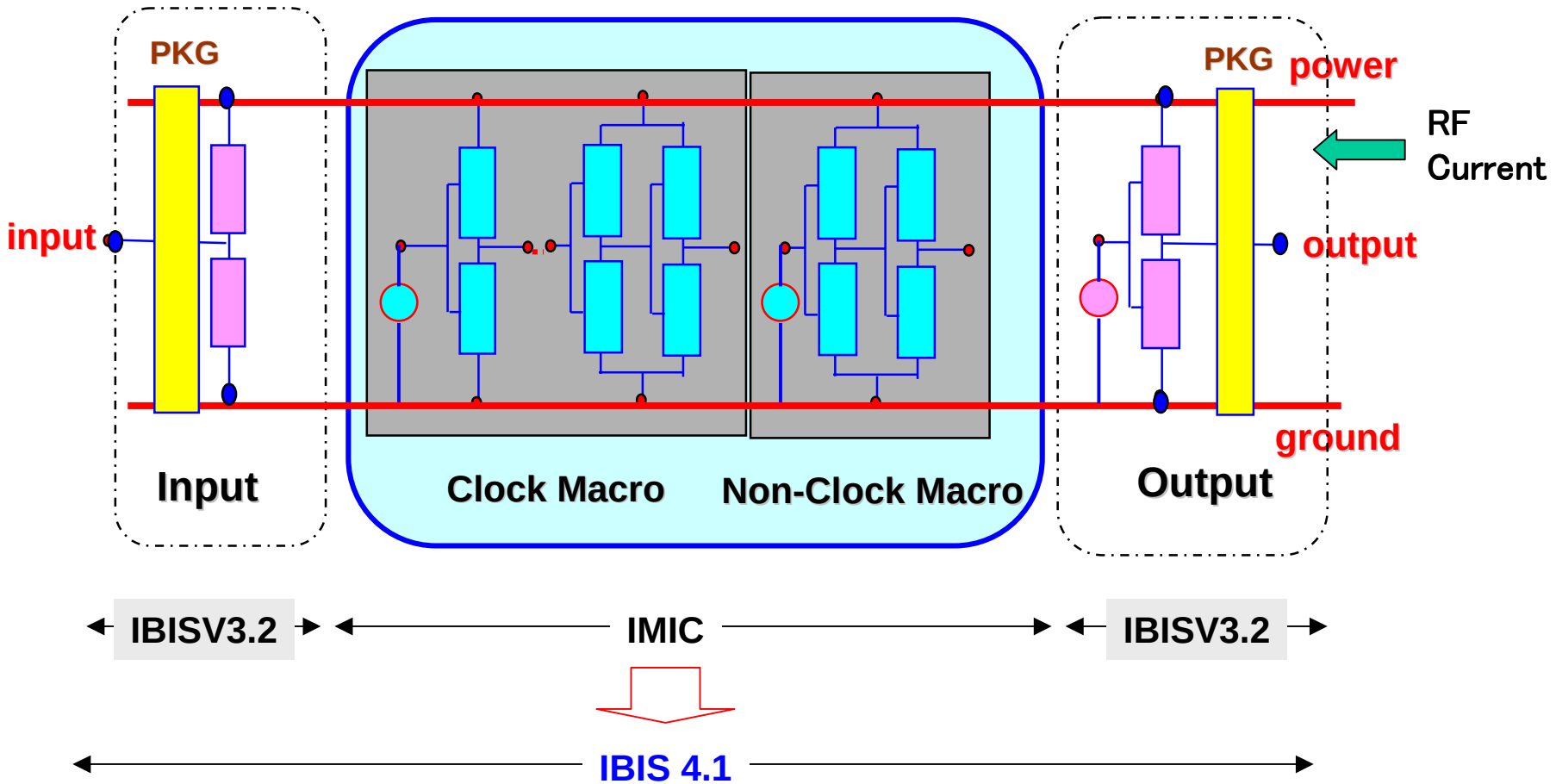
© APSIM



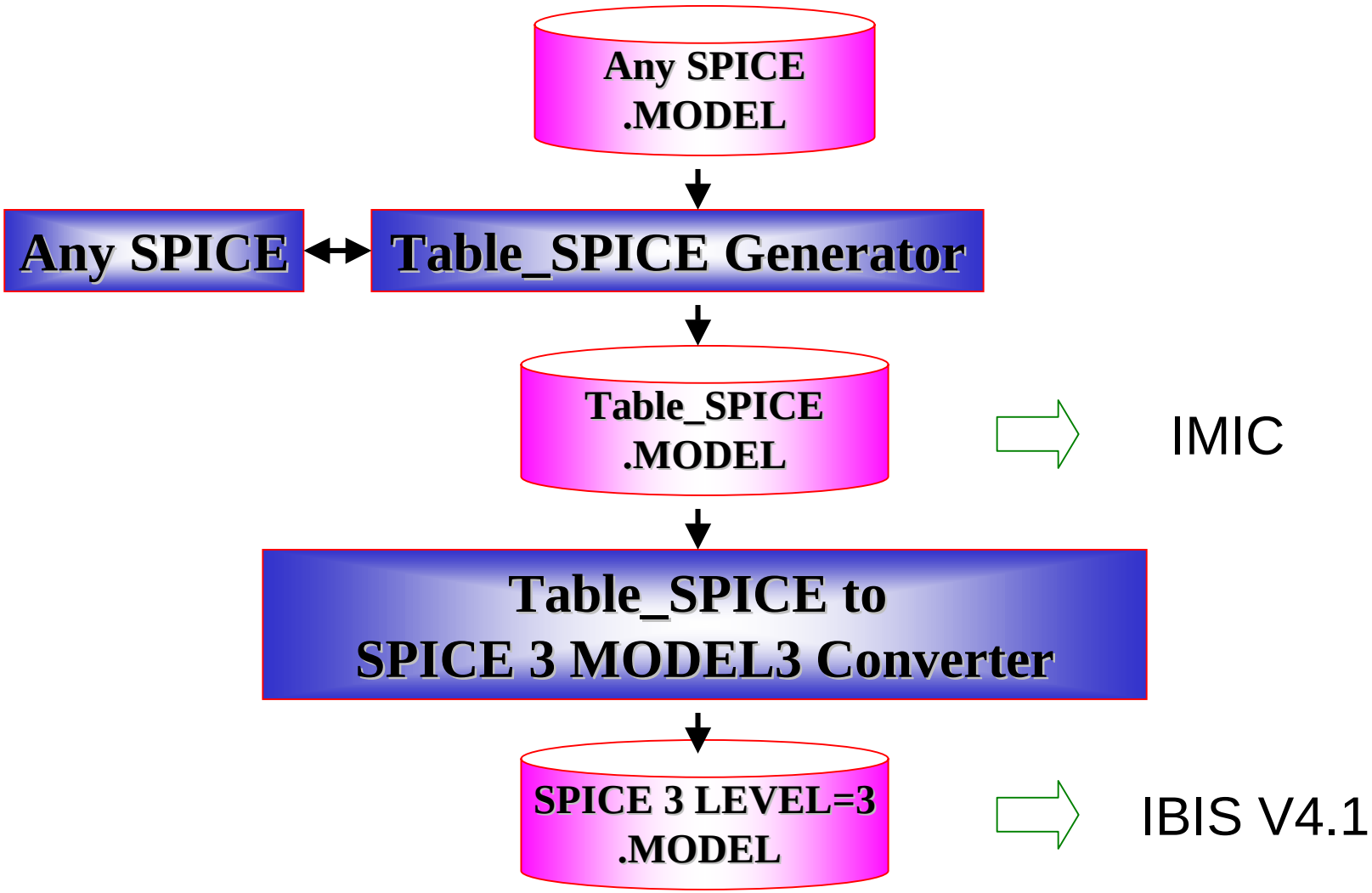


EMI Simulation Model for LSI

Power and Ground Model of Core Logics (internal gates)

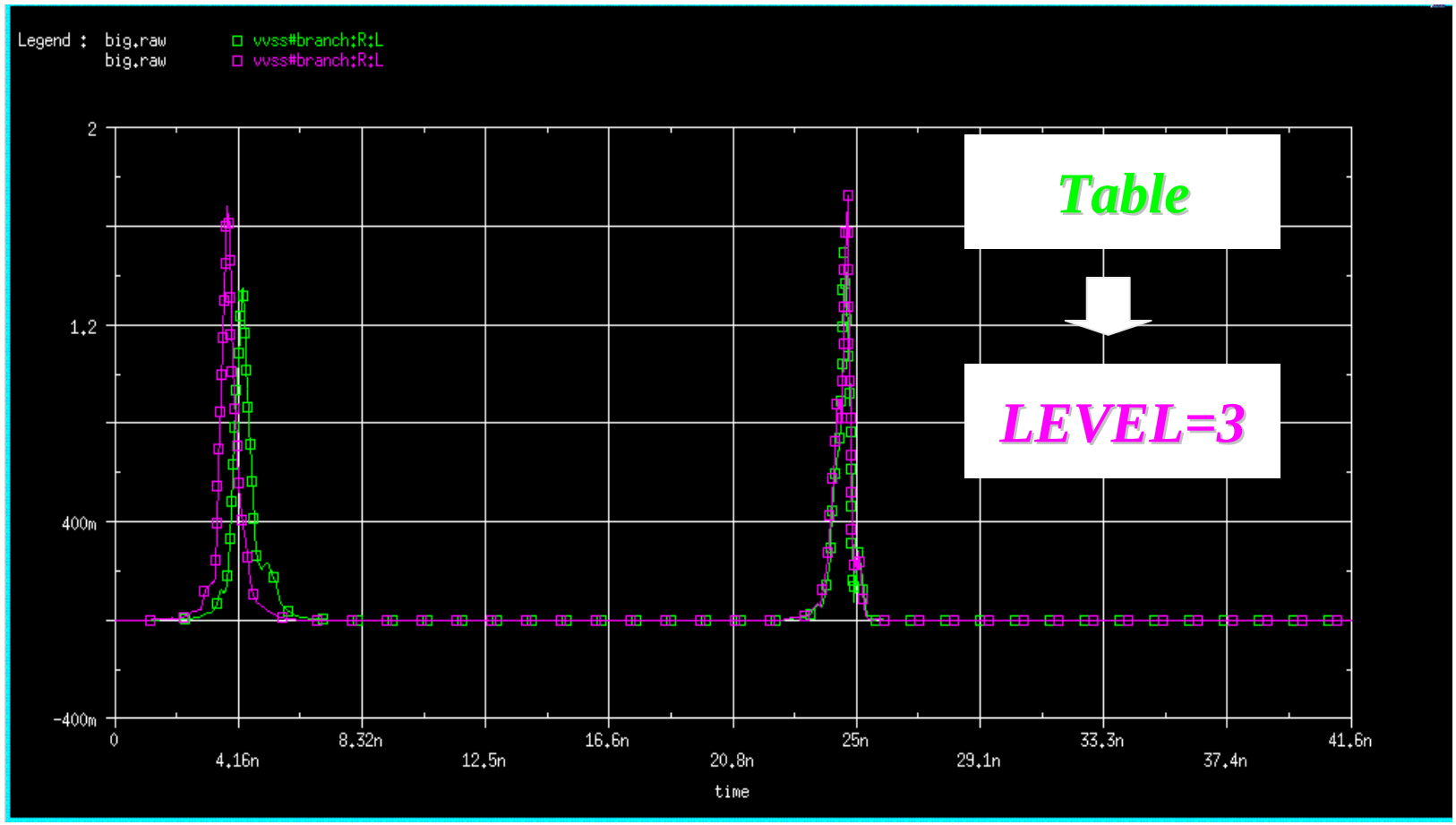


Developed IMIC to IBIS V4.1 Converter



The parameters of LEVEL=3 can't disclose those of the original SPICE.

Full chip power/ground current models in time/frequency domain for EMI Simulation



Example of LSI Power/Ground Model (IBIS V 4.1)

```
Apsim LSI Power and Ground model ckt file
* Command:       ApsimLPG      1.400.5
* File:  big.ckt
* Pre - Driver Model
xPRDRV.in PreVDD PreVSS PreIN PreMID PRDRV.in
xPRDRV.out PreVDD PreVSS PreMID PreOUT PRDRV.out
vvdd1 PreVDD 0 dc 3.3
vvss1 PreVSS 0 dc 0.0
xshort1 PreOUT D2P_N0039026 D2P_N0000004 D2P_N0000003 D2P_N0000002 D2P_N0000001 short1
* Clock - Driver Model
cD2P_N0039026_1 D2P_N0039026 VDD 2.192774e-013
cD2P_N0039026_2 D2P_N0039026 VSS 2.192774e-013
xD2P_I0033331.in VDD VSS D2P_N0039026 mid_D2P_I0033331 F111.in
xD2P_I0033331.out VDD VSS mid_D2P_I0033331 D2P_N0029114 F111.out
cD2P_N0029114_1 D2P_N0029114 VDD 5.332500e-016
cD2P_N0029114_2 D2P_N0029114 VSS 5.332500e-016
xD2P_I0033330.in VDD VSS D2P_N0029114 mid_D2P_I0033330 F111.in
xD2P_I0033330.out VDD VSS mid_D2P_I0033330 D2P_N0028992 F111.out
cD2P_N0028992_1 D2P_N0028992 VDD 3.680150e-015
cD2P_N0028992_2 D2P_N0028992 VSS 3.680150e-015
xD2P_I0033329.in VDD VSS D2P_N0028992 mid_D2P_I0033329 F111.in
xD2P_I0033329.out VDD VSS mid_D2P_I0033329 D2P_N0028991 F111.out
cD2P_N0028991_1 D2P_N0028991 VDD 8.436000e-016
cD2P_N0028991_2 D2P_N0028991 VSS 8.436000e-016
```

```
xFF1.in VDD VSS D2P_N0000092 FF1_mid FF1.in
xFF1.out VDD VSS FF1_mid FF1_out FF1.out
rFF1.out FF1_out 0 100meg
* Non-Clock Model
*xnc VDD VSS NCFF
xnc VDD VSS NCCR
* Voltage source
vvdd VDD 0 dc 3.3
vvss VSS 0 dc 0.0
* Open Nodes
Ropen1 node_open1 0 100Meg
* Include file
.include      big.tst
.include      mos_tsp.lib
*.include spice.lib
.include      big.sckt
* Save current
.save vvdd#branch vvss#branch
.end
```

Example of LSI Power/Ground Model (IBIS V 4.1)

① Original SPICE MOS parameters

```
.MODEL  NENH            NMOS
+    LEVEL     =                          TOX       =
+    LMIN      =                          PHI       =
+    VFB       =                          GAMMA     =
+    VDOP      =                          CDOP      =
```

② Table_SPICE MOS V-I-C data

```
.model NENH nmos model=table
+ l=0.25u w=2u pd=5e-6 ps=5e-6 ad=0.5e-12 as=0.5e-12
+ nolimiting
+ data=channel
+ points=1326
+ grid=yes
+ vbs = 0.000e+00
*    Vgs        Vds           Ids          Cgs           Cgd          Cgb
*
+ 0.000e+00  0.000e+00  0.000e+00  2.093e-16  2.093e-16  2.763e-16
+ 0.000e+00  1.000e-01  1.821e-12  2.093e-16  2.093e-16  2.749e-16
+ 0.000e+00  2.000e-01  2.039e-12  2.093e-16  2.093e-16  2.734e-16
+ 0.000e+00  3.000e-01  2.240e-12  2.093e-16  2.093e-16  2.720e-16
+ 0.000e+00  4.000e-01  2.460e-12  2.093e-16  2.093e-16  2.706e-16
+ 0.000e+00  5.000e-01  2.704e-12  2.093e-16  2.093e-16  2.691e-16
+ 0.000e+00  6.000e-01  2.973e-12  2.093e-16  2.093e-16  2.677e-16
```

③ SPICE 3 Level=3 MOS minimum parameters

```
.model NENH nmos level = 3 tox = 1.11102e-08 phi = 0.6
+ vt0 = 0.631419 kp = 1.31264e+09 theta = 8.18536e+12
+ vmax = 196589 u0 = 4.22341e+15
+ js = 2.0364e-06
```