I-V curve linearity and buffer impedance

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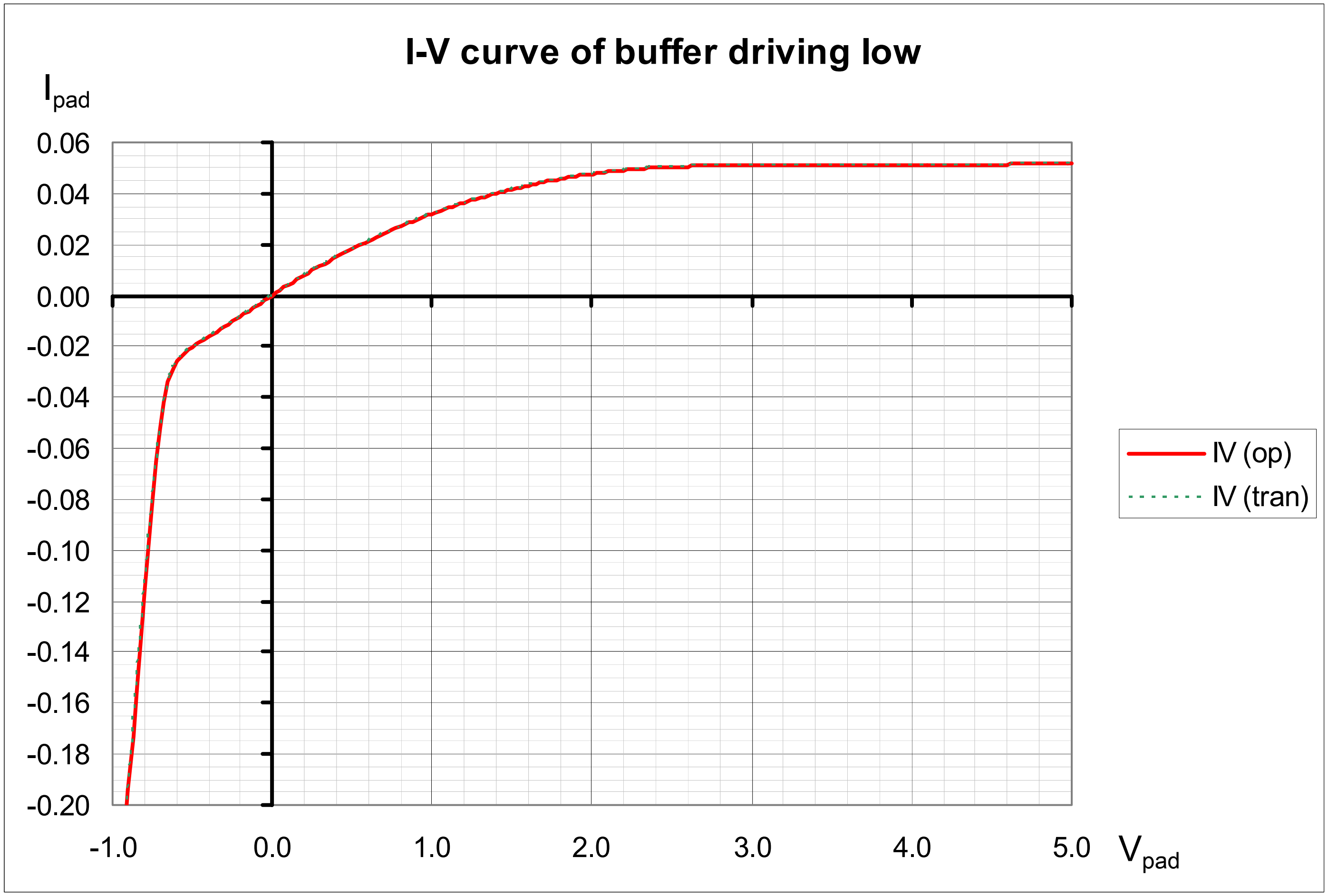
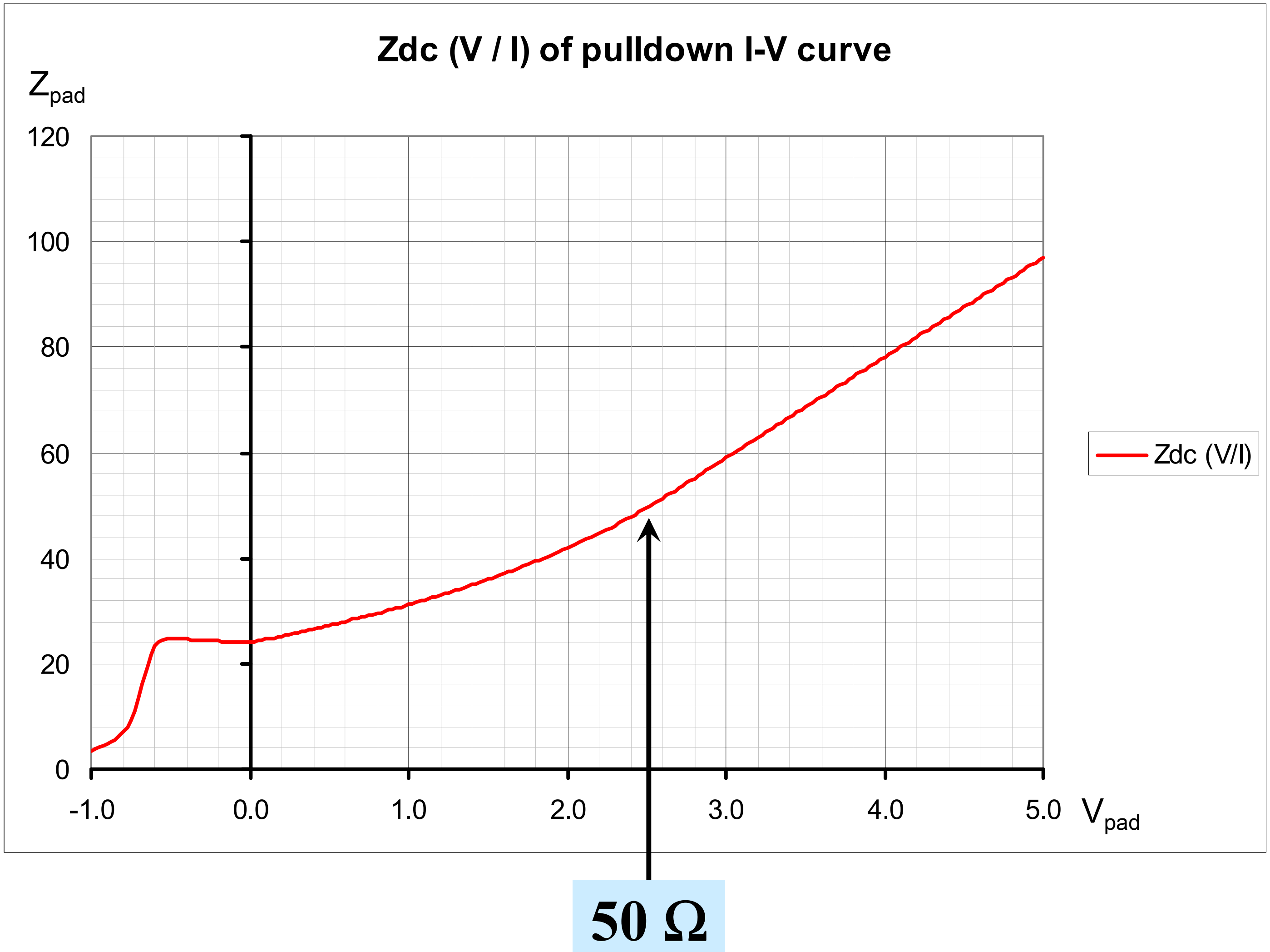
Background

- **New, high frequency bus specifications see the need to not only define the min., max. I-V curve range, but also the allowable shape of the I-V curve within that range**
  - linearity specification
- **Some buses are designed to operate in the current mode, others use linear drivers**
  - DDR3 (linear driver)
  - PCI-express (current mode driver)
- **"R_{on}" (vs. voltage) is another popular way to describe the driver**
- **There are numerous ways to bound the shape of the I-V curve**
- **We need to understand the physical meaning and relationship of these terms better to make meaningful buffer specifications**

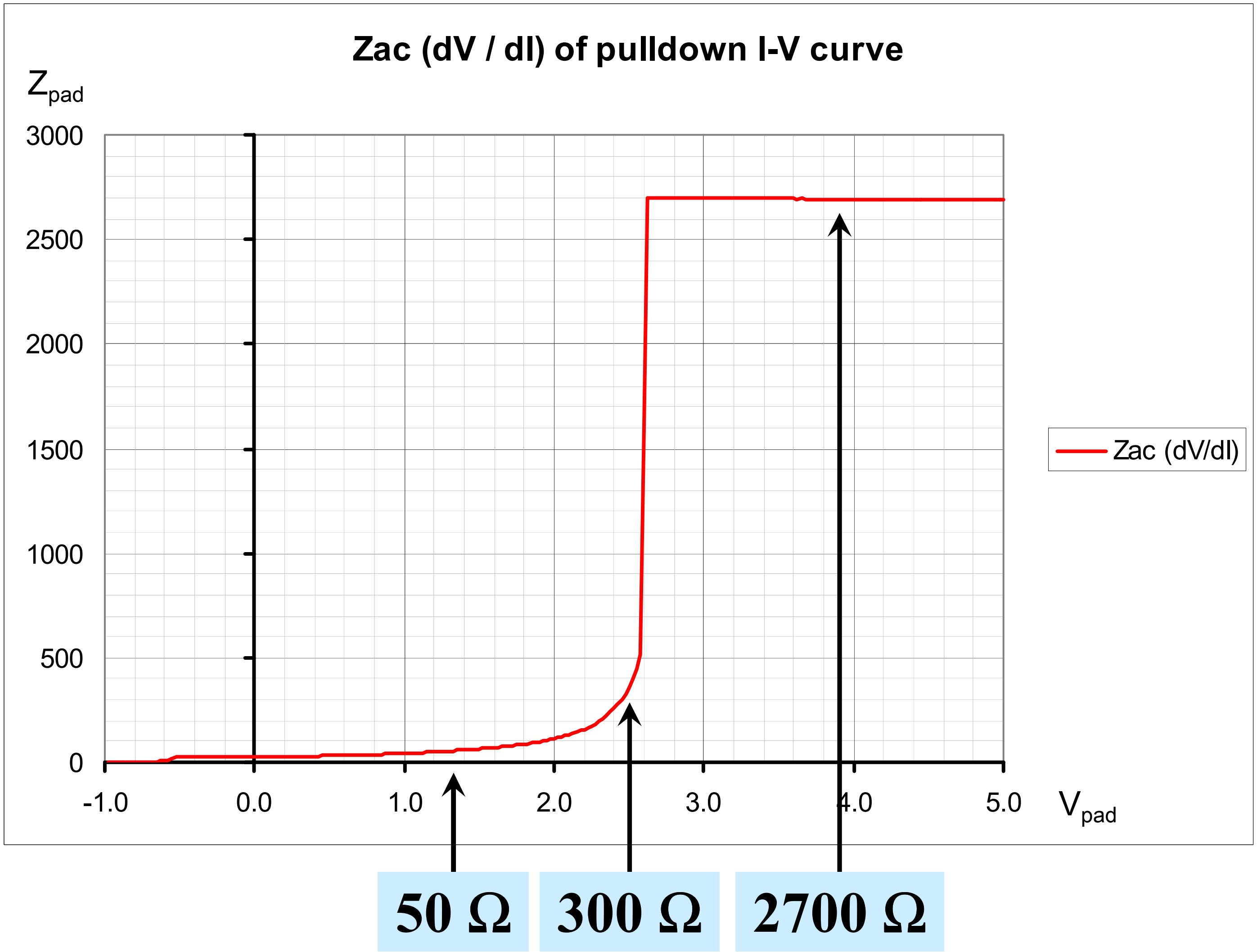
I-V curve of a pulldown transistor



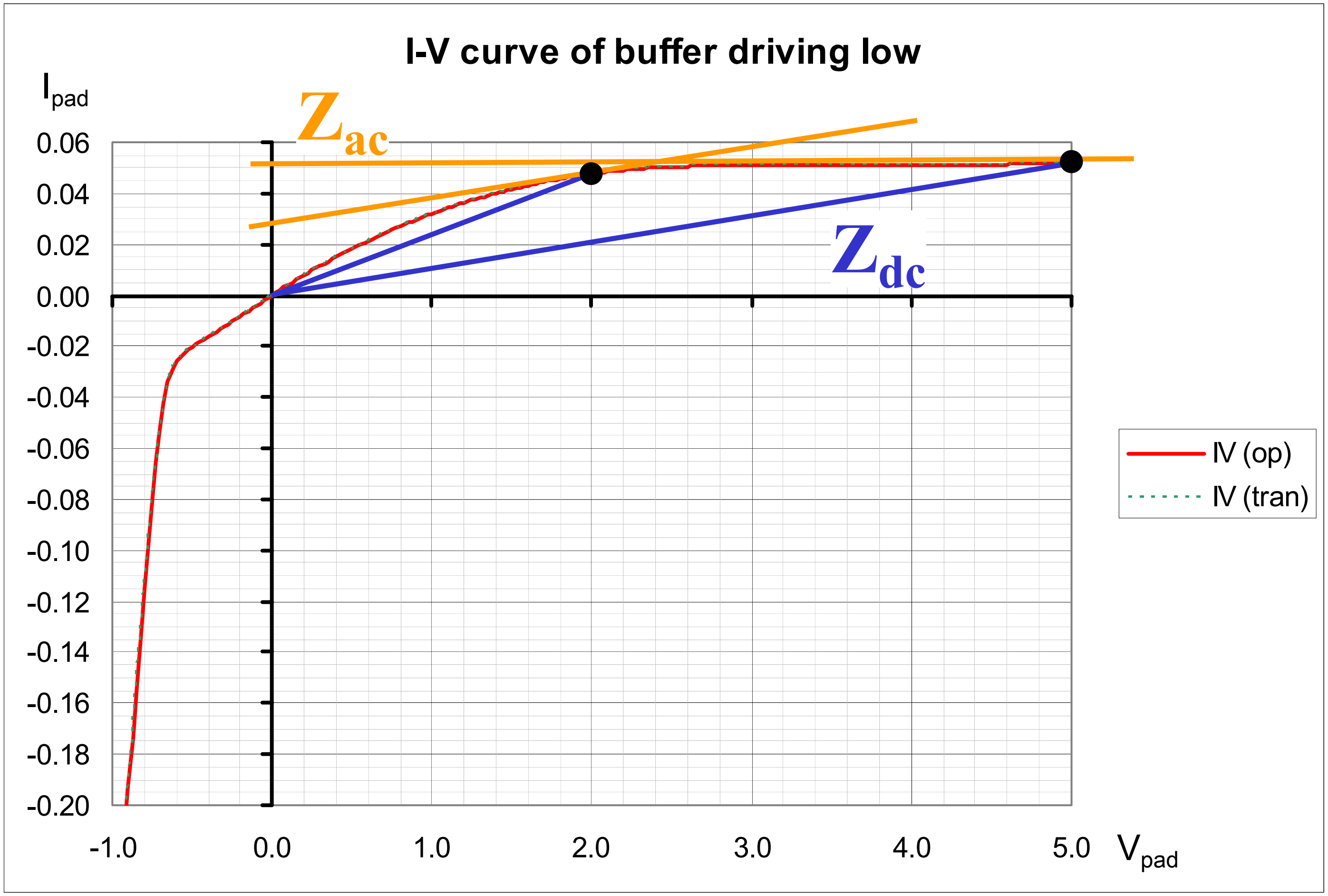
Z_{dc} (V / I) curve of a pulldown transistor



Z_{ac} (dV / dI) curve of a pulldown transistor



Putting them all together



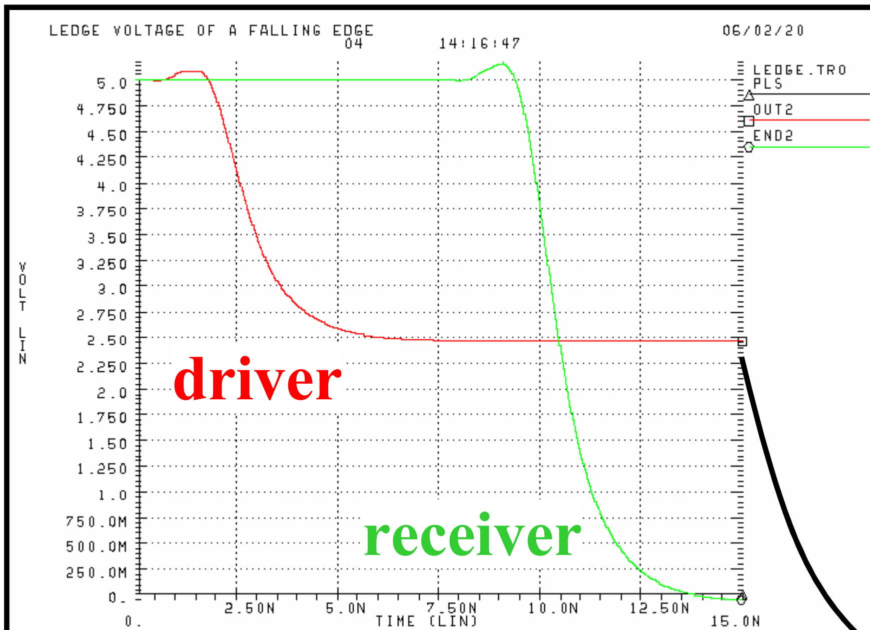
$dZ_{dc} \neq Z_{ac}$!!!

Notes on behavioral modeling

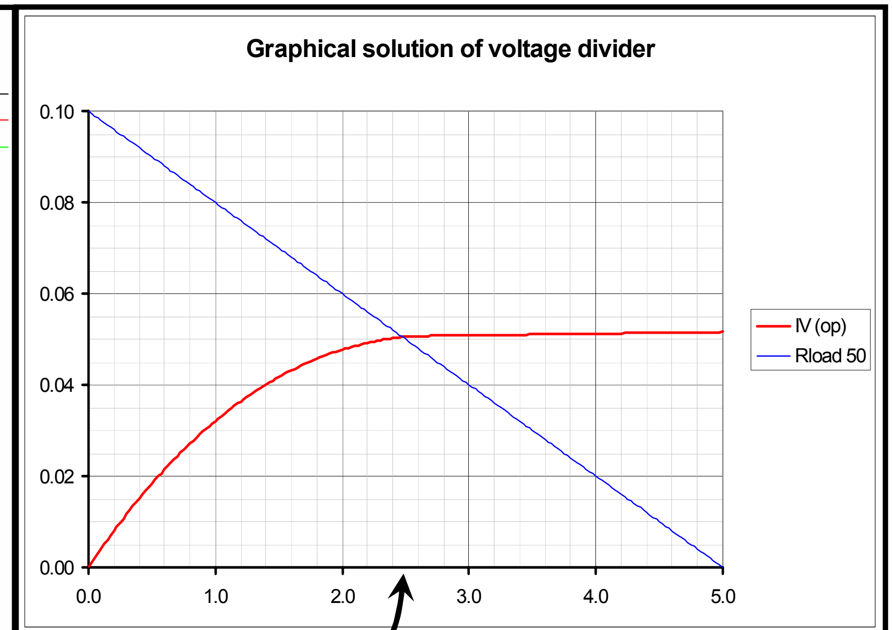
- **Beware of how simulators work in the frequency domain!**
  - first they obtain the DC operating point solution
    - finding a point on the I-V table, or R-V table
  - then they obtain a linearized (small signal) AC model for the circuit at that operating point
  - if you are using an I-V table (PWL source), this AC model will use the tangent to the I-V curve (derivative)
  - if you are using an R-V table (PWL source), this AC model will use the R value that is found in the R-V table at the operating point
    - the derivative or R is still R!
- **The R-V table and I-V table models will give different results in frequency domain (.AC) simulations!**
  - your resonance effects will be unrelated between TD and FD!
- **In time domain (.TRAN) simulations the R-V and I-V models give identical results**
  - this is most likely because the large signal R-V and I-V models provide identical current-voltage relationships between iterations

Determining the voltage swing

- The DC level of a signal is determined by the voltage divider formed by the buffer and the load
- The value of the voltage can be found graphically by drawing the load line over the I-V curve
- Use the impedance of the T-line and Z_{dc} of the buffer to determine the initial “ledge voltage” of a transition



Waveform of driver and receiver

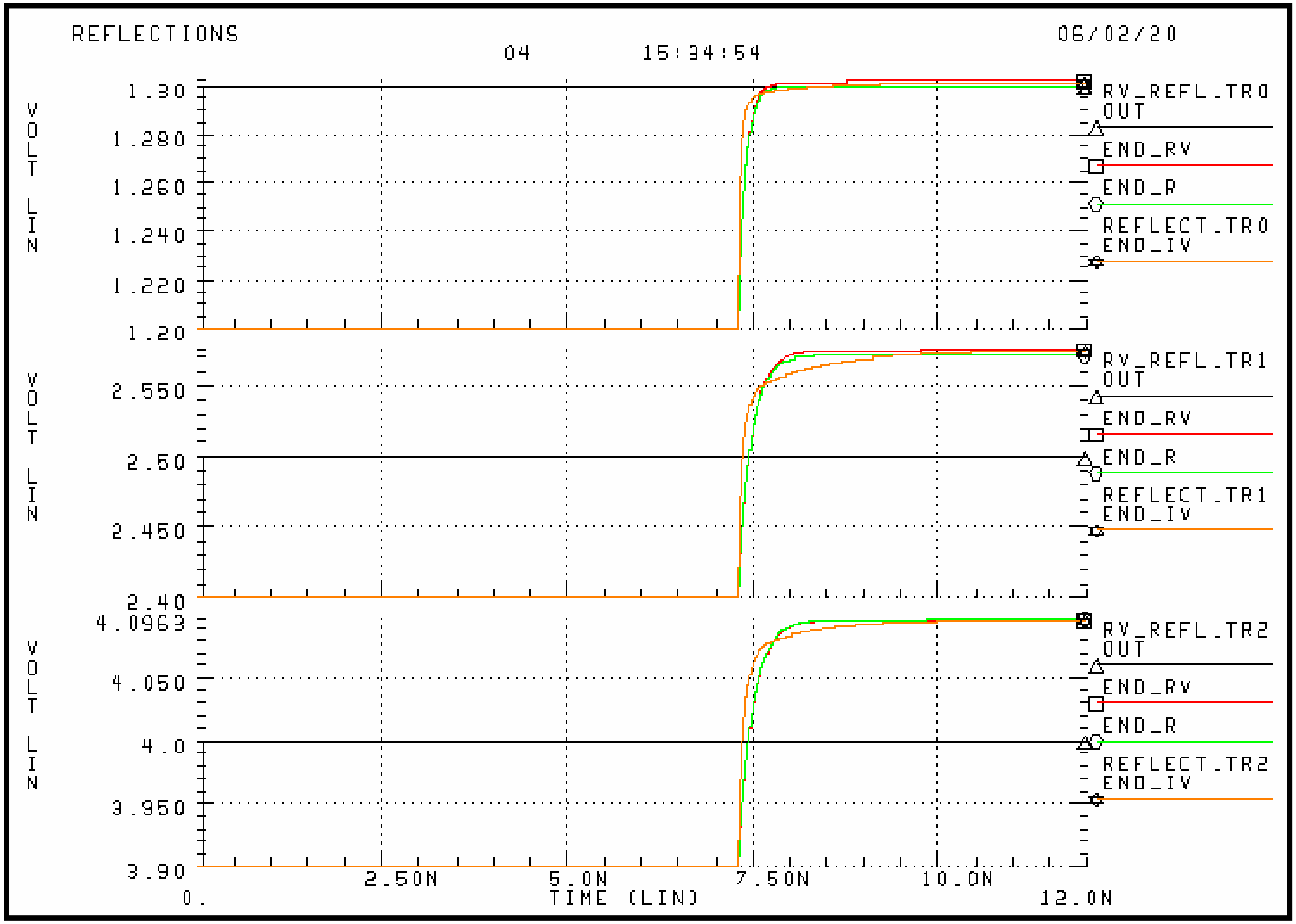


I-V curve / load line

Determining the amount of reflection

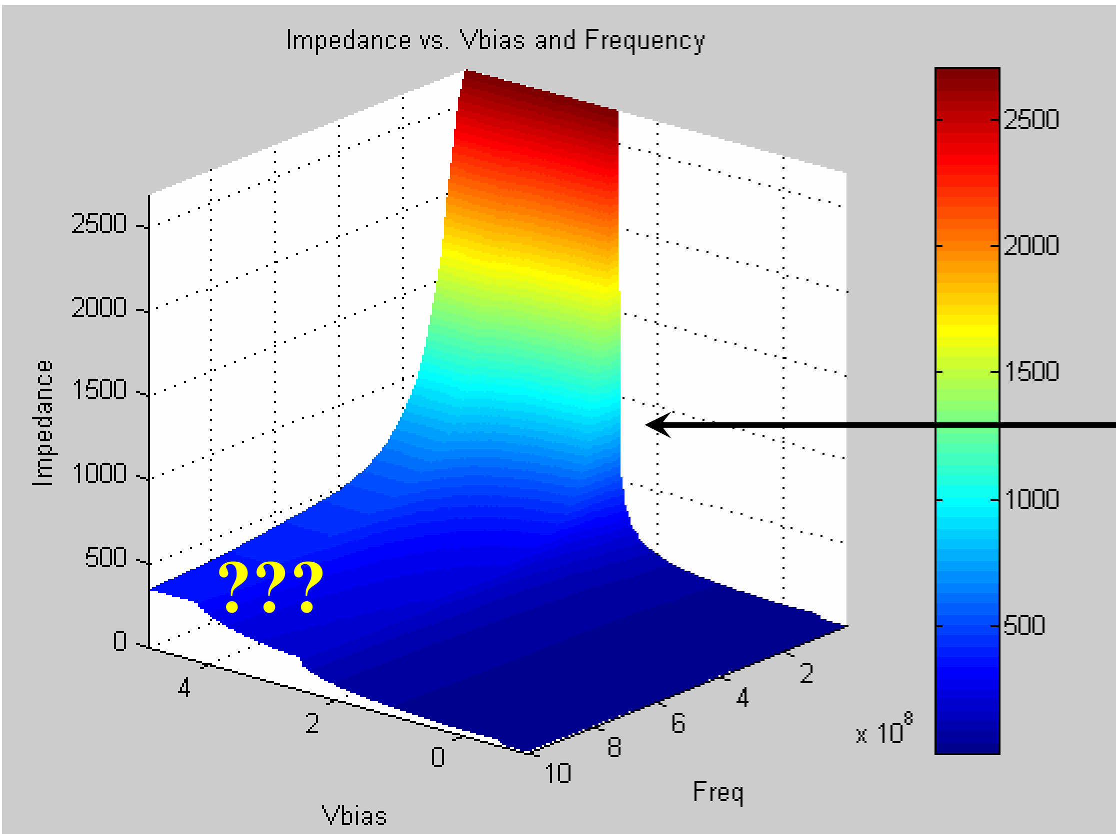
- It is the ratio between the impedance of the T-line and Z_{ac} of the buffer that determines the amount of reflection

$$\Gamma = \frac{Z_{drv} - Z_{load}}{Z_{drv} + Z_{load}}$$



Frequency dependence

- We can measure Z_{ac} directly with a .AC sweep
- Z_{ac} can be calculated from $Re(V_{ac})/ Re(I_{ac})$
- Z_{ac} is then available for the range of frequency swept with .AC
- A V_{dc} offset with the AC source provides the voltage dependency

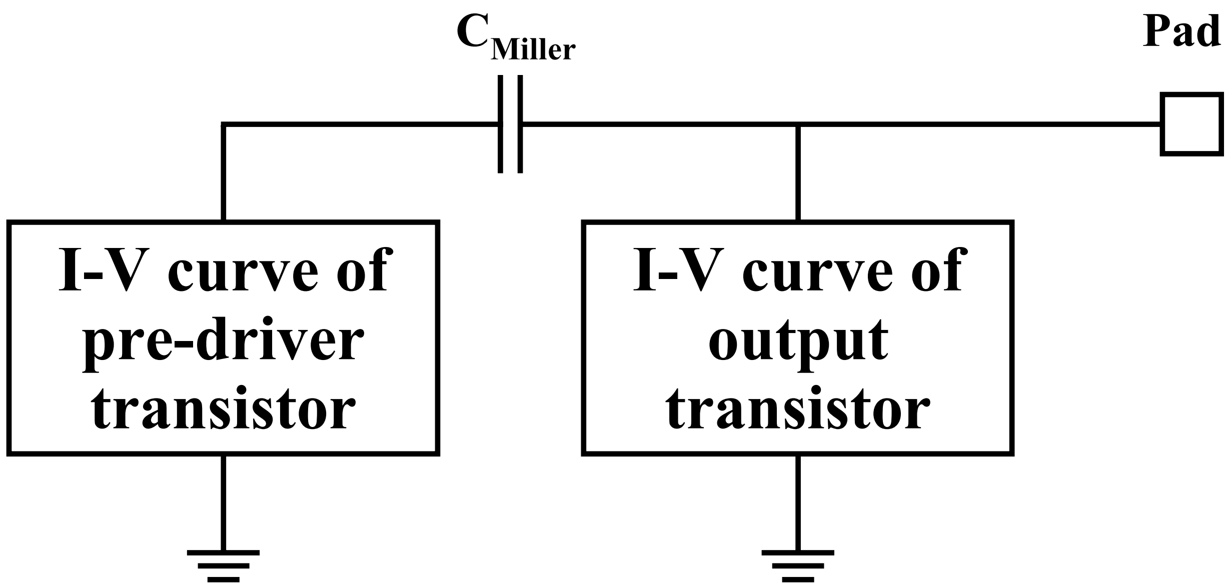


Good match with dV/dI method

Explanation of frequency dependence in Z_{ac}

- **The decreasing high frequency impedance response can be explained with a Miller capacitance, coupling the pre-driver impedance to the output pad**
- **The circuit shown here also agrees with the analysis results of BIRD 79 and the accompanying presentations**

http://www.vhdl.org/pub/ibis/birds/bird79.txt
http://www.eda.org/pub/ibis/summits/mar02/giacotto.pdf
http://www.eda.org/pub/ibis/summits/jun02/giacotto.pdf



Conclusions

- **A "linear" driver will show less of this effect because it operates in the linear region of its I-V curve where its Z_{ac} is usually lower than the pre-driver's Z_{ac}**
- **A "current mode" driver will show this effect very clearly because it operates mostly in the saturation region where Z_{ac} is high relative to the pre-driver's Z_{ac}**
- **A behavioral model omitting these high frequency effects may not be accurate for GHz simulations!**
- **Be aware of these effects when writing I-V curve linearity specs!**